Transactions Briefs

Phase Noise Simulation and Estimation Methods: A Comparative Study

Yuxian Ou, Nathen Barton, Radu Fetche, Nilakantan Seshan, Terri Fiez, Un-Ku Moon, and Kartikeya Mayaram

***Abstract*—A comparison of various simulation and estimation methods available to predict the phase noise in oscillators is presented in this paper. The phase noise of two ring oscillators and one radio frequency CMOS oscillator was determined using the Hajimiri and Lee phase noise analysis method, and the commercial simulators SpectreRF and EldoRF. Good agreement was obtained between the estimated and simulated phase noise performances. These oscillators were fabricated in a 0.35-μm CMOS process. The measured data also shows reasonable agreement with the analysis and simulations.**

***Index Terms*—Noise simulation, oscillators, oscillator noise, phase noise analysis, phase noise simulation.**

I. Introduction

With the growth of wireless communication systems and stringent performance requirements, the issue of phase noise in oscillators has become an important consideration in the design of oscillators. Several publications addressing phase noise have been published [1]–[9]. Recently, Hajimiri and Lee (H&L) [1] have proposed a time variant model based on the impulse sensitivity function to predict phase noise. This technique provides insight into the design of oscillators. Commercially available software packages also have the capability to simulate phase noise in oscillators. Two examples are SpectreRF [10] and EldoRF [11]. Since all of these methods follow different schemes to simulate phase noise, there is a need to compare the predicted phase noise from these three methods. Furthermore, it is important to know how the predicted phase noise from these methods compares with the measured phase noise of actual oscillators.

In this paper, we have compared the phase noise results obtained from the H&L analysis [1], SpectreRF, EldoRF and measurements for two ring oscillators and one radio frequency (RF) *LC* oscillator. The intent is to provide an objective comparison of the results without getting into simulator specific details. It is expected that a summary of these results would be beneficial to other researchers. The paper is organized as follows: The various oscillator circuits used for the comparison are

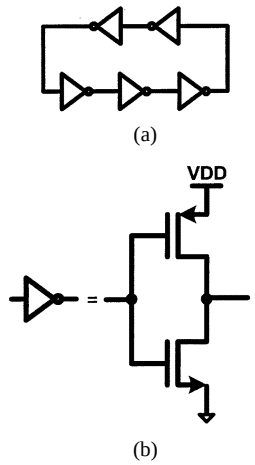


Fig. 1. (a) Simple five-stage ring oscillator. (b) Unit delay cell.

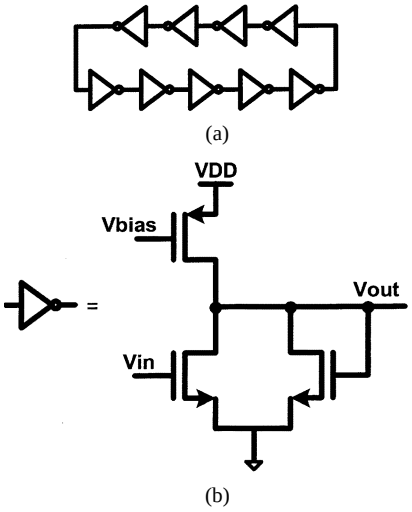


Fig. 2. (a) Nine-stage current starved ring oscillator. (b) Unit delay cell.

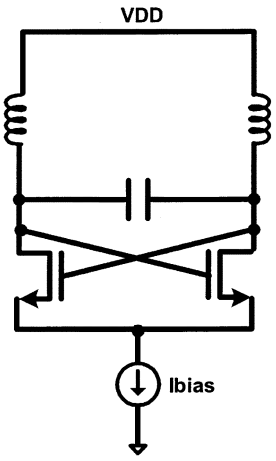


Fig. 3. Cross-coupled LC oscillator.

Manuscript received January 25, 2002; revised October 24, 2002. This paper was recommended by Associate Editor A. Hajimiri. This work was supported in part by the National Science Foundation (NSF) Center for Design of Analog and Digital Integrated Circuits (CDADIC) and in part by the NSF under Grant CCR-0096176.

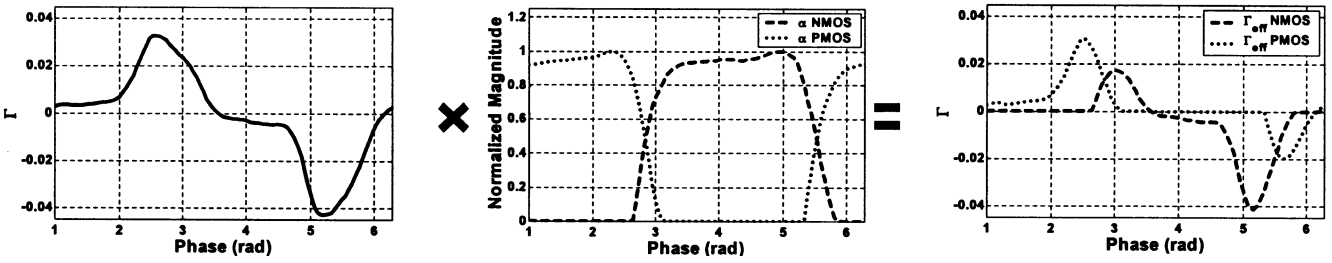
Y. Ou was with the Department of Electrical and Computer Engineering, Oregon State University, Corvallis, OR 97331 USA. He is now with Cypress Semiconductor, Woodinville, WA 98072 USA.

N. Barton and N. Seshan were with the Department of Electrical and Computer Engineering, Oregon State University, Corvallis, OR 97331 USA. They are now with Texas Instruments, Dallas, TX 75243 USA.

T. Fiez, U.-K. Moon, and K. Mayaram are with the Department of Electrical and Computer Engineering, Oregon State University, Corvallis, OR 97331 USA (e-mail: karti@ece.orst.edu).

R. Fetche is with the School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA 99164 USA.

Digital Object Identifier 10.1109/TCSII.2002.806739



(a) (b)

Fig. 4. (a) Impulse sensitivity function. (b) Noise modulation functions. (c) Effective impulse sensitivity functions.

described in Section II. Section III discusses the H&L phase noise estimation and our implementation. The comparison of results obtained from the H&L analysis, SpectreRF, EldoRF and measurements is given in Section IV. Conclusions are presented in Section V.

II. Oscillator Circuits

Three oscillator circuits have been fabricated in the 0.35-μm Taiwan Semiconductor Manufacturing Corporation (TSMC) CMOS process. A brief description of these is provided below.

Oscillator 1: Simple Five-Stage Ring Oscillator

A simplified schematic of a simple five-stage ring oscillator is shown in Fig. 1. The measured oscillation frequency was 261 MHz with a 3 V supply voltage, and was determined completely by parasitic capacitances. The transistors were sized to provide equal rise and fall times. The noise sources are the NMOS and PMOS transistors of each stage, which undergo complete rail-to-rail switching and thus cyclostationary noise modulation [1].

Oscillator 2: Current Starved Nine-Stage Ring Oscillator

In this oscillator, shown in Fig. 2, the oscillation frequency is controlled by a PMOS current source, and the voltage swing is limited with a diode connected NMOS device [Fig. 2(b)]. The measured oscillation frequency was 108 MHz with a 3-V supply voltage. Because the level of $Vbias$ is constant over many cycles, the PMOS transistor's noise sources can be considered to be stationary, while both NMOS transistors' noise sources are modulated periodically.

A. Oscillator 3: LC Cross-Coupled Oscillator

An LC cross-coupled oscillator circuit is shown in Fig. 3. This oscillator, designed for a GPS application, had a measured oscillation frequency of 1.64 GHz with a 3-V supply voltage. The inductors were implemented as on-chip planar spirals, and an off-chip bipolar transistor current source was used for biasing. The third and fourth metal layers were stacked together to form the inductors. This stacked inductor had a better quality factor as compared to a similar inductor on the fourth metal layer only. In this oscillator, the significant phase noise contributors are the switching transistors and the series resistance of the spiral inductors. The noise sources for the switching transistors are periodically modulated.

III. H&L Analysis Implementation

In the Hajimiri and Lee analysis method [1], [2], the excess phase of an oscillator due to an arbitrary noise source is given by

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\,\tau) i(\tau)\, d\tau = \frac{1}{q_{\max}} \int_{-\infty}^{\infty} \Gamma(\omega_0 \tau) i(\tau)\, d\tau \qquad (1)$$

where $i(\tau)$ is the current injected at the node, and $\Gamma(\omega_0 t)$ is the *impulse sensitivity function* (ISF). The ISF is essentially a transfer function between an arbitrary noise source and the excess phase at the output of the oscillator.

Using this result, it can be shown that the phase noise of an oscillator due to thermal noise is [1], [2]

$$L\{\Delta\omega\} = 10 \cdot \log_{10}\left(\frac{\Gamma_{\rm rms}^2}{q_{\max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{2 \cdot \Delta\omega^2}\right) \qquad (2)$$

and the phase noise of an oscillator due to flicker noise is

$$L\{\Delta\omega\} = 10 \cdot \log_{10}\left(\frac{c_0^2}{q_{\max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{4 \cdot \Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega}\right). \qquad (3)$$

The quantity $\Gamma_{\rm rms}$ is the rms value of the ISF. In this work, all ISFs were obtained using Spectre time domain simulations by injecting small current pulses into an oscillator node over one oscillation cycle and observing the resulting phase shift several cycles later.

To complete the analysis, the cyclostationary nature of the noise sources must be considered. The ISF contains only the sensitivity to noise as a function of time, but it has no information as to the time duration for which a noise source is present. Hence, the effective ISF is given by

$$\Gamma_{eff}(x) = \Gamma(x) \times \alpha(x) \qquad (4)$$

where $\alpha(x)$ represents the noise modulation function [9].

As an example, consider the H&L analysis of the simple five-stage ring oscillator shown in Fig. 1. The simulated ISF with an injected charge of 0.1 pC, shown in Fig. 4(a), is nearly symmetric suggesting from (3) a small flicker noise corner. When the ISF is multiplied by the NMOS and PMOS noise modulation functions in Fig. 4(b), the effective ISFs are shown in Fig. 4(c). These ISFs are nonsymmetric and will cause a large amount of flicker noise upconversion as shown later.

IV. Comparison of SpectreRF, EldoRF, H&L and Measurements

The commercial simulation tools SpectreRF [10] and EldoRF [11] find the periodic steady state of the oscillator, by periodic steady-state (PSS) analysis in SpectreRF or steady-state (SST) analysis in EldoRF. The circuit is linearized around this operating trajectory and the resulting time-varying system is used to obtain the noise power spectral densities. The only difference in the output of these two simulators is that SpectreRF gives the single side-band phase noise power, whereas EldoRF gives the double side-band phase noise power. Hence, while comparing EldoRF and SpectreRF, the results obtained from EldoRF should be divided by two.

The simulations were performed on the three oscillator circuits described in Section II. Transistor models were extracted from the MOSIS run. The BSIM3v3 noise model was used for the thermal noise of the transistors. For the flicker noise, the SPICE2 flicker noise model was used [12] since parameter extraction was simpler. Measurements were done on a test transistor to characterize the flicker noise. A Burr–Brown low noise amplifier INA103 was used

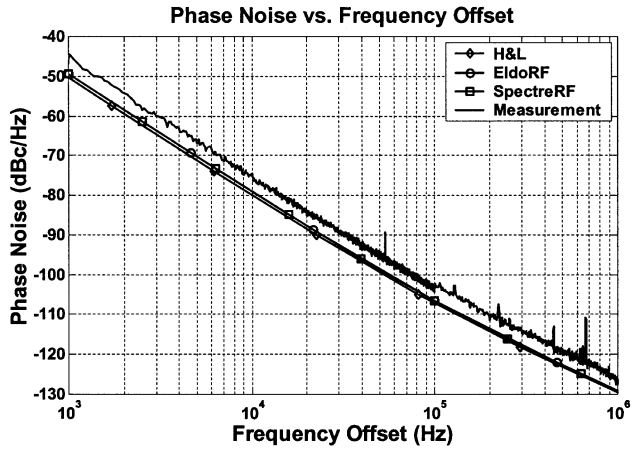


Fig. 5. Phase noise spectrum of the simple five-stage ring oscillator from H&L, SpectreRF, EldoRF, and measurement.

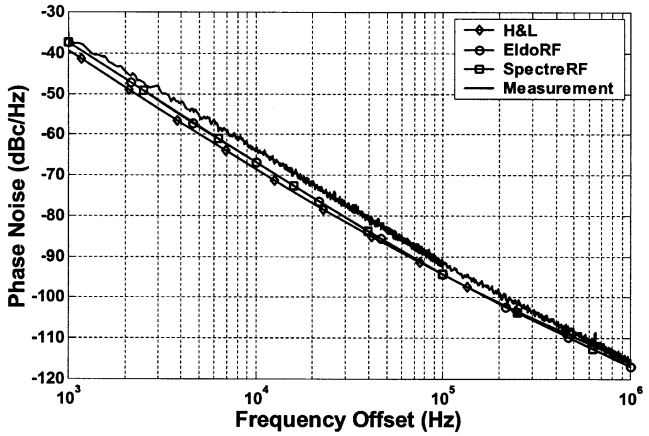


Fig. 6. Phase noise spectrum of the current starved nine-stage ring oscillator from H&L, SpectreRF, EldoRF, and measurement.

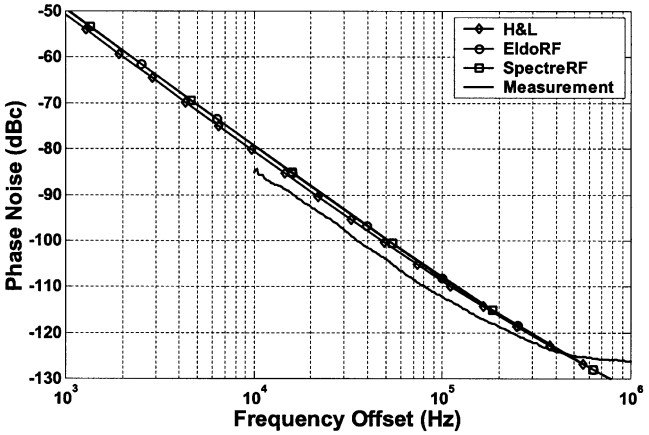


Fig. 7. Phase noise spectrum of the LC cross-coupled oscillator from H&L, SpectreRF, EldoRF, and measurement.

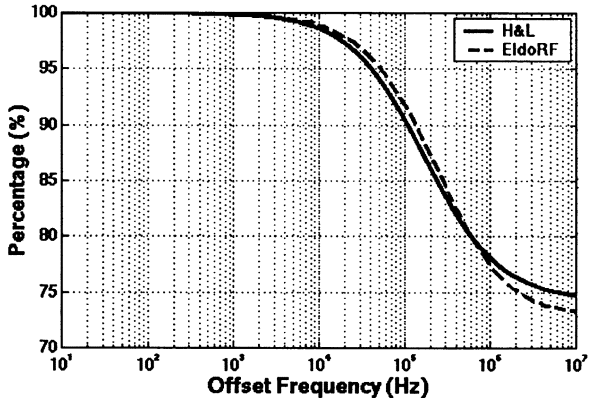
and the drain noise power spectral density was measured for the transistor. The $1/f$ noise corner frequency of approximately 2 MHz was obtained. The kf value required for the noise model was extracted from the noise power spectral density curve. For the H&L analysis the thermal noise power spectral density was taken as $\overline{i}_{nd}^{\,2}/\Delta f = (8/3)kTg_{ds0}$ where g_{ds0} is the value of g_{ds} for zero drain-source bias and the flicker noise was modeled as in SPICE2.

TABLE I
COMPARISON OF THE PHASE NOISE AT 1 MHZ OFFSET FROM THE CARRIER FOR THE NMOS CROSS-COUPLED OSCILLATOR

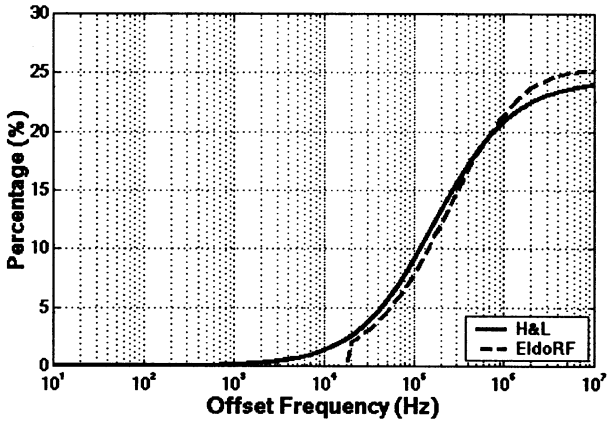
Ibias (mA)	SpectreRF (dBc/Hz)	EldoRF (dBc/Hz)	H&L (dBc/Hz)
0.2	-116.1	-115.7	-117.1
0.3	-120.2	-120.3	-121.4
0.4	-122.8	-122.6	-123.8
0.6	-122.6	-122.5	-124.8
0.8	-122.0	-122.4	-124.6

TABLE II
COMPARISON OF THE PHASE NOISE AT 1 MHZ OFFSET FROM THE CARRIER FOR THE COMPLEMENTARY CROSS-COUPLED OSCILLATOR

Ibias (mA)	SpectreRF (dBc/Hz)	EldoRF (dBc/Hz)	H&L (dBc/Hz)
0.1	-118.6	-118.2	-121.4
0.15	-123.3	-122.9	-126.0
0.2	-123.8	-123.4	-126.2
0.3	-122.3	-122.2	-122.0
0.4	-122.6	-122.7	-121.1



(a)



(b)

Fig. 8. (a) Noise contribution of the NMOS transistors. (b) Thermal noise contribution of the series resistance of the spiral inductor. There is good agreement between EldoRF simulations and H&L analysis.

The simple five-stage ring oscillator and the current-starved nine-stage ring oscillator were fabricated in the TSMC 0.35-μm three metal layer process whereas the LC cross-coupled oscillator was fabricated in the TSMC 0.35-μm four metal layer process. The measurements on these oscillators where compared with the simulation results from

SpectreRF, EldoRF, and the H&L model. These comparisons are shown in Figs. 5–7.

The comparisons show good agreement (within 5 dBc/Hz) between the simulated and measured phase noise characteristics. The difference between the results obtained from H&L analysis method and direct phase noise simulators SpectreRF and EldoRF is less than 2 dBc/Hz.

For further validation between these methods, we consider two CMOS oscillators (an NMOS cross-coupled pair and a complementary cross-coupled pair) designed for an operating frequency of 2.4 GHz in a 0.25-μm BiCMOS process. The details of these oscillators are provided in [13]. For the simulations presented here we used a fixed capacitance value instead of the switched capacitor bank used for tuning in the actual design. The comparisons of the simulators SpectreRF, EldoRF, and the H&L analysis method are summarized in Tables I and II for different values of the bias current. From this data it can be seen that SpectreRF and EldoRF are in very good agreement with differences less than 0.5 dBc/Hz. The H&L analysis is also in good agreement with the simulators except for some bias conditions in which the difference between the analysis and simulations is as large as 3 dBc/Hz.

Both SpectreRF and EldoRF have a feature that provides the contribution of each noise source to the phase noise at the output of the oscillator. This data can be used to gain insight into reducing the overall phase noise. As an example, consider the LC cross-coupled oscillator of Fig. 3. The noise contribution of the NMOS transistors and the series resistance of the spiral inductors as a percentage of the total output noise are shown in Fig. 8. It can be concluded that the flicker noise of the NMOS pair is a significant contributor to phase noise at frequencies smaller than the flicker noise corner. At larger offset frequencies the effect of series resistances of the inductors on phase noise becomes relatively larger (when compared to smaller offset frequencies). However, the active device noise still constitutes a larger portion of the total phase noise. These results are in agreement with extensions of the H&L analysis wherein the individual noise contributions are also obtained, as shown in Fig. 8. EldoRF is used as an illustration and similar results were obtained with SpectreRF.

V. Conclusion

The H&L phase noise analysis employs a linear time-variant model for the oscillator. It also gives physical insight into how device noise contributes to the overall phase noise. In this paper, we have compared the phase noise of three different oscillator structures from H&L analysis, SpectreRF and EldoRF. In addition, these oscillators were validated with measurements. Additional simulation based comparisons were also provided. The results from the H&L analysis and direct phase noise simulators were within 3 dBc/Hz, whereas the measurements were within 5 dBc/Hz of the simulation results for the oscillator circuits presented in this paper.

Acknowledgment

The authors would like to thank Texas Instruments for their help with the phase noise measurements. They also thank D. C. Lee for several discussions.

References

[1] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, pp. 179–194, Feb. 1998.
[2] ——, "Oscillator phase noise: A tutorial," *IEEE J. Solid-State Circuits*, vol. 35, pp. 326–336, Mar. 2000.
[3] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proc. IEEE*, vol. 54, pp. 329–330, Feb. 1966.
[4] L. S. Cutler and C. L. Searle, "Some aspects of the theory and measurement of the frequency fluctuations in frequency standards," *Proc. IEEE*, vol. 54, pp. 136–154, Feb. 1966.
[5] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, pp. 331–343, Mar. 1996.
[6] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," *IEEE J. Solid-State Circuits*, vol. 34, pp. 716–724, May 1999.
[7] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, pp. 790–804, June 1999.
[8] W. Robins, *Phase Noise in Signal Sources*. Stevenage, U.K.: Peregrinus, 1982.
[9] A. Hajimiri and T. H. Lee, *The Design of Low Noise Oscillators*. Norwell, MA: Kluwer, 1999.
[10] "Affirma RF simulator, Version 4.4.5," Cadence Design Systems, Dec. 1999.
[11] EldoRF, "Version v5.3_1.1, Mentor Graphics,", May 2000.
[12] W. Liu *et al.*, "BSIM3v3.2.2 MOSFET model – users' manual,", 1999.
[13] N. Seshan, J. Rajagopalan, and K. Mayaram, "Design of low power 2.4 GHz CMOS LC oscillators with low phase-noise and large tuning range," in *Proc. Int. Symp. Circuits and Systems*, May 2002, pp. 409–412.

A CMOS High-Speed Wide-Range Programmable Counter

Sang-Hoon Lee and Hong June Park

***Abstract*—A CMOS high speed wide-range programmable divide-by-N counter was designed and the performance was verified by SPICE simulations and the measurements on the fabricated chip. A new reloading scheme and the use of simplified circuits for three least significant bit flip-flops enabled the high-speed operation of the proposed counter, independently of the number of counter stages. The proposed and Chang's [1] counters were fabricated on the same chip using a 0.6-μm triple-metal CMOS technology. The proposed and Chang's counters with six stages were measured to work up to the clock frequencies of 1.34 GHz and 930 MHz, respectively.**

***Index Terms*—CMOS integrated circuits, counting circuits, digital circuits, frequency division, frequency synthesizer, high-speed electronics.**

I. Introduction

In modern communication systems, the frequency synthesizer is often used to generate high frequency outputs from a fixed low frequency input. The performance of frequency synthesizer is usually limited by the frequency divider and the voltage-controlled oscillator (VCO) [1]. Traditionally, high-speed frequency dividers were implemented in GaAs or BiCMOS technology [2], [3]. Recently, various CMOS implementations of high-speed frequency dividers were presented [1], [4]–[6]. However the programmability of frequency divisor value of most conventional high-speed frequency dividers is limited to two frequency values. These frequency dividers are called the dual-modulus prescalers. On the other hand, the wide-range frequency divider called the divide-by-N counter has a programmability of

Manuscript received March 28, 2001; revised September 24, 2002. This paper was recommended by Associate Editor M. Yu. This work was supported in part by the National Research Lab program, in part by the BK21 Program of the Korean government, and in part by the Multi-Project Wafer (MPW) program of the IC Design Education Center (IDEC) of Korea.

The authors are with the Electrical and Computer Engineering Division, Pohang University of Science and Technology, Pohang, Kyungbuk, 790-784, Korea (e-mail: hjpark@postech.ac.kr).

Digital Object Identifier 10.1109/TCSII.2002.805627