A 1V 10b 30MSPS Switched-RC Pipelined ADC

Gil-Cho Ahn, Min Gyu Kim, Pavan Kumar Hanumolu and Un-Ku Moon

School of EECS, Oregon State University, Corvallis, OR 97331

***Abstract*— A 10b 30MS/s pipelined ADC using fully-differential switched-RC multiplying digital-to-analog converter (MDAC) is presented. It utilizes a resistive loop to reset the feedback capacitor in the MDAC without using the floating switch. The measured differential and integral nonlinearities of the prototype IC fabricated in a 0.13μm CMOS process are less than 0.54 LSB and 1.75 LSB respectively. The prototype ADC achieves 51.6dB SNDR and 65.9dB SFDR with 1V supply while consuming 17mW power.**

I. Introduction

The continued down-scaling of CMOS technology requires similar scaling of the supply voltage to ensure device reliability. Digital circuits gracefully scale with the technology, thus maximizing the benefits offered by advanced CMOS processes. However, the design of interface circuits such as filters and data converters operating under low supply voltage poses several design challenges. In particular, switched capacitor (SC) circuit technique, that have been the preferred means of implementing data converters in CMOS technology, suffer from severe performance degradation due to floating switches. Existing low-voltage circuit techniques, such as switched-opamp [1] and opamp-reset switching technique [2], eliminated the floating switch by using the previous stage output to reset the following stage sampling capacitor. However, these techniques required two different common-mode levels between phases, and they are difficult to design using fully-differential circuits. In this paper, we present an alternative design technique that enables low-voltage fully-differential operation. A 1 V 10-bit 30 MSPS CMOS pipelined ADC is presented to demonstrate the proposed technique. The paper is organized as follows: a brief overview of the ADC architecture is presented in Section II; the proposed low-voltage multiplying digital-to-analog converter (MDAC) is discussed in detail in Section III; and the experimental results validating the proposed design techniques are presented in Section IV.

II. ADC Architecture

A block diagram of a conventional 10-bit pipelined ADC is shown in Fig. 1. It consists of a cascade of nine 1.5-bit stages. Each of these stages consists of a 3-level sub-ADC and an MDAC to generate the residue. This architecture has a built-in redundancy of half an LSB ($1/4V_{ref}$) in each stage thus permitting large comparator and amplifier offsets. In order to reduce power consumption, no dedicated front-end sample and hold amplifier (SHA) is employed, at the expense of reduced margin for comparator and amplifier offsets correction range. Sampling capacitors and bias currents in the later stages of the pipeline were scaled down to reduce the power consumption and area. There are two major difficulties in implementing this ADC to operate at sub-1V supply voltage. First, the floating switches required to implement the conventional MDAC are inoperable at low supply voltages. Second, fully differential amplifiers and comparators either perform poorly or are not functional at low supply voltages. In the following section we present an MDAC that utilizes switched-RC technique to obviate the need for floating switches. Circuit design techniques to implement low-voltage fully differential amplifier and comparator will also be discussed.

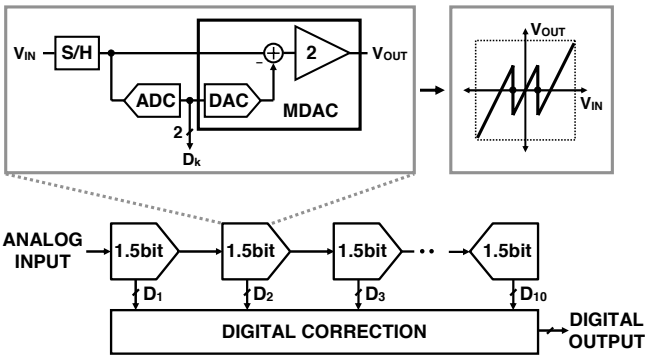

Fig. 1. 10-bit pipelined ADC architecture.

III. Low Voltage Circuits Implementation

A. MDAC with switched-RC technique

The proposed fully differential MDAC is shown in Fig. 2. There are two major differences between the proposed and the conventional MDAC [3]. First, the switched capacitor based input sampling network of a conventional MDAC is replaced by a switched-RC branch consisting of switches MSP, MSN, R_1 and C_{S1} [4][5]. Second, resistive feedback is employed to reset the feedback capacitor (C_{F1}), thus achieving a distinct multiplying amplifier operation in contrast to integrator operation in [4]. These two changes obviate the need for floating switches at the input and in the feedback respectively. The operation of the proposed MDAC will be discussed in detail now.

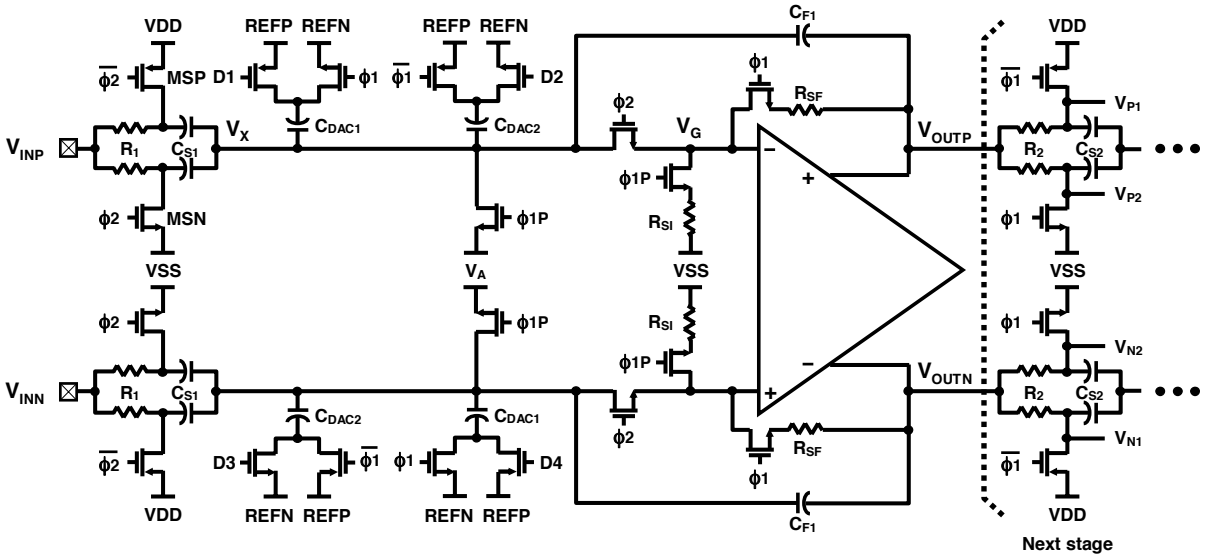

Fig. 2. Schematic of the low-voltage fully-differential switched-RC MDAC.

During Φ_1 phase, the input signal is sampled into the capacitor C_{S1} through the resistor R_1 while C_{DAC1} and C_{DAC2} are pre-charged to REFN and REFP respectively. At the same time, feedback capacitor C_{F1} is reset, by connecting the top plate to virtual ground bias level V_A, and the bottom plate to the output common-mode level provided by the amplifier through the resistive feedback path. In this phase, the amplifier virtual ground node is biased by appropriately choosing the resistor values for R_{SI} and R_{SF}. The expression for the node voltage V_G is given by

$$V_G = (VCMO - VSS)\,\frac{R_{SI}}{(R_{SI} + R_{SF})} \cong V_A \qquad (1)$$

where VCMO = (VDD + VSS)/2 is the nominal output common-mode level of the amplifier and V_A is the input common-mode bias level of the amplifier. Unlike switched-opamp and opamp-reset techniques which have different output common-mode level for each clock phase, the proposed resistive reset technique maintains constant output common-mode level during both phases. This feature eases the design of common-mode feedback amplifier for the fully-differential implementation. During the following Φ_2 phase, the signal charge in C_{S1} and the charge from the DAC capacitors is transferred to the feedback capacitor C_{F1} to produce the residue voltage at the output of the opamp.

A disadvantage of the switched-RC technique employed in Nyquist-rate data converters without sample and hold amplifier is that during amplification phase Φ_2 (input branch is reset; see Fig. 2), a small fraction of the input appears at the V_X node due to finite ON resistance of switches MSN and MSP. This input leakage introduces non-linearity into the overall ADC characteristic. In order to suppress this non-ideality, three cascaded switched-RC branches as shown in Fig. 3 are used in the first stage of the ADC [6].

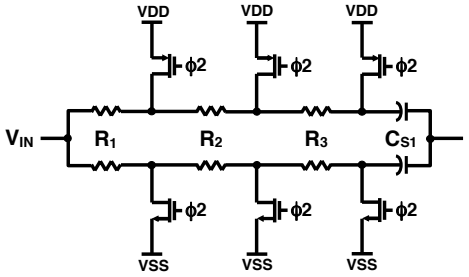

Fig. 3. Cascaded SRC branches.

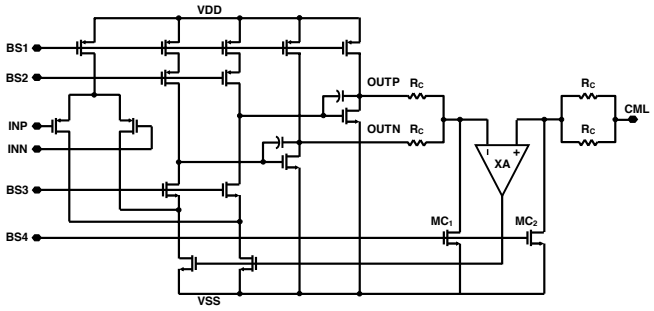

Fig. 4. Fully-differential low-voltage opamp.

B. Amplifier design

The circuit diagram of the amplifier is shown in Fig. 4. An internally compensated two-stage fully-differential amplifier was used to achieve high gain and large output swing under low supply voltage. The main difficulty in building a fully-differential low-voltage amplifier is the design of a common-mode feedback (CMFB) circuit. To maximize output swing,

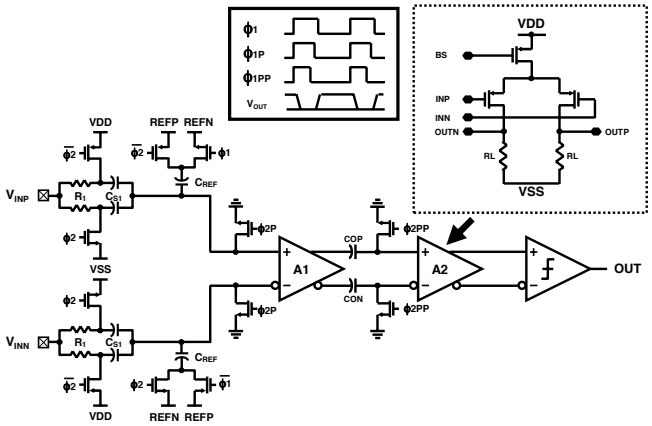

Fig. 5. Low-voltage comparator.

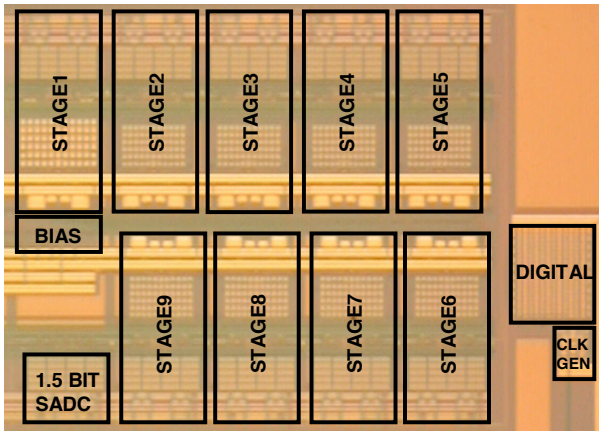

Fig. 6. Chip micrograph.

an output common-mode level of (VDD+VSS)/2 is used. However, under low supply voltage, this output common-mode level cannot be directly fed to the input of CMFB amplifier due to its limited input common-mode range. To alleviate this problem, a level shifting block consisting of resistor R_C and the current sources MC_1, MC_2 is used in this design [5]. Both the common-mode reference level (CML) and output common-mode level of the main amplifier were shifted by the voltage drop across these resistors in order to bring these voltages to within the input common mode range of the amplifier XA.

C. Sub-ADC design

The schematic of the low-voltage comparator is shown in Fig. 5. Instead of sharing the switched-RC input branch of the MDAC, each sub-ADC block has its own resistor and switch for switched-RC sampling. The use of a dedicated sampling branch reduces the noise coupled from the comparators to the MDAC input. The comparator also uses two preamps to cancel offset and prevent kick-back noise from the latch. The second amplifier A2 provides level shifting by using resistor as load and sets the common-mode level of the following latch input to $I_{BIAS}R_L/2$, where I_{BIAS} is the bias current of the amplifier A2. Two comparators are used to implement the 3-level sub-ADC with threshold levels nominally set at $\pm 1/4VREF$.

IV. Experimental Results

The prototype 10-bit pipelined ADC was fabricated in a $0.13\mu m$ CMOS technology, and occupies $1.6 \times 1.2\ mm^2$ active die area. The chip micrograph is shown in Fig. 6. The measured differential and integral nonlinearities (DNL and INL) are illustrated in Fig. 7. The measured DNL and INL are +0.49/-0.54 LSB and +1.75/-1.24 LSB, respectively, at 30MSPS with 1V supply voltage. Fig. 8 shows the measured power spectrum of the output for a 3MHz, 0.8V peak-to-peak differential input sine wave with 30MHz sampling frequency. The measured SNDR and SFDR are 51.6dB and 65.9dB, respectively. The measured dynamic performance versus supply

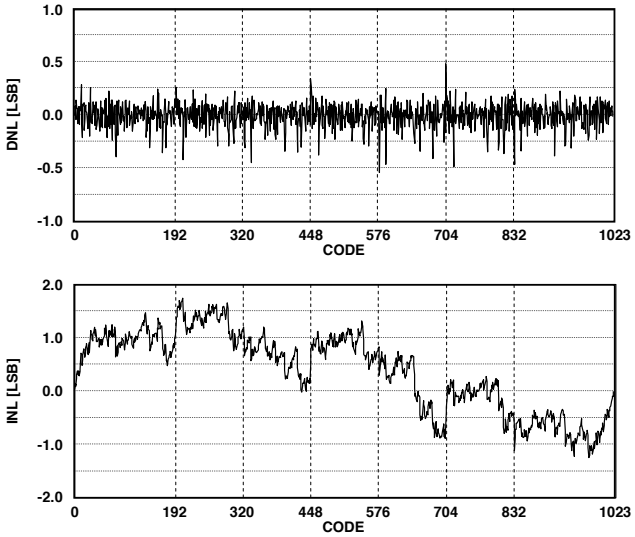

Fig. 7. Measured DNL/INL.

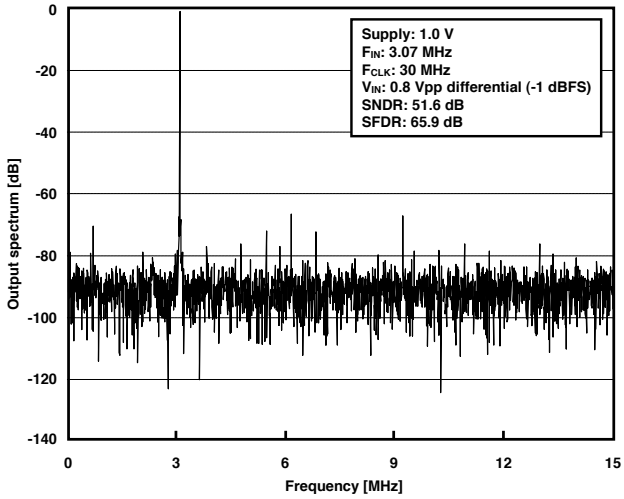

Fig. 8. Measured output spectrum.

voltage is shown in Fig. 9. The overall performance of the ADC is summarized in Table I.

V. Conclusion

A 10-bit 30MSPS CMOS pipelined ADC operating with 1V supply is described. The prototype IC demonstrates the very first implementation of resistive feedback reset and switched-RC techniques for low-voltage MDAC operation. The measured results of the prototype IC fabricated in a $0.13\mu m$ CMOS technology verify the validity of the proposed design techniques for low-voltage operation.

Acknowledgment

The authors would like to thank Samsung Electronics for providing IC fabrication, and V. Kratyuk for his help with the board design. This work is supported by the Semiconductor Research Corporation under contract 2005-HJ-1308, and partly by NSF CAREER CCR-0133530.

References

[1] J. Crols and M. Steyaert, "Switched opamp: An approach to realize full CMOS SC circuits at very low supply voltages," *IEEE J. Solid-State Circuits*, vol. 29, pp. 936-942, August 1994.

[2] D. Chang and U. Moon, "A 1.4-V 10-bit 25 MSPS pipelined ADC using opamp-reset switching technique," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1401-1404, August 2003.

[3] S. Lewis, H. Fetterman, G. Gross, R. Ramachandran, T. Viswanathan, "A 10-b 20-Msample/s analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 27, pp. 351-358, March 1992.

[4] G. Ahn *et al*., "A 0.6-V 82-dB delta-sigma audio ADC using switched-RC integrators," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2398-2407, December 2005.

[5] M. Kim *et al*., "A 0.9V 92dB double-sampled switched-RC $\Delta\Sigma$ audio ADC," *IEEE VLSI Circuits Symposium*, June 2006.

[6] J. Li, G. Ahn, D. Chang, and U. Moon, "A 0.9-V 12-mW 5-MSPS algorithmic ADC with 77-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 40, pp. 960-969, April 2005.

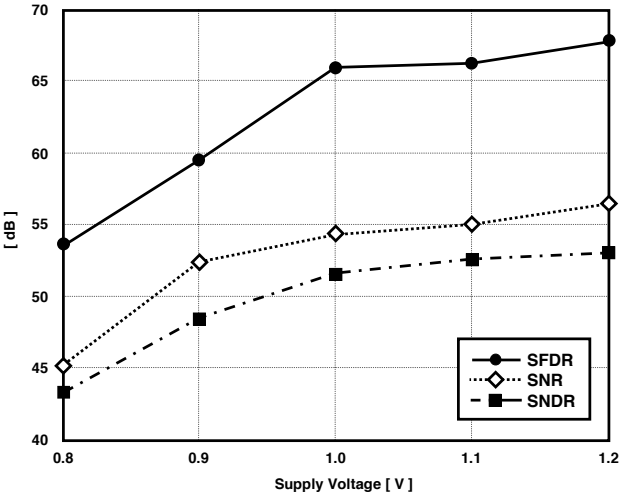

Fig. 9. SNR, SNDR and SFDR vs. supply voltage.

TABLE I
Performance Summary

Supply Voltage	1V
Resolution	10bits
Clock Frequency	30MHz
Input range	$0.9V_{pp}$ differential
DNL	+0.49/-0.54LSB
INL	+1.75/-1.24LSB
SNDR	51.6dB (Fin = 3.07MHz)
Power consumption	17mW
Active Die Area	$1.92mm^2$
Technology	$0.13\mu m$ CMOS