

Mismatch-shaping switching for two-capacitor DAC

J. Steensgaard, U. Moon and G.C. Temes

A mismatch-shaping scheme is proposed for a two-capacitor digital-to-analogue converter (DAC). It uses a delta-sigma loop for finding the optimal switching sequence for each input word. Simulations indicate that the scheme can be used for the realisation of DACs with 16 bit linearity and SNR performance.

Introduction: A very economical digital-to-analogue converter (DAC) containing only two capacitors, a reference voltage source and a few switches (Fig. 1) was described by Suarez *et al.* [1]. It functions by charging C_1 to V_{ref} or 0 depending on the incoming bits (starting with the least significant bit (LSB), and repeatedly sharing the charge between C_1 and C_2). It is somewhat slow; it requires N clock periods to convert an N bit digital word into an analogue voltage. However, it requires only a small chip area and little DC power, and is fully compatible with CMOS technology. A major disadvantage of the circuit is that its linearity is limited by the matching of the two capacitors, which (even for careful layout) cannot be much better than 0.1%, corresponding to only about 12 bit linearity. Recently, several papers [2, 3] have discussed methods for eliminating or reducing this nonlinearity, by using sophisticated algorithms for the operation of the switches so that C_1 and C_2 can change roles in every clock cycle, and by duplicating the DAC and combining the two resulting analogue outputs. These algorithms, however, require very complex logic and introduce new practical problems associated with the precise addition of the analogue outputs.

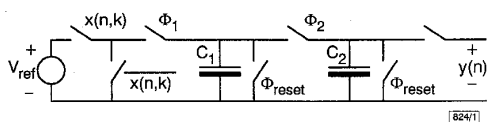


Fig. 1 Basic two-capacitor DAC topology

This Letter proposes a different approach which randomises the DAC error caused by mismatch, and performs a highpass filtering of the resulting noise. Thus, for oversampled operation, the inband portion of the error spectrum is suppressed. The technique does not require duplication of the analogue part of the DAC, and the digital correction system needed is much simpler than those used in the earlier schemes [2, 3].

Proposed system: The block diagram of the proposed system is shown in Fig. 2. In the upper part of the Figure, $x(n, k)$ denotes the k th bit of the n th input word $x(n)$, $y(n)$ is the corresponding analogue output sample, $V_{ref}\epsilon(n)$ is the error in $y(n)$, and $t(n, k) = \pm 1$ controls the choice of C_1 or C_2 when $x(n, k)$ is converted. In the lower part, $\epsilon_d(n) = 0$ is the desired average value of $\epsilon(n)$, $\epsilon^*(n)$ is the output of the digital lowpass filter $H(z)$, $t(n)$ is the n th word containing the signs $t(n, k)$, and $\hat{\epsilon}(n)$ is the computed value of the error $\epsilon(n)$ in $y(n)$. The P/S blocks perform parallel-to-serial conversion, and the T blocks truncate the data. The digital delays needed for timing are ignored for simplicity in Fig. 2.

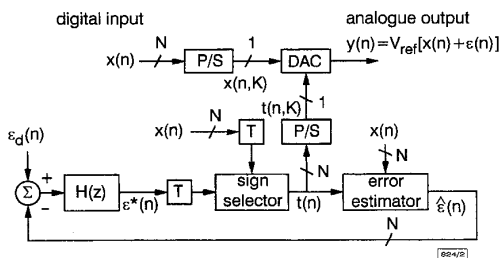


Fig. 2 Proposed mismatch-shaping system

Clearly, the lower part is a delta-sigma loop which attempts to keep the average value of $\hat{\epsilon}(n)$ equal to $\epsilon_d(n) = 0$ over a large range of n values. More specifically, the loop forces the z -trans-

form $\hat{E}(z)$ of the computed error $\hat{\epsilon}(n)$ to satisfy $\hat{E}(z) \approx E_\epsilon(z) + Q(z)/H(z)$, where $Q(z)$ is the z -transform of $q(n) = \hat{\epsilon}(n) - \epsilon^*(n)$, i.e. the quantisation introduced by the sign selector (SS) and error estimator (EE) blocks. Since the input signal is $\epsilon_d(n) = 0$, at low frequencies the error energy can be made very low by using a high-gain/high-order $H(z)$ and by making the SS and EE blocks as accurate as possible.

The SS block is a crucial component of the loop. Its role is to generate a $t(n)$ vector (composed of N elements ± 1) such that the computed error $\hat{\epsilon}(n)$ is as close to $\epsilon^*(n)$ as the given conditions allow. Specifically, for a relative mismatch between C_1 and C_2

$$\delta = \frac{C_1 - C_2}{C_1 + C_2} \quad (1)$$

it can be shown that the error, to a first-order approximation, is

$$\begin{aligned} \epsilon(n) &\approx \frac{\delta}{2} \hat{\epsilon}(n) \\ &= \frac{\delta}{2} \sum_{k=1}^N t(n, k) \left[2^{k-N} x(n, k) - \sum_{j=1}^{k-1} 2^{j-N} x(n, j) \right] \end{aligned} \quad (2)$$

This expression, even though different in appearance, is equivalent to that found in [3].

The task of the SS block is to choose the signs $t(n, k)$ on the basis of eqn. 2 such that, for given $x(n)$ and $\epsilon^*(n)$, the difference $[\hat{\epsilon}(n) - \epsilon^*(n)]$ is minimised. Since this is affected mainly by the first few most significant bits (MSBs) of the words $x(n)$, $\epsilon^*(n)$, and $t(n)$, both inputs to the SS block can be truncated to (say) 4 bit, and the LSBs of $t(n)$ may be fixed to one value. Hence, the SS block can be realised as a small (4x4x4 bit) ROM which outputs the near-optimum N bit sign vector $t(n)$. The signs $t(n, k)$ are then provided to the DAC to control the switching sequence, and to the EE block which derives $\hat{\epsilon}(n)$ using eqn. 2.

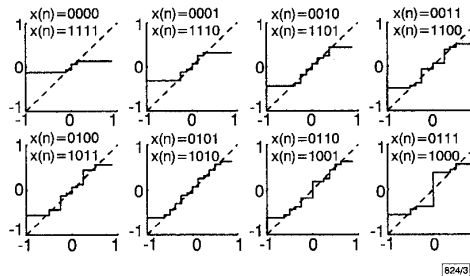


Fig. 3 Optimum transfer characteristics for sign selector (SS) and error estimator (EE) blocks

Under ideal conditions, the cascade of the SS and EE blocks should have a linear unity gain, i.e. $\hat{\epsilon}(n) = \epsilon^*(n)$. This would yield zero DAC error at all frequencies, but unfortunately this is impossible to achieve. Fig. 3 shows the transfer characteristics obtained by choosing the optimum $t(n)$ for each of the 16 possible 4 bit truncated $x(n)$ inputs. Clearly, some inputs (0101, 1010) allow nearly perfect transfer characteristics, while others (0000, 1111) do not.

Note that the scheme of Fig. 2 can be used to shape the error of any physical system which has only a single error source (cf. δ in eqn. 1), and where the formula for the output error is known (cf. eqn. 2). Note also that the principle of the scheme is somewhat similar to that of the mismatch-shaping technique proposed by Schreier for high-linearity multibit flash DACs [4]. However, [4] discusses systems with multiple errors $\delta_1, \delta_2, \dots$ and hence multiple control loops, and each control loop employs a quantiser which is both highly nonlinear and time-variant. Also, Hernandez described a scheme [5] in which the switching sequence in a mismatch-shaped multi-stage DAC was controlled by digital delta-sigma loops.

This Letter did not address several important aspects of the proposed system, such as assuring its stability and preventing idle tones in $y(n)$. This will be discussed in a full-length paper currently being prepared for publication.

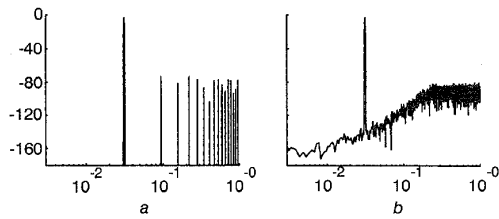


Fig. 4 DAC output spectra without and with mismatch shaping
 a Without mismatch shaping
 b With mismatch shaping

Simulation results: The operation of the system in Fig. 2 was simulated under the following conditions: relative matching accuracy $\delta = 0.1\%$, $H(z) = 1/z - 1 + 0.5z/(z-1)^2 + 0.25z^2/(z-1)^3$, $N = 16$, and the words $\epsilon^*(n)$ and $x(n)$ were truncated to 4 bit when entered into the SS. The sinusoidal input signal had a peak-to-peak amplitude $0.707 V_{ref}$ and a frequency 32 times lower than the Nyquist rate. Fig. 4 compares the output spectra obtained with and without the proposed correction scheme. Without compensation, the harmonics are dominant, and the total harmonic distortion is only ~ -70 dB. With compensation, there are no observable harmonic spurs, and the third-order noise shaping is evident. For an oversampling ratio (OSR) of 10, the inband-noise-to-signal ratio of the corrected system is around -96 dB, corresponding to a 16 bit performance.

© IEE 1998 17 June 1998
 Electronics Letters Online No: 19981121

J. Steensgaard (Department of Information Technology, The Technical University of Denmark, Denmark)

E-mail: jest@it.dtu.dk

U. Moon and G.C. Temes (Department of Electrical and Computer Engineering, ECE Building, Rm 220, Oregon State University, Corvallis, OR 97331, USA)

E-mail: moon@ece.orst.edu, temes@ece.orst.edu

J. Steensgaard: Currently a visitor at the Department of Electrical and Computer Engineering, ECE Building, Rm 220, Oregon State University, Corvallis, OR 97331, USA

References

- SUAREZ, R., GRAY, P., and HODGES, D.: 'All MOSFET charge-redistribution analog-to-digital conversion techniques-Part II', *IEEE J Solid-State Circuits*, 1975, **10**, pp. 379-385
- WEYTEN, L., and AUDENAERT, S.: 'Two-capacitor DAC with compensative switching', *Electron. Lett.*, 1995, **31**, (17), pp. 1435-1436
- ROMBOUTS, P., WEYTEN, L., RAMAN, J., and AUDENAERT, S.: 'Capacitor mismatch compensation for quasi-passive switched-capacitor DAC', *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, 1998, **45**, (1), pp. 68-71
- SCHREIER, R., and ZHANG, B.: 'Noise-shaped multibit D/A converter employing unit elements', *Electron. Lett.*, 1995, **31**, (20), pp. 1712-1713
- HERNANDEZ, L.: 'Binary-weighted D/A converters with mismatch shaping', *Electron. Lett.*, 1997, **33**, (24), pp. 2006-2007

Symmetry conditions of Boolean functions in complex Hadamard transform

S. Rahardja and B.J. Falkowski

A method to identify symmetries in Boolean functions using a complex Hadamard transform is proposed. It is shown that only the half spectrum is needed to detect symmetries in Boolean functions.

Introduction: Two spectral approaches, based on either the Reed-Muller or the Hadamard-Walsh transform, have been applied to the identification of Boolean symmetries [3]. Both of these spectral

approaches used the arithmetic manipulation of subsets of spectral coefficients. In this Letter, the conditions for Boolean symmetries are given for complex Hadamard transforms that are based on the complex Boolean spectra and do not require any manipulation. The analysis is limited to all possible symmetries of degree 2 for any n -variable Boolean function, and the symbols used for different types of symmetries follow the notation from [3].

Property 1: If the basis transform matrix of the complex Hadamard transform is

$$C = \begin{bmatrix} 1 & i \\ -i & -1 \end{bmatrix}$$

then the elements of the matrix are related by

$$C_{(2^n-1-j)k} = i^{-\gamma} \overline{C_{jk}} \quad (1)$$

where 2^n defines the order of the complex Hadamard matrix, $\gamma = n \bmod 4$.

Definition 1: Let $f(\vec{x}_n)$ be a Boolean function of n variables, with $\vec{x}_n = \{x_n, x_{n-1}, \dots, x_1\}$, $x_u \in \{0, 1\}$, $1 \leq u \leq n$. The truth vector \vec{f} can be mapped to an M -coded \vec{F} with encoding $[0 \rightarrow 1 + i]$ and $[1 \rightarrow -1 - i]$.

Theorem 1: Let the encoded truth vector $\vec{F} = [f_0, f_1, \dots, f_k, \dots, f_{2^n-1}]^T$ have complex Hadamard spectra of $\vec{M} = [m_0, m_1, \dots, m_j, \dots, m_{2^n-1}]^T$. Then,

$$m_{2^n-1-j} = \overline{m_j} \exp\left[(1-\gamma)\frac{\pi}{2}i\right] \quad (2)$$

where $\gamma = n \bmod 4$.

Proof: Let $f_k = f_{sk}(1+i)$ and $0 \leq k \leq 2^n-1$ where $f_{sk} \in \{+1, -1\}$ represents the S -coded minterms of the Boolean function [3]. By definition 1, each of the elements in \vec{M} is expressed as $m_j = \sum_{k=0}^{2^n-1} c_{jk} f_k = \sum_{k=0}^{2^n-1} c_{jk} f_{sk}(1+i)$, where the complex Hadamard matrix $C^n = \{c_{jk} = \alpha_{jk} + i\beta_{jk}\}$ and $0 \leq j \leq 2^n-1$. Then,

$$\begin{aligned} m_j &= \sum_{k=0}^{2^n-1} f_{sk}[(\alpha_{jk} - \beta_{jk}) + i(\alpha_{jk} + \beta_{jk})] \\ &= \sum_{k=0}^{2^n-1} f_{sk}(\alpha_{jk} - \beta_{jk}) + i \sum_{k=0}^{2^n-1} f_{sk}(\alpha_{jk} + \beta_{jk}) \end{aligned}$$

and, from property 1,

$$m_{2^n-1-j} = i^{-\gamma} \left[\sum_{k=0}^{2^n-1} f_{sk}(\alpha_{jk} + \beta_{jk}) + i \sum_{k=0}^{2^n-1} f_{sk}(\alpha_{jk} - \beta_{jk}) \right]$$

By separating summation terms, eqn. 2 is proved.

Definition 2: The reverse operator R on either row vector or column vector is defined as reversing the positions of all its elements. For example, if \vec{F} is as defined in definition 1, then $R(\vec{F}) = [f_{2^n-1}, f_{2^n-2}, \dots, f_0]^T$.

Property 2: From theorem 1 and definition 2,

$$R(\overline{M^{(3)}}) = \exp\left[(1-\gamma)\frac{\pi}{2}i\right] \overline{M^{(0)}} \quad (3)$$

and

$$R(\overline{M^{(2)}}) = \exp\left[(1-\gamma)\frac{\pi}{2}i\right] \overline{M^{(1)}} \quad (4)$$

where the conjugate operation on a column vector is defined as converting every element in the column vector to its complex conjugate equivalence. The proof of property 2 is immediate from theorem 1.

Theorem 2: Let an n -variable Boolean function $f(\vec{x}_n)$ possess symmetries of degree 2 in $E\{x_n, x_{n-1}\}$. Then, the complex spectral test for this symmetry is

$$\overline{M^{(0)}} = R \left[\exp\left[(1-\gamma)\frac{\pi}{2}i\right] \overline{M^{(0)}} \right] \quad (5)$$