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A Noise-Shaping Accelerometer Interface Circuit for Two-Chip Implementation

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Abstract *– A proposed third-order noise-shaping accelerometer interface circuit enhances the SNR, compared with the previously presented interface circuits. The solution for the two-chip implementation is described and a novel cross-coupled CDS integrator is proposed. This scheme functions even with the large parasitic capacitances between the sensor and the interface circuit. The op-amp noise is first-order shaped. Dithering circuit is also implemented on the chip, fabricated in AMI 1.6μm CMOS process.*

Keywords *– delta-sigma modulator, accelerometer, sensor interface, CDS, dither*

I. INTRODUCTION

Modern micromachining technology allows the fabrication of mechanical sensors on chip. A successful application is the accelerometer, widely used in automobile air-bag systems. This is basically a capacitive sensor, but its capacitance is quite small. There are several ways to sense the capacitance accurately. Our previous result [1] shows that one can use the sensor as the input capacitor in the delta-sigma loop. The other solution using the delta-sigma loop is based on force feedback [2], [5]. For the accelerometer, force feedback is attractive, since it offers the potential of wide dynamic range [3]. Recently, we introduced a two-chip implementation of a capacitive sensor interface circuit, intended especially for the accelerometer [4]. However, practical circuit implementation including $1/f$ noise and offset voltage reduction was not shown yet.

In Sec. II, we describe the sensor's characteristics. In Sec. III, we review a new noise-shaping structure with higher loop gain and three-level force feedback. In Sec. IV, we show how to solve the problem for two-chip implementation. In Sec. V, a novel fully-differential cross-coupled integrator is described. It allows a large parasitic capacitance at the input of the op-amp with correlated double sampling to reduce $1/f$ noise and cancel offset voltages. A practical way to apply dithering is described in Sec. VI. A fabricated interface chip is described in Sec. VII. Our conclusions are given in Sec. VIII.

II. ACCELEROMETER SENSOR

Fig. 1 shows the model of the accelerometer used in the simulation and design of the interface circuit. It consists of two capacitors with a common center plate.

By detecting the capacitance changes, we can measure the acceleration. The top and bottom plates in Fig. 1 are fixed, but the center plate will move when there is acceleration. This movement creates the capacitance changes. The dynamic characteristic of the sensor can be modeled

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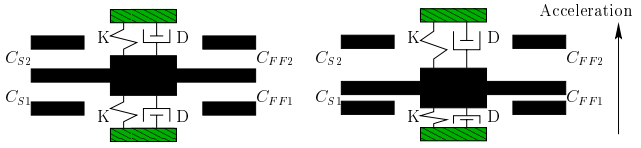


(a) $C_{S1} = C_{S2}$ (b) $C_{S1} > C_{S2}$

Fig. 1. Accelerometer sensor (C_{S1}, C_{S2}:sensor capacitors, C_{FF1}, C_{FF2}:force feedback capacitors)

by

$$H(s) = \frac{x(s)}{\alpha(s)} = \frac{1}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \quad (1)$$

where x is the mass displacement, α is the acceleration, $\omega_n = \sqrt{K/M}$ is the resonant frequency, $Q = \sqrt{KM}/D$ is the quality factor, K is the spring constant, D is the damping factor, and M is the mass of the center plate. The second-order characteristic of Eq. (1) with an additional integrator gives a third-order noise-shaping with proper compensation [4].

With recent micromachining technology, this type of sensor can be fabricated in a small size and has potential use in many applications. However, the necessary detection of small variation of the capacitance is challenging. Typical sensor capacitance is 100 fF, its variation is only ~0.1 fF, and it may have to be detected with a resolution of the order of 1 aF (10^{-18} farads).

The sensor can be modeled as a three-terminal capacitor. This means that a large common-mode signal will appear when the common-node voltage is changed. When the two end-nodes are used to inject a reference voltage, the sensor output will be a single-ended signal with respect to the common node and this results in a large common-mode noise. Cross-coupled fully-differential configuration will solve both problems.

III. THIRD-ORDER STRUCTURE

Fig. 2 shows the proposed structure for the sensor interface circuits [4]. The main departure from earlier structures [2], [5] is the additional integrator in the loop. Eq. (1) gives no noise-shaping for the signal. That means that the SNR is determined by the sensor gain, or its resonance frequency. The integrator is added for additional noise shaping to get a higher SNR at low frequencies, and the op-amp noise, amplified due to the large parasitic capacitance between the chips, is also first-order shaped. A novel three-level force feedback with mismatch shaping enables the use of a simple digital compensator for this high-order noise-shaping structure [4].

There are several advantages to fabricating the sensor and the interface circuits separately. First, one can use this circuit technique when there is no access to micromachining technologies, and commercial sensor must be used. Second, it is likely to provide higher yield, since the micromachining process is still complicated and failure-prone. Third, one can use more advanced process for the interface circuit and use more transistors, because micromachining usually uses older processes. One can also apply this circuit for multiplexed sensors. Once a two-chip solution is obtained, it will be less challenging to generate a single-chip implementation.

To implement the interface circuit separately, we have to solve the problems arising from stray capacitance due to the wiring between sensors and circuits. These are discussed in the next section. A fully-differential cross-coupled integrator with CDS is proposed in Sec. V to solve the problems.

IV. TWO-CHIP IMPLEMENTATION

Even for an on-chip sensor or a surface MEMS sensor, for low-noise op-amps the parasitic input capacitance can be several pF large [5]. For two-chip implementation, it can be 10 ~ 30 pF large. To minimize the problems due to the large parasitic capacitance, the following basic rules must be satisfied:

- The floating terminal of the parasitic capacitor must not be reset to a dc potential in any clock phase;
- No series switch must be placed between the parasitic capacitor and the input terminal of the op-amp;
- The front-end circuit block should not be an amplifier, but an integrator.

Next, the reasons for these rules will be discussed.

A. Rule 1; Offset Sampling

The first rule holds because switching or resetting the large parasitic capacitor creates a large error charge flow since the input potential of the op-amp is not exactly at ground. In Fig. 3(a), the voltage at Ⓐ contains an offset voltage, random noise dominated by the $1/f$ effect at low frequencies, and also some signal due to the finite op-amp gain. After resetting C_p with S_1, this error charge will flow into the feedback capacitor C_f.

B. Rule 2; kTC Charge Noise

The second rule must be satisfied in order to minimize the kTC charge noise caused by the resistance of the switch.

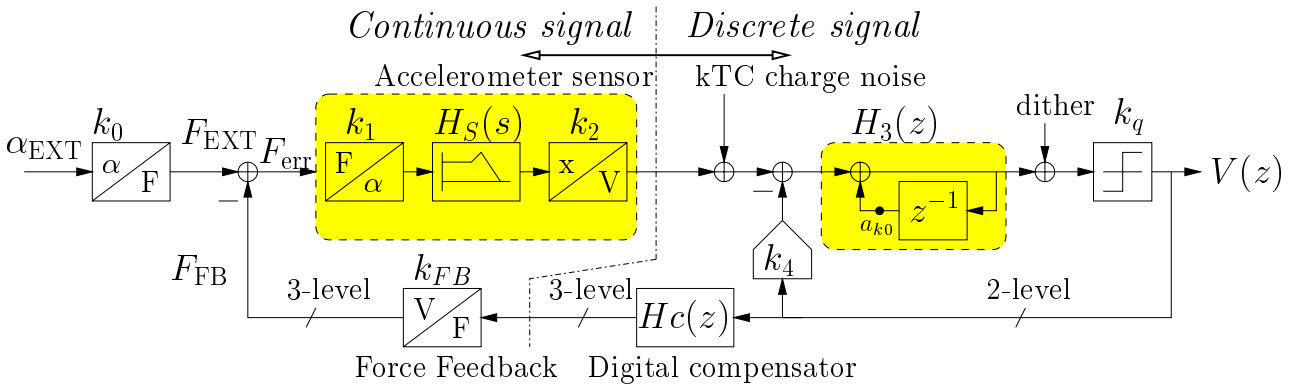


Fig. 2. 3rd order sensor circuit block

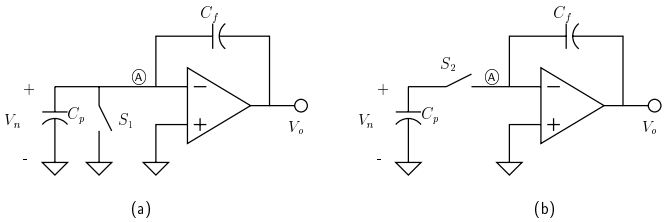


Fig. 3. Problems occurring for SC stages with a parasitic capacitor

In Fig. 3(b), the switch S_2, between the parasitic capacitor C_p and the input terminal, creates a noise voltage with a mean-square value kT/C_p, which leads to an RMS noise charge $\sqrt{kTC_p}$. This is large if C_p is large. For example, an input capacitor $C_{in} = 1$ pF causes 64 $\mu\mathrm{V}_{rms}$ of kT/C noise, but the charge noise from a parasitic capacitor C_p=20 pF, referred back to the input, is as large as 287 $\mu\mathrm{V}_{rms}$, more than 4 times larger than the kT/C noise of the input capacitor. Even for only C_p=2 pF, the input-referred noise due to C_p is 91 $\mu\mathrm{V}_{rms}$, 50 % larger than that due to C_{in}.

The noise is sampled by S_2, and will appear at the output of the op-amp. The bandwidth of this kTC_p charge noise is determined by the op-amp. The power spectral density is given by

$$S^{S/H}(\omega) \propto \frac{kT}{C_p}\left(\frac{(R_{on}+R_{eq})C_p\omega_0}{\alpha+1}\right)\left(\frac{\alpha f_s}{\omega}\right)^2 \qquad (2)$$

where $\alpha = \frac{C_p}{C_f}$, R_{on} is the on-resistance of the switch S_2, R_{eq} is the equivalent resistance for the input-referred op-amp noise, ω_0 is a unity gain frequency of the op-amp, and f_s is a sampling frequency [6]. Eq. (2) indicates that the noise from the parasitic capacitor is directly proportional to the bandwidth of the op-amp and the ratio of two capacitors C_p and C_f if it is switched by S_2 in Fig. 3(b).

C. Rule 3; Op-Amp Noise

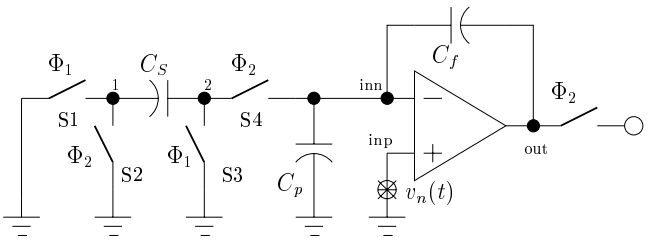
To understand the third rule proposed above, consider the SC circuits shown in Fig. 4. Their noise performance was simulated in HSPICE. The generation of the noise voltage for the op-amp and the post-processing were performed using MATLAB, and the noise source was imported as a piece-wise linear voltage source into HSPICE. The noise changed at least 10 times in each clock period so that it behaved as a continuous-time signal. The op-amp's DC gain was assumed to be 60 dB, and its bandwidth 5 MHz. The clock rate was 1 MHz.

The output noise spectrum and the input-referred noise spectrum for each case are shown in Fig. 5. The parasitic capacitor C_p amplified the op-amp noise in both cases, but due to integrating action, the input-referred noise of the integrator is much smaller than that of the amplifier. Hence, for measurements of low-frequency signal, it is better to use the integrator for the front-end circuit block in the sensor interface circuits.

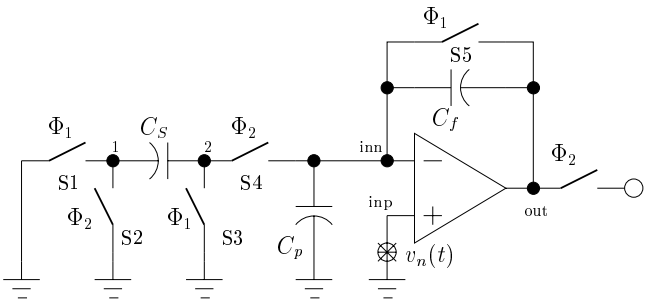
V. FULLY-DIFFERENTIAL CDS INTEGRATOR

A novel CDS circuit is shown in Fig. 6. C_{S1} and C_{S2} are on the sensor chip, which has several switches. The rest of the components are on the interface chip, except for the large parasitic capacitors C_{p1} and C_{p2}. Cross-coupled input modulates the common-mode signal injected from the common-plate node. When the common terminal of the sensor is switched, a large common-mode signal with the small sensor signal is injected into the feedback capacitors C_{f1} and C_{f2}. That large common-mode signal is subtracted during $\Phi 2$ and $\Phi 4$ due to the cross-coupling. At the same time, the differential signal (sensor signal) is doubled.

The basic principle of operation [7] is that if the input and feedback capacitors $C_{S1,S2}$ and $C_{f1,f2}$ are connected to the virtual ground while switches at the input-side terminal of $C_{S1,S2}$ are toggled between V_{in} and ground, then



(a) Integrator



(b) Amplifier

Fig. 4. (a) Integrator, (b) Amplifier

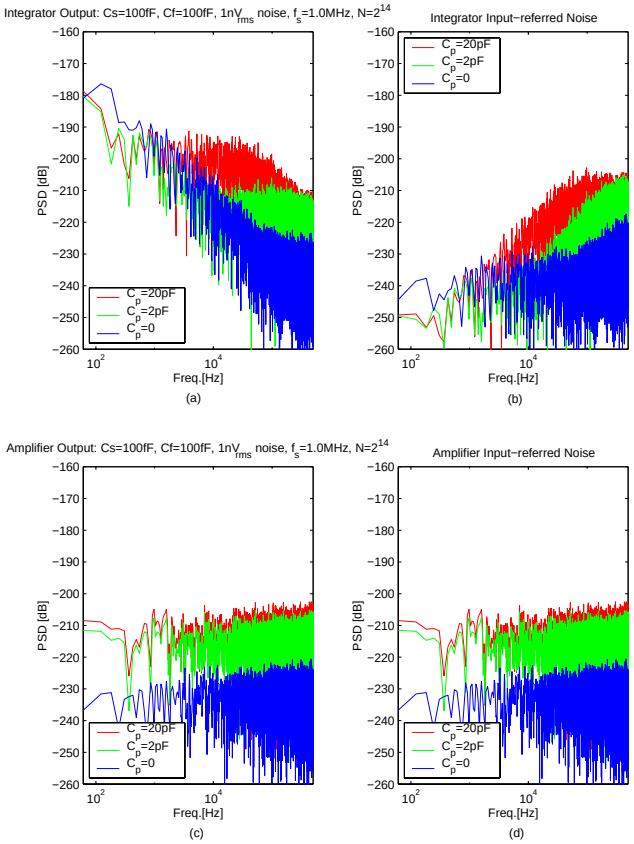


Fig. 5. (a) Output noise of an integrator, (b) Input noise of an integrator, (c) Output noise of an amplifier, (d) Input noise of an amplifier

the magnitude of the charge entering the feedback capacitors $C_{f1,f2}$ will be (to a very good approximation) $C_{S1,S2} \cdot V_{REF}$, independent of the slowly varying components (offset, $1/f$ noise, and signal) of the op-amp input error voltage. If afterwards the feedback capacitors are disconnected, then their charge injection is independent of the input signal and causes only a small constant offset at the output. Thus, the charge integration is nearly ideal.

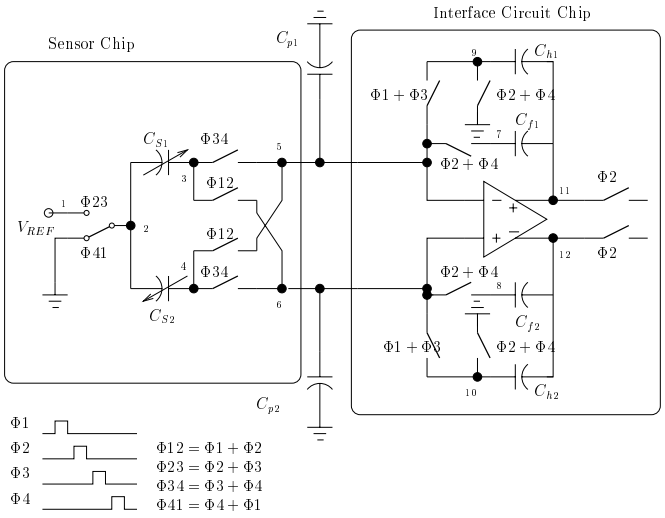


Fig. 6. New CDS fully-differential circuit

Detailed circuit operation is as follows. Before the input switches are toggled between the ground and V_{REF} (from $\Phi 1$ to $\Phi 2$ and from $\Phi 3$ to $\Phi 4$), the input capacitors $C_{S1,S2}$ are reset by the right-hand side switches during $\Phi 1$ and $\Phi 3$. The integrating capacitors $C_{f1,f2}$ are disconnected during $\Phi 1$ and $\Phi 3$, but the holding capacitors $C_{h1,h2}$ hold the previous outputs. When the switches next to $C_{f1,f2,h1,h2}$ are toggled, the right-hand-side switches of the input capacitors remain closed. During this period, the op-amp's input node voltage (due to offset voltage, noise, and finite op-amp gain) is stored in $C_{S1,S2}$. Hence, the sampled charge delivered by $C_{S1,S2}$ to $C_{f1,f2}$ at $\Phi 2$ and/or $\Phi 4$ is not affected by the voltage at the input node.

As described in the previous section Sec. IV, the parasitic capacitance is not reset in the circuit of Fig. 6, and there is no series switch between the parasitic capacitors and the input terminal of the op-amp. The integrator is used to shape the op-amp noise as well.

VI. DITHERING

Since the input signal of the accelerometer is usually at very low frequencies, tone generation may occur in the loop. Dithering signal helps to reduce such tones in the band of the interest.

There are several ways to implement dithering. Thermal noise of the pn junction can be used for generating the dither signal [8]. However, it is better to use a pseudo-random sequence in a digital circuit for testability and repeatability.

Fig. 7 shows the circuit used in the actual interface chip.

$C_{1,2,3,4}$ are used to sample the output of the op-amp and the dither signal. Those two signals are added at the input of the quantizer. The random sequence is controlled by a digital pseudo-random noise code (PNC). It is easily obtained using shift registers. The dither voltage level is determined by the constant voltage V_{dith}. V_{dith} can be supplied by a simple single-ended voltage source. It is modulated by the PNC and added to the signal from the integrator at the quantizer input. The left-hand terminals of the sampling capacitors are tied together to cancel the common-mode voltage.

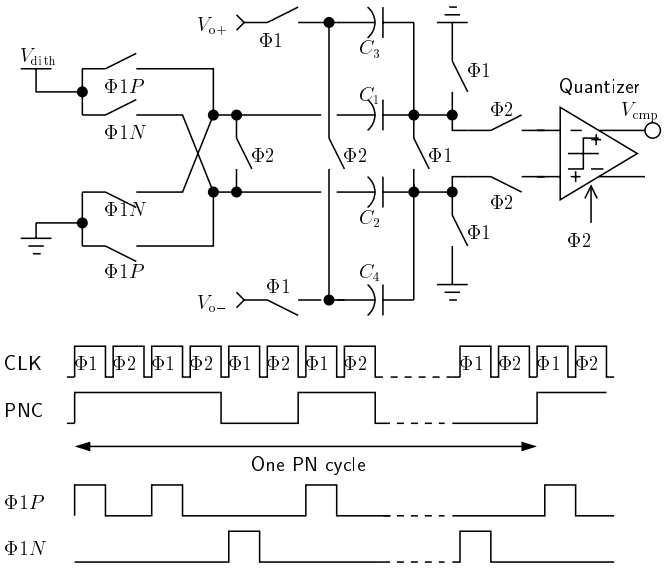


Fig. 7. Dithering circuit

Fig. 8 shows the simulation result using MATLAB. It shows that the SNR is much improved with dithering, especially at small accelerations.

VII. TEST CHIP IMPLEMENTATION

Fig. 9 shows the layout of the interface chip. The chip size is 2.0 x 2.0 mm^2 and was designed for the AMI 1.6 μm CMOS process. It is now under test. Fig. 10 is a layout of the accelerometer sensor chip, fabricated by courtesy of Analog Devices.

VIII. CONCLUSION

A new interface circuit containing a novel fully-differential CDS integrator was proposed. It allows large parasitic capacitors, and is effective in the presence of large common-mode charge as well as common-mode noise.

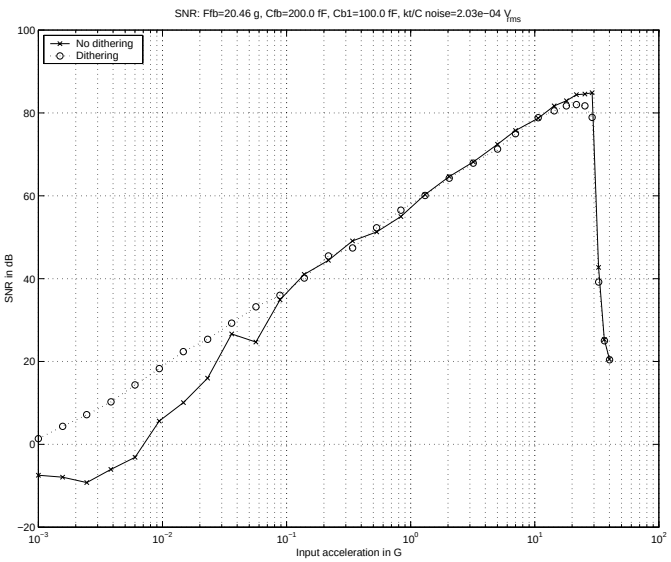


Fig. 8. SNR vs. input acceleration with and without dithering

A practical dither circuit was also shown. Even though the third-order delta-sigma structure helps the noise-shaping, only first-order behavior can be expected in the band of interest. Since the sensor signal is very close to dc, tones will affect the signal-to-noise ratio. Hence, dithering helps to improve the SNR.

ACKNOWLEDGMENTS

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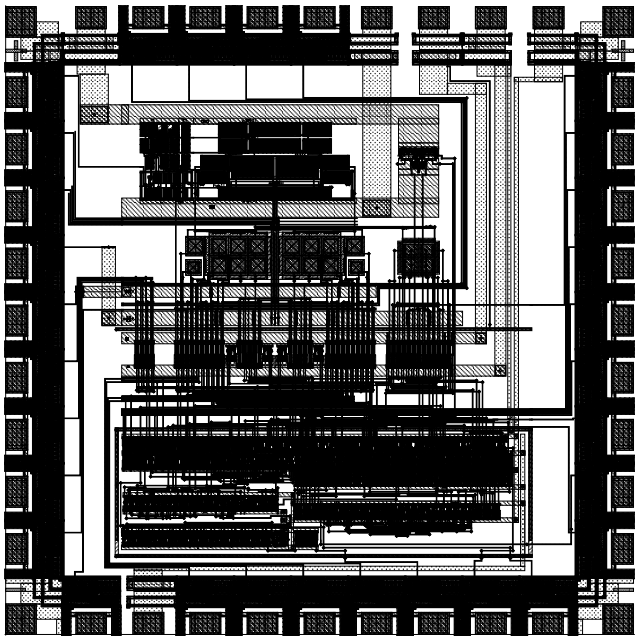

Fig. 9. Interface chip layout (MOSIS AMI 1.6 μm CMOS process: 2.0 x 2.0 mm^2)

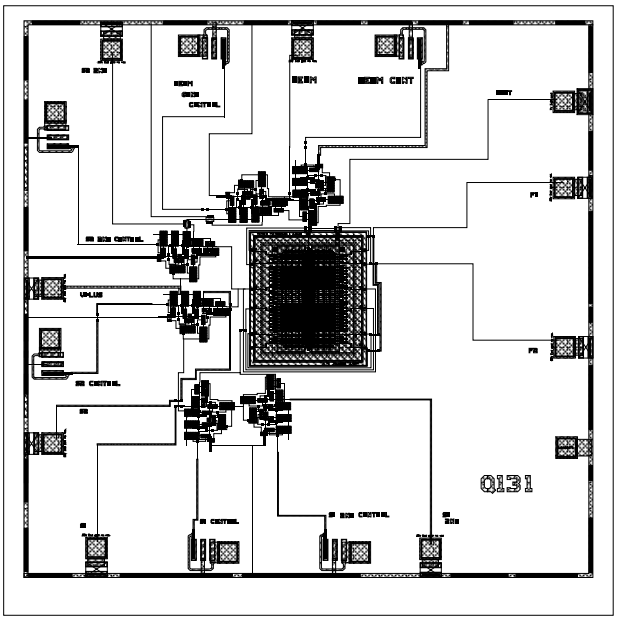

Fig. 10. Sensor chip layout (ADI iMEMS process)

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