IMPROVED ADAPTIVE DIGITAL COMPENSATION FOR CASCADED ΔΣ ADCS

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ABSTRACT

Cascaded delta-sigma (MASH) converters offer a good compromise between high accuracy, robust stability and speed. However, they are very sensitive to analog circuit imperfections. This paper presents an improved adaptive on-line digital compensation of these errors. Behavioral and circuit-level simulations have confirmed an achievable 13-bit performance and 6-MHz bandwidth for the proposed ADC.

1. INTRODUCTION

Cascaded delta-sigma (MASH) converters offer a good compromise between high accuracy, robust stability and speed. However, they are very sensitive to analog circuit imperfections, because they rely on the perfect matching between an analog filter and its digital counterpart.

An effective adaptive digital compensation of these errors was proposed in our previous work [1], [2]. This paper deals with the improvement to this technique, and its application in a very fast (sampling frequency f_S=100-MHz, oversampling ratio OSR=8–16, signal bandwidth f_B=3–6-MHz) and high-accuracy (signal-to-noise ratio SNR=13–15-bit) implementation. Significant improvements were achieved by choosing a tri-level quantizer in the first stage instead of a simple bi-level comparator, by redesigning the interstage coefficients of the MASH ADC structure, by adding a differentiator in front of the adaptation filter, and by carefully choosing the adaptation parameters.

2. IMPROVED 2-0 MASH ADC STRUCTURES

The structure of the cascaded delta-sigma modulator was investigated in order to improve its dynamic range and peak-SNR performances. Based on theoretical and numerical analysis [3], an improved 2-0 MASH structure was found, which is presented in Fig. 1. The factor $m_0 < 1$ keeps the second stage from overloading, and to compensate for this attenuation the digital output v_2 must be scaled by $m_2 = \frac{1}{m_0}$. In this structure, by adjusting β and m_1, an optimal weighting of the input y_{i2} and the output v_{1a} of the first-stage quantizer can be achieved in the second-stage input signal u_{2a}, thereby allowing the largest possible value for m_0 [4]. By using the coefficients shown in Fig. 1, we gained a 6-dB peak-SNR improvement compared with our previous results [2].

Furthermore, the usable input signal range u_1 can be controlled also in the first stage, not only by changing the interstage coefficients. Therefore, by using a tri-level quantizer in the first stage [5], the usable input signal range u_1 was extended, which in turn improved the achievable peak SNR by an additional 6 dB (Fig. 2).

For the selected coefficient values (Fig. 1), the simulation results are presented in Fig. 2 for OSR=16, N_1=1–1.5 bits, N_2=12 bits and ideal analog circuits. The $\frac{kT}{C}$ noise was neglected. This structure has a 12 dB higher peak SNR than the MASH described in our previous work [2].

Since we are aiming for a large-bandwidth and high-resolution ADC, a high (f_S=100-MHz) sampling frequency was chosen, and the modulator will operate at a low oversampling ratio of OSR=8–16. For the second stage, a 10-bit pipelined ADC was chosen. With a sampling capacitor of 7 pF, the $\frac{kT}{C}$-noise floor can be limited to -92 dB (15 bits). The simulated performance is presented in Fig. 3; a peak SNR of 86 dB was obtained for the structure presented in Fig. 1. Due to the analog circuit imperfections, namely the finite DC gain A_{DC}, and relative capacitor accuracy $\Delta = \frac{\Delta C_2}{C_2} - \frac{\Delta C_1}{C_1}$ of the integrators, first-stage quantization noise leakage occurs [2], and the performance drops

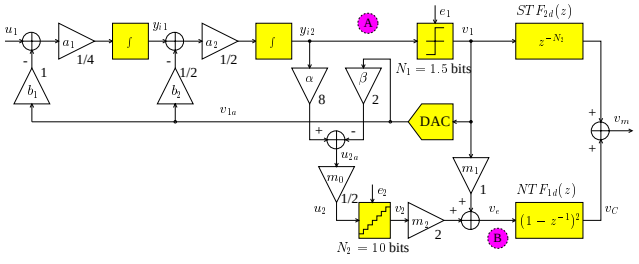

Figure 1: Improved structure of the 2-0 MASH ADC.

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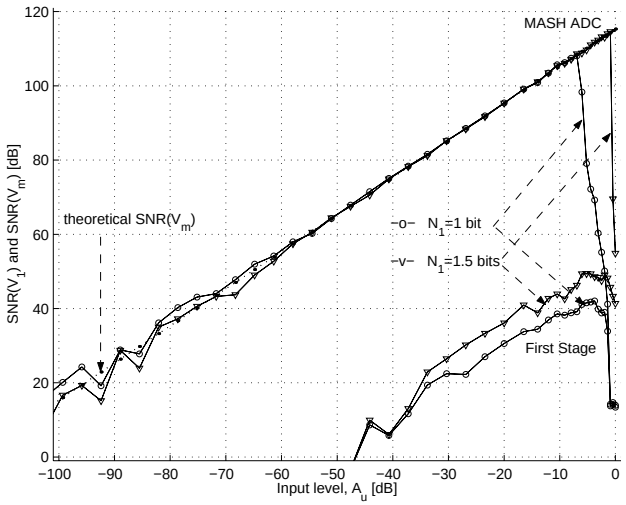

Figure 2: Comparative performance of the ideal 2-0 MASH ADC with bi-level and tri-level quantizer used in the first stage ($OSR = 16$, $N_2 = 12$ bits, and $N\left(\frac{kT}{C}\right) = -\infty$).

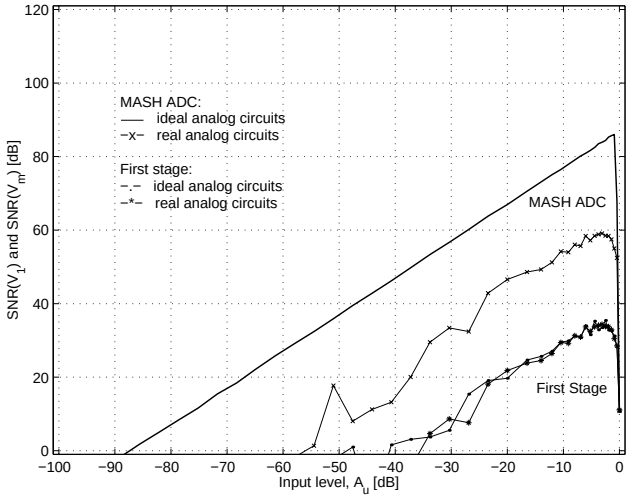

Figure 3: Simulated performance of the ideal and real 2-0 MASH ADC for $A_{DC} = 54$ dB and $\Delta = 0.8\,\%$ ($OSR = 8$, $N_1 = 1.5$ bits, $N_2 = 10$ bits, and $N(\frac{kT}{C}) = -92$ dB).

by more than 25 dB (Fig. 3). However, using our on-line adaptive compensation method (Section 3), these errors can be effectively reduced and 13-bit 6-MHz bandwidth ADC is achievable.

3. IMPROVED ERROR CANCELLATION

An improved MASH structure, which uses an adaptive digital FIR filter $L_C(z)$ to compensate on line for the noise leakage due to the analog circuit imperfections, is shown in Fig. 4. For adaptively adjusting the M coefficients $\overrightarrow{l}$ of the adaptive compensation filter $L_C(z)$, a test signal $test$ is entered into the modulator at its most insensitive node, before the first-stage quantizer, and is adaptively cancelled in the output signal v_m. The coefficients $\overrightarrow{l}$ are updated by the sign-sign-block-least-mean-square (SSBLMS) algorithm which provides a simple circuit-level implementation for $L_C(z)$:

$$\overrightarrow{l}\,[(j+1)K] = \overrightarrow{l}\,[jK] - \gamma\, sign\left\{\sum_{k=0}^{K-1} v_m[jK-k]\, sign\left\{\overrightarrow{test}[jK-k]\right\}\right\}, \quad (1)$$

where K is the block size, j is the current adaptation step and γ is the adaptation coefficient.

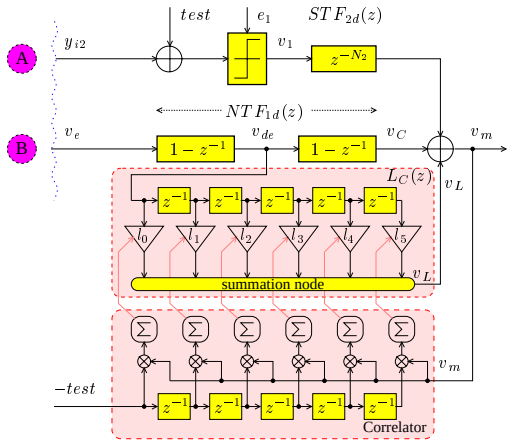

Figure 4: Improved adaptive digital noise-leakage compensation scheme for the proposed 2-0 MASH ADC.

Theoretical analysis and extensive simulations both demonstrated [3] that the test signal should be a white and uniformly distributed noise in order to optimize the adaptation process. A binary pseudo-random sequence was chosen for the simplicity of circuit implementation.

The properties of the noise leakage were studied in order to determine the influence of the analog circuit imperfections on the performance of the cascaded ADC, and to build an effective compensator. Our study indicated that a modification of the previously used adaptive FIR filter [2] can improve the performance. Specifically, a differentiator was added to the compensation structure, which reduced the ripple of the adaptation noise significantly by 6 dB. The modified structure is presented in Fig. 4. Also, by carefully choosing the parameters of the adaptation process, the ripple of the adaptation noise could be further reduced, to the very comfortable value of 1 dB. The performance is illustrated in Figs. 5 and 6. It turns out that the simulated performance of the compensated practical MASH ADC approaches closely that of the ideal MASH ADC.

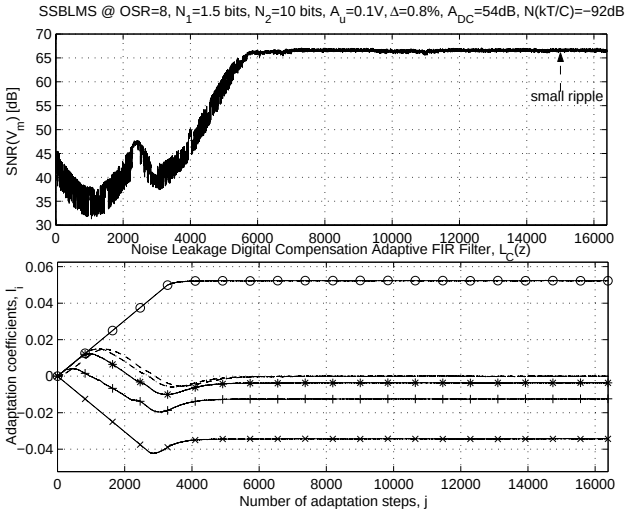

Figure 5: Convergence curves for a compensation process.

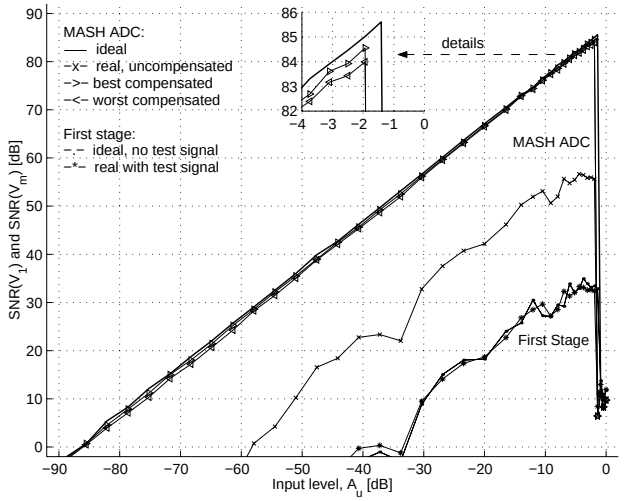

Figure 6: Simulated SNR performance.

4. IMPLEMENTATION

To verify the performance of the proposed 2-0 MASH structure, a chip is being designed in a 0.25-μm 3.3-V digital CMOS process. The circuit implementation offers some special challenges due to the targeted high speed of operation. In the first stage, all blocks are to be operated with a clock frequency of f_S=100 MHz. An existing 10-bit pipelined ADC is used for the second stage. This ADC can be clocked at only 50 MHz, if the technique suggested in [6] is used. At this point, the described circuit-level results are for the first-stage delta-sigma modulator only.

The integrators are realized using correlated-double-sampling techniques [7], which greatly reduce the gain requirements for the operational amplifiers. The first integrator, shown in Fig. 7, uses the same capacitor to implement the coefficients a_1 and b_1, mentioned in Fig. 1. The second integrator has additional capacitors for the implementation of the coefficient b_2=1/2.

The tri-level DAC, also shown in the Fig. 7 as part of the integrator, is based on a structure which solves the linearity issue [8]. During Φ_2, the sampling capacitors are connected to the positive reference, the negative reference, or to each other depending on the state of the digital inputs H, M and L. The circuit maintains its linearity despite mismatches in the sampling capacitors, which are translated into gain errors, and despite any asymmetries between the voltage references and the middle level, which are corrected by common-mode feedback operation.

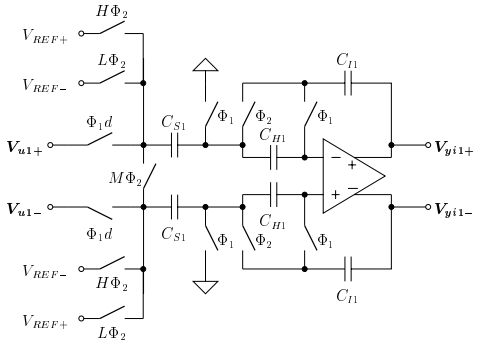

Figure 7: First integrator for the first-stage modulator.

The opamps use a single-stage telescopic cascode structure for high speed, good phase margin, and low power consumption. Tab. 1 summarizes the achieved results. The poor DC gain obtained is effectively doubled by the correlated-double-sampling action of the integrators, and other finite-gain effects will be corrected by the adaptive error cancellation algorithm.

The comparator, based on [9], uses a current comparator driven by a voltage-to-current conversion stage (Fig. 8). The comparator uses additional inputs with smaller transconductance for the definition of the threshold voltages and test signal. The current comparator itself is composed of a source

Parameter	Opamp 1	Opamp 2	Units
DC gain	55.3	59.9	dB
Dominant pole	631.1	467.3	kHz
Unity-gain frequency	387.1	462.1	MHz
Non-dominant pole	6.42	3.94	GHz
Phase margin	95.3	96.3	degrees
Slew rate	520	398	V/μs
Diff. output swing	1.149	1.098	V
Load capacitance	20	3.6	pF
Power consumption	26.4	3.3	mW

Table 1: Parameters of the opamps used in the integrators.

follower operating in class AB, for low input impedance, and an inverter providing positive feedback. This combination results in considerable speed improvement. The tri-level quantizer is built with two of such comparators and a decoder providing the digital lines H, M and L.

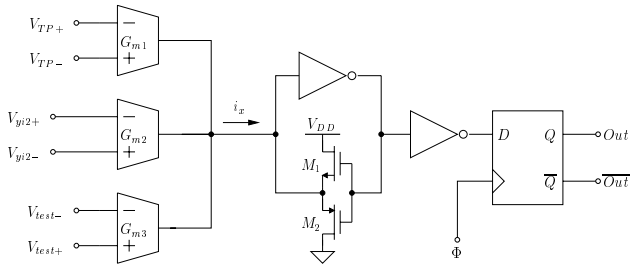

Figure 8: Comparator used for the first-stage modulator.

The first stage was simulated at full transistor level. Fig. 9 shows a 1024 point FFT obtained from the output bitstream, and verifies the proper operation of the first stage at the desired frequencies. The first-stage power consumption will be about 30 mW.

The transistor-level design of the whole MASH ADC is still in progress. We hope to provide the actual chip area and power consumption, as well as experimental data about the performance, at the time of the presentation.

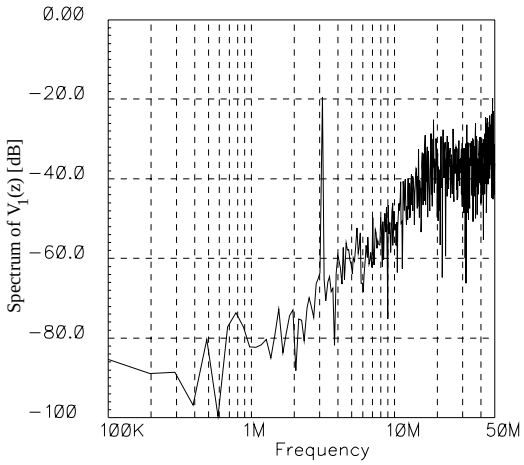

Figure 9: Output spectrum for the first-stage modulator.

5. CONCLUSIONS

The architecture and the adaptive correction algorithm of the 2-0 MASH ADC proposed by us earlier [2], were studied and improved. Using the improved architecture and adaptive digital on-line compensation method, a 13-bit performance and 6-MHz bandwidth ADC appears to be feasible. Such a converter will be faster than any previous high-accuracy ADC, as demonstrated in Fig. 10.

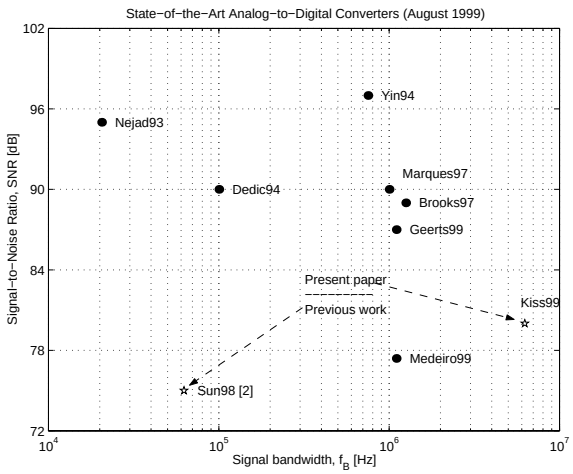

Figure 10: State-of-the-art ADCs (August 1999).

6. REFERENCES

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