A NOISE-SHAPING ACCELEROMETER INTERFACE CIRCUIT FOR TWO-CHIP IMPLEMENTATION

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ABSTRACT

This paper introduces a new architecture for sensor interface circuits using a delta-sigma modulator. The three-level force feedback allows the use of a digital compensator to stabilize the loop. A 3rd-order delta-sigma structure shapes the opamp noise and allows two-chip implementation with high loop gain at low frequencies.

1. INTRODUCTION

Modern micromachining technology allows the fabrication of mechanical sensors on chip. A successful application is the accelerometer, widely used in automobile air-bag systems. This is basically a capacitive sensor, but its capacitance is quite small. There are several ways to sense the capacitance accurately. Our previous result [1] shows that one can use the sensor as the input capacitor in the delta-sigma loop. The other solution using the delta-sigma loop is based on force feedback [2, 3]. For the accelerometer, force feedback is attractive, since it offers the potential of wide dynamic range [4].

In this paper, we introduce a two-chip implementation of a capacitive sensor interface circuit, intended especially for the accelerometer. There are several advantages to fabricating the circuits separately. First, one can use this circuit technique when there is no access to micromachining technologies, and commercial sensor must be used. Second, it is likely to provide higher yield since the micromachining process is still complicated and failure-prone. Third, one can use more advanced process for the interface circuit and use more transistors, because micromachining usually uses older processes. One can also apply this circuit for multiplexed sensors. Once a two-chip solution is obtained, it will be less challenging to generate a single-chip implementation.

To implement the interface circuit separately, we have to solve the problems arising from stray capacitance due to the wiring between sensors and circuits: 1) large kTC charges, 2) large gain for the opamp noise. A cross-coupled integrator is proposed to solve the problems. Also using a higher-order delta-sigma loop increases the loop gain and reduces nonlinearity.

In Sec.2, we describe the sensor characteristics. In Sec.3, we propose a new noise-shaping structure with higher loop gain and three-level force feedback. In Sec.4, we show how the noise from the opamp will be shaped by the additional integrator. The simulation of the additional stage with compensator is described in Sec.5. Our conclusions are given in Sec.6.

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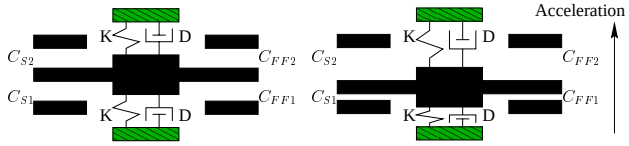
2. ACCELEROMETER SENSOR

Fig. 1 shows the model of the accelerometer used in the simulation and design of the interface circuit. It consists of two capacitors with a common center plate.



(a) $C_{S1} = C_{S2}$ (b) $C_{S1} > C_{S2}$

Figure 1: Accelerometer Sensor (C_{S1}, C_{S2}:Sensor capacitors, C_{FF1}, C_{FF2}:Force feedback capacitors)

By detecting the capacitance changes, we can measure the acceleration. The top and bottom plates in Fig. 1 are fixed, but the center plate will move when there is acceleration. This movement creates the capacitance changes. The dynamic characteristic of the sensor can be modeled by Eq.(1):

$$H(s) = \frac{x(s)}{\alpha(s)} = \frac{1}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \tag{1}$$

where x is the mass displacement, α is the acceleration, $\omega_n = \sqrt{K/M}$ is the resonant frequency, $Q = \sqrt{KM}/D$ is the quality factor, K is the spring constant, D is the damping factor, and M is the mass of the center plate.

With recent micromachining technology, this type of sensor can be fabricated in a small size and has a potential use in many applications. However, the necessary detection of small variation of the capacitance is challenging. Typical sensor capacitance is 100 fF, its variation is only ∼0.1 fF, and it may have to be detected with a resolution of the order of 1 aF (10^{-18} farads).

3. THIRD-ORDER STRUCTURE

Fig. 2 shows the proposed structure for the sensor interface circuits. An integrator is added for additional noise shaping to get a higher SNR at low frequencies, and the opamp noise, amplified due to the large parasitic capacitance between the chips, is also first-order shaped, as discussed in Sec.4 below. Extra compensation is needed, because the sensor itself has the second-order

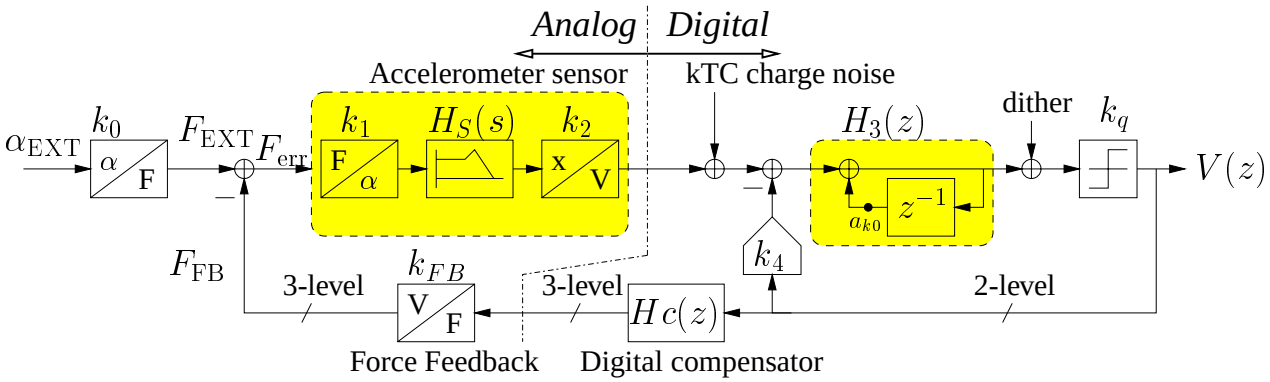


Figure 2: 3rd order sensor circuit block

characteristic as given in Eq.(1), and the system would be unstable without a compensator due to the excessive loop phase shift. One possible solution is to insert an analog compensator before the quantizer [3]. This implementation is not suitable for the third-order structure, because the effect of the last stage will be canceled by the local loop. Hence, the position of the compensator was chosen as shown in Fig. 2. Now the input of the compensator is a digital signal, and it can be realized as a simple digital differentiator with a transfer function $(1 - z^{-1})$.

Fig. 3 shows the root loci and the magnitude responses of the quantization noise transfer function for various quantizer gains. As the root loci verify, the digital compensator stabilizes the loop for all quantizer gains values.

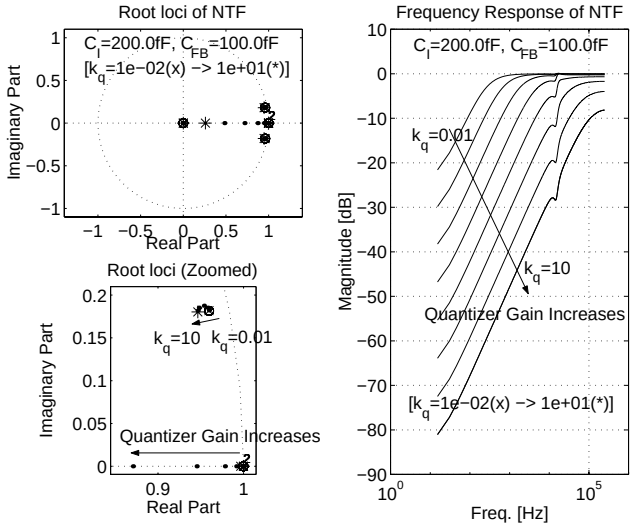


Figure 3: Root locus and NTF

3.1. Circuit realization

Fig. 4 shows the proposed circuits. The first stage is on the sensor chip and the second stage is on the interface circuit chip.

At the input stage of the interface chip, an integrator is used, instead of an amplifier as in [3]. This is because here we have amplified opamp noise, since there are large parasitic capacitances.

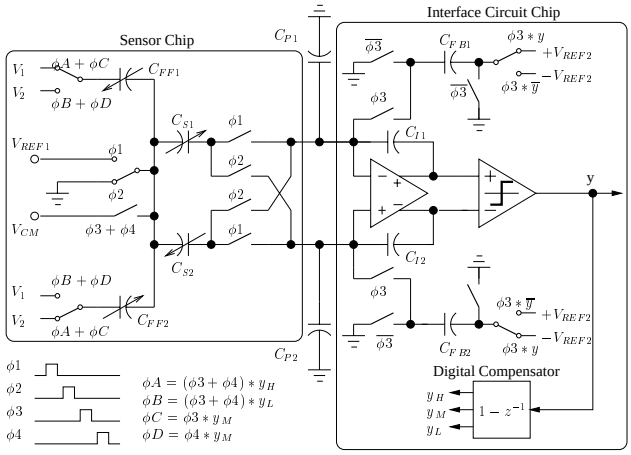


Figure 4: The two-chip accelerometer

Due to the input integration, the input-referred opamp noise will be shaped in the proposed circuit, as discussed later in Sec.4. The interstage nodes are not switched to the ground, and this is a major difference from ordinary integrators. Since these nodes are not switched, the kTC charge noise from the large parasitic capacitances does not enter the signal. The sensor capacitors are switched in a cross-coupled connection. This scheme doubles the amplitude of the sensor signals, and also reduces the large common-mode signal.

C_{FB1} and C_{FB2} provide two-level electrical feedback from the quantizer to the integrating stage. The digital compensator creates a zero to stabilize the loop and provides a three-level output since the quantizer is a two-level one. The three-level force feedback is applied to the sensor capacitors. Unlike the complex analog compensator needed in [3], a simple digital compensator is adequate to stabilize the system. The challenge here is the three-level feedback signal generated from the output of the digital compensator. This three-level signal has to be very accurate and highly linear.

3.2. Three level force feedback

Fig. 5 shows the proposed force-feedback arrangement. V_1 and V_2 are the voltages at the top plate and the bottom plate, respec-

tively. V_{cm} is the center plate voltage. d_1 and d_2 are the distances between the plates of the capacitive sensor, C_{S1} and C_{S2}, respectively. Here $d_1 + d_2 = \text{constant}$, because the outer plates of the sensor capacitor do not move. Typical values of d_1 and d_2 are around 1 μm. x is the displacement due to the acceleration.

There is nonlinearity in the force feedback in terms of the mismatch between d_1 and d_2, and the displacement x. This nonlinearity problem can be solved using a time-averaged force-feedback scheme during the $\phi 3$ and $\phi 4$ phases as shown in Figs. 4 and 5.

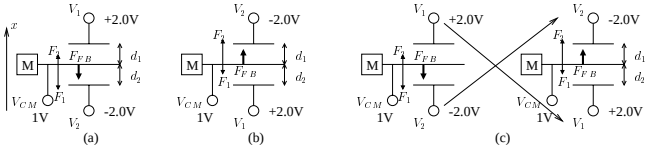


Figure 5: Four-phase force feedback scheme: (a) y_H=1, (b) y_L=1, (c) y_M=1

In Figs. 5(a), let the potential of the center plate be 1 volt. If $d_1 < d_2$ after applying acceleration, the top plate will be connected to $+2.0$ volts, and the bottom plate to -2.0 volts during both $\phi 3$ and $\phi 4$ phases for moving the center plate in the same direction. This creates higher electric field in the bottom capacitor, and pulls down the center plate towards the middle.

If the center plate moves down and it causes $d_1 > d_2$ in Fig. 5(b), the voltages of the outer plates will be reversed, causing the center plate to move up.

If the digital compensator's output is zero ($y_M = 1$), the force feedback is averaged in time using the $\phi 3$ and $\phi 4$ phases. This will be done by applying the force feedback in opposite direction during $\phi 3$ and $\phi 4$. This approach is similar to that proposed for a three-level DAC in [5].

Hence, the feedback force F_{FB} has three levels, given by

$$F_{FB}=\begin{cases} F_{FB+} = -\frac{\epsilon A}{2}\left[\left(\frac{V_1-V_{cm}}{d_1+x}\right)^2-\left(\frac{V_{cm}-V_2}{d_2-x}\right)^2\right] & \text{if } y_H{=}1 \\ (F_{FB+}+F_{FB-})/2 & \text{if } y_M{=}1 \\ F_{FB-} = -\frac{\epsilon A}{2}\left[\left(\frac{V_{cm}-V_2}{d_1+x}\right)^2-\left(\frac{V_1-V_{cm}}{d_2-x}\right)^2\right] & \text{if } y_L{=}1 \end{cases} \quad (2)$$

where y_H, y_M, and y_L are the outputs of the digital compensator. The signal y_H is activated when the compensator output is $+2$, y_M is for 0, and y_L is for -2, since the digital compensator $1 - z^{-1}$ outputs are $+2, 0, -2$. The voltages used for the outer plates, V_1 and V_2, do not need to have exactly the same absolute values.

Table 1 shows how to select the three-level force feedback during the $\phi 3$ and $\phi 4$ phases. The sign "$+$" or "$-$" shows the direction of the force feedback. First-order mismatch shaping can be expected when $\phi 3$ and $\phi 4$ are chosen alternatively, as indicated in Table 1. This is a significant advantage for the three-level DAC because it assures high linearity.

4. NOISE LIMITATIONS

4.1. Amplifier noise

Using an amplifier after the sensor as in [3], correlated double-sampling may be used to cancel the kT/C noise from the sensor capacitor, but the opamp noise will be dominant when there is a large parasitic capacitance, as is the case for the two-chip implementation.

Table 1: Force-feedback direction

Comp. output	$\phi 3$	$\phi 4$	
$y_H = 1$	$+$	$+$	
$y_L = 1$	$-$	$-$	
$y_M = 1$	$+$	$-$	alternated
	$-$	$+$	

The amplifier noise gain H_n from the noninverting input node to the output node (Fig. 6) is

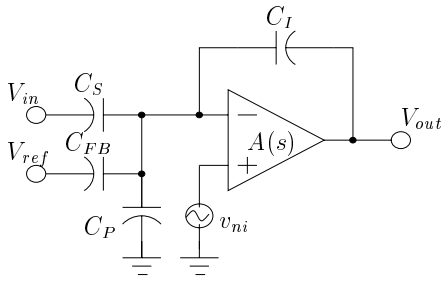


Figure 6: Noise gain equivalent circuit

$$H_n(s) = \frac{V_{out}(s)}{V_{ni}(s)} = \frac{A(s)}{1 + A(s)\dfrac{C_I}{C_S + C_{FB} + C_P + C_I}} \quad (3)$$

where $A(s)$ is the opamp's voltage gain transfer function, V_{ni} is the input-referred opamp noise, C_S is the sensor capacitance, C_{FB} is the feedback capacitance from the quantizer, C_P is the parasitic capacitance at the input node of the opamp, and C_I is the feedback capacitance of the opamp.

The noise transfer function can be approximated by

$$|H_n(\omega)| \approx \left.\frac{C_S + C_{FB} + C_P + C_I}{C_I}\right|_{\omega=\text{low frequency}}. \quad (4)$$

As Eq.(4) shows, the opamp noise is amplified more when the parasitic capacitor C_P is large. The output noise spectrum of the opamp is flat in a wide frequency range, and is band-limited by the unity-gain frequency of the opamp.

4.2. Integrator noise

In an integrator, when the input-referred noise is calculated, the spectrum of the amplified opamp noise is shaped because of the integration. Even though there is large output noise due to the parasitic capacitances, the shaped noise level will be low at low frequencies. This is the advantage of using the integrator at the front end of the interface circuit. Also, the integrator can be used as the additional noise-shaping stage of the delta-sigma interface circuit.

In addition to the opamp noise, which is shaped by the integrator, there is also kT/C noise from the sensor, which remains

unshaped. This seems to be a disadvantage because the sensor capacitor is quite small. But when we compare the noise levels of the amplifier and the integrator, it should be noted that the opamp noise is larger than the kT/C noise and, in our circuit, it will be shaped in the integrator. The parasitic capacitor is *not* switched, and hence there is no kTC charge noise from the parasitic capacitors.

The noise gain from the *sensor* to the output in Fig. 6 is given by

$$H_n(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{\dfrac{C_S \cdot A(s)}{C_S + C_{FB} + C_P + C_I}}{1 + \dfrac{C_I \cdot A(s)}{C_S + C_{FB} + C_P + C_I}}$$

$$|H_n(\omega)| \approx \left. \frac{C_S}{C_I} \right|_{\omega = \text{low frequency}} . \qquad (5)$$

The kT/C noise from the sensor will be amplified as shown in Eq.(5), but it is independent of the parasitic capacitance.

4.3. Comparison of input-referred noises

Following [3], it will be assumed that the input-referred noise and the unity-gain frequency of the opamp are 4.5 nV/$\sqrt{\text{Hz}}$ and 91 MHz, respectively, and the parasitic capacitance C_P is 1.7 pF for the one-chip implementation. Assume the nominal sensor capacitance C_S is 100 fF, the integrating capacitor C_I is 200 fF, the electrical feedback capacitor C_{FB} is 100 fF. Also, the clock frequency is 500 kHz and the band of interest is DC–100 Hz, i.e. the oversampling ratio is 2500. The computed values of the input-referred noises for these parameters are given in Table 2.

Table 2: Input-referred rms noise [μV_{rms}]

Parasitic Cap.	Amplifier 1.7pF	Integrator 1.7pF	Integrator 20pF
Sensor kT/C	cancelled	8.14	8.14
opamp	22.60	1.42	13.79
Total	22.60	8.26	16.01

Even if the parasitic capacitor is as large as 20 pF due to the two-chip structure, the total input-referred noise of the integrator is smaller than that of the amplifier on chip. Also, due to additional shaping at low frequencies, the circuit topology of Fig. 4 allows an improved SNR for two-chip implementation.

5. SIMULATION RESULTS

The proposed two-chip system was simulated using MATLAB under the conditions ω_n=15 kHz and $Q = 4$, with a sine-wave acceleration input 5 G (49.05 m/sec^2) peak. Due to the additional stage, it provided good noise shaping at lower frequencies and hence a high SNR.

The sensor structure is based on the lateral fringe capacitors with small mismatch. According to [3], the mismatch is about 0.02%. We also assumed a 0.02% mismatch in the sensor capacitors. The simulation result is shown in Fig. 7. There is a dc component due to mismatch, but no visible harmonics.

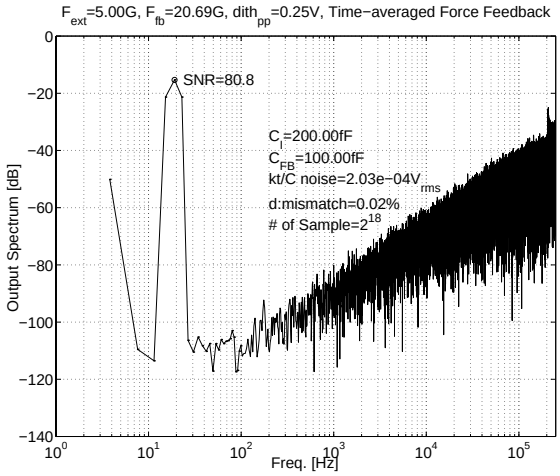


Figure 7: Output spectrum with sine-wave input, a 0.02% mismatch between sensors

6. CONCLUSIONS

A two-chip implementation was proposed for a MEMs accelerometer. The first stage of the sensor interface circuits is an integrator, which is preferable to an amplifier from a noise point of view. The spectrum of the amplified opamp noise due to the parasitic capacitors is then shaped. The additional integrator increases the loop gain and reduces the harmonics. To make the loop stable, a new architecture was chosen for the delta-sigma modulator with digital compensation and three-level force feedback. This interface circuit technique is applicable not only to accelerometers but also to capacitive sensors requiring two-chip implementations.

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7. REFERENCES

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