A 1.4-V 10-bit 25-MS/s Pipelined ADC Using Opamp-Reset Switching Technique

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***Abstract*—A low-voltage opamp-reset switching technique (ORST) that does not use clock boosting, bootstrapping, switched-opamp (SO), or threshold voltage scaling is presented. This technique greatly reduces device reliability issues. Unlike the SO technique, the opamps stay active for all clock phases and, therefore, the ORST is suitable for high-speed applications. This new switching technique is applied to the design of a 10-bit 25–MS/s pipelined analog-to-digital converter (ADC). The prototype ADC was fabricated in a 0.35-μm CMOS process and demonstrates 55-dB signal-to-noise ratio, 55-dB spurious-free dynamic range, and 48–dB signal-to-noise-plus-distortion ratio performance with a 1.4-V power supply. The total power consumption is 21 mW. The ADC's minimum operating power supply is 1.3 V ($|V_{\mathrm{TH,P}}| = 0.9$ V) and the maximum operating frequency is 32 MS/s. The ORST is fully compatible with future low-voltage submicron CMOS processes.**

***Index Terms*—Analog-to-digital converter (ADC), low voltage, opamp-reset switching technique (ORST), pipeline.**

I. Introduction

THE continued downscaling of transistor dimensions in submicron CMOS technology is driven by the need for increased speed and integration density in the state-of-the-art digital IC systems. As the supply voltages are necessarily scaled proportional to the transistor dimensions, the power dissipation of digital circuits is also reduced. While this trend is mostly welcomed by digital systems, many great low-voltage *analog* design challenges lie ahead. Because analog circuits are routinely integrated with digital blocks in most digital signal processors today (e.g., data converters, filters, etc.), it is highly desirable that traditional analog functions migrate easily to digital CMOS processes. This brings renewed attention to the difficult analog IC design challenges ahead.

One of the key limitations of future CMOS technologies remains the restricted supply voltage, limited primarily by the thin gate oxide that is prone to voltage stress (reliability) and breakdown. One class of circuits strongly affected by this trend is switched-capacitor (SC) circuits, used in many practical analog signal processing applications including a majority of CMOS data converters. The fundamental limitation on the operation of a floating switch in SC circuits arises when the supply voltage becomes about same as or less than the sum of the absolute values of the pMOS and nMOS threshold voltages.

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There are several well-known solutions to bypass this floating-switch problem. These approaches include: 1) the clock boosting schemes (e.g., $2V_{\mathrm{DD}}$ clock signal) [1] which cannot be used in submicron low-voltage CMOS processes as the gate oxide can only tolerate the technology's maximum voltage V_{DD}; 2) the use of scaled/lower threshold transistors [2] which are not always scalable to very low voltage supplies as they could suffer from an unacceptable amount of leakage current (i.e., the switch may not fully turn off); 3) the use of bootstrapped clocking [3], [4] which has added loading and possible reliability issues; and 4) the switched-opamp (SO) technique [5] which is fully compatible with low-voltage submicron CMOS processes but the operating speed is limited due to slow transients from the opamp being switched off and on. Although higher speed applications have been attempted [6], speed/accuracy remains limited. In this brief, the opamp-reset switching technique (ORST) topology is proposed for low-voltage operation. A 10-bit 25-MS/s pipelined analog-to-digital converter (ADC) prototype IC has been implemented using this technique. The reset-opamp concept first appeared in [7] and a $\Delta\Sigma$ modulator design example using reset-opamp integrators was demonstrated in [8]. In this work, the ORST is applied to a video-rate pipelined ADC design [9].

The implementation details of the low-voltage ADC design incorporating ORST are described in Section II, followed by the prototype IC measurement results in Section III and concluding remarks in Section IV.

II. Low-Voltage ADC Design

The ADC architecture is a 10-bit 1.5-bit/stage pipelined ADC. The ADC consists of a front-end low-voltage input buffering circuit followed by eight identical stages, each of which is composed of a three-level ADC and a multiplying DAC (MDAC) in which the three-level sub-DAC and the residue amplifier operations are merged. The last/ninth stage is a true 2-bit ADC (four levels). In the prototype IC implementation, the proposed ORST is applied to the input buffering circuit as well as the MDACs.

There are several reasons for choosing a 1.5-bit/stage architecture for the low-voltage ADC design. In the MDAC with the ORST, the opamp is in the unity-gain reset mode during one of the clock phases. It is desirable that the feedback factors during the amplification phase and the reset phase remain comparable to maintain similar settling dynamics. If the feedback factors are drastically different, the opamp would have to be overcompensated to cover a wide range of loop bandwidths. The MDACs with a gain of two proved to be a simpler choice in this regard. Another reason for choosing the 1.5-bit/stage architecture

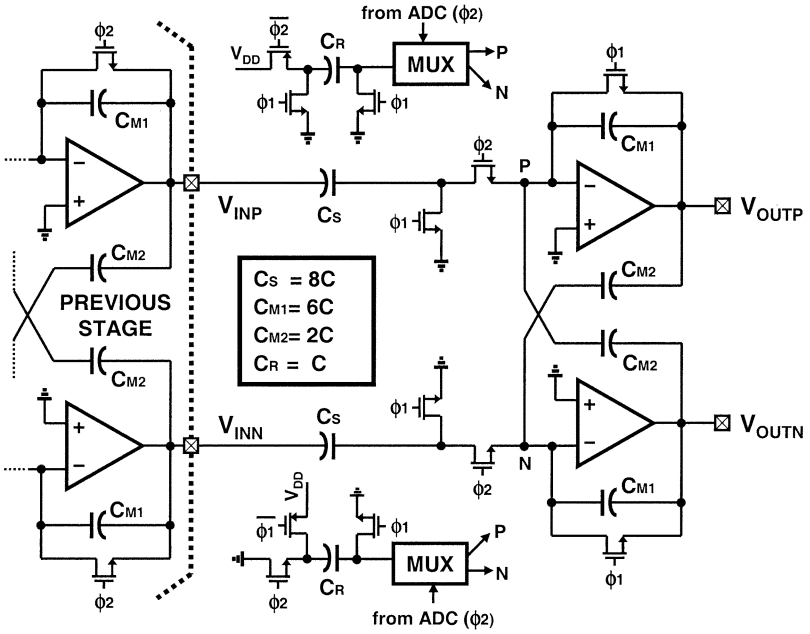

Fig. 1. Full schematic of the proposed low-voltage MDAC.

was that under low-voltage conditions, the reference range is significantly reduced compared to the high-voltage ADCs. The same amount of offset error would be much more crucial in low-voltage design. For this reason, the digital correction/redundancy range needed to be maximized to relax the comparator and opamp offset accuracy requirements.

A. Low-Voltage MDAC

The full schematic of the proposed MDAC is shown in Fig. 1. A pseudodifferential architecture, which has two single-ended opamps working in parallel, is employed. In this design, the ADC uses a 1.4-V supply voltage. To avoid the use of floating switches, the reference voltages $V_{\rm REFP}$ and $V_{\rm REFN}$ are derived from the same voltage potential as the supply rail. To highlight this voltage potential, they are denoted as $V_{\rm DD}$ and GND in the schematic. In the actual IC implementation, these reference voltages represent nodes that are connected separately to a set of quiet voltage references. During the sampling phase ϕ_1, the opamp is placed in the unity-gain reset configuration while C_S samples the previous stage's (sourcing opamp) output. The capacitors C_{M1} and C_{M2} are shorted during this phase. The operation of these capacitors as common-mode feedback (CMFB) will be described in the discussion of the amplification phase that will follow. Due to low-voltage operation, $\pm V_{\rm ref}$ sampling cannot be incorporated into the signal path as the conventional *capacitor flip-over* architecture [10]. Therefore, extra capacitors C_R are added to provide the reference injection. Since all switches are to be connected to either $V_{\rm DD}$ or GND, the desired reference voltage, which is less than the $V_{\rm DD}$ level, is generated by a capacitor ratio. A capacitor ratio of 8:1 is used in this design. This effectively provides the $\pm V_{\rm REF}/4$ reference for the full-scale signal range that is $V_{\rm DD}$ peak-to-peak differential. During the amplification phase ϕ_2, C_R is connected to either node P or N, depending on the sub-ADC decision. The previous, sourcing stage provides the reset level during this phase. If the pseudodifferential architecture is employed without an effective CMFB circuit (C_{M1} and C_{M2} as shown), any common-mode voltage errors entering the cascaded stages would accumulate with multiplication as these errors are multiplied by the same $2\times$ gain of the MDAC. This is because the pseudodifferential configuration inherently does a single-ended operation, resulting in a common-mode gain that is the same as the differential gain. Building a traditional CMFB circuit to alleviate this common-mode accumulation problem under such low voltage headroom while using no floating switches is a challenging task. Such CMFB designs result in relatively inefficient realizations, taking up an unwanted amount of chip area and power consumption. In this work, a traditional CMFB circuit is avoided by introducing a mild amount of positive feedback with C_{M2}. This configuration realizes the required differential gain of $A_{\rm DIFF} = 2$ while allowing a common-mode gain of $A_{\rm CM} = 1$. The common-mode errors now stay unchanged without experiencing the $2\times$ multiplication at each MDAC stage. Thus, the common mode is controlled and retained throughout the stages without the addition of complex CMFB circuitry.

The opamp used in this work is a differential input and single-ended output two-stage Miller-compensated amplifier. The input stage is a modified folded-cascode with a pMOS input pair for high open-loop gain. The second stage consists of an nMOS common-source output stage to achieve high signal swing. The input of the opamp is set to 0.25 V such that when the opamp is configured as a unity-gain buffer during ϕ_1, the nMOS devices in the opamp's output stage will not go out of the saturation region. The 0.25 V is low enough to keep the feedback switches free of the floating-switch overdrive problem.

B. Input Buffering Circuit

Another major challenge in the low-voltage ADC design is to sample/transfer the input signal quickly and accurately from sources external to the ADC during one clock phase and the reset signal during the other phase. One such circuit exists in the context of the SO technique [11]. Fig. 2 shows the modified

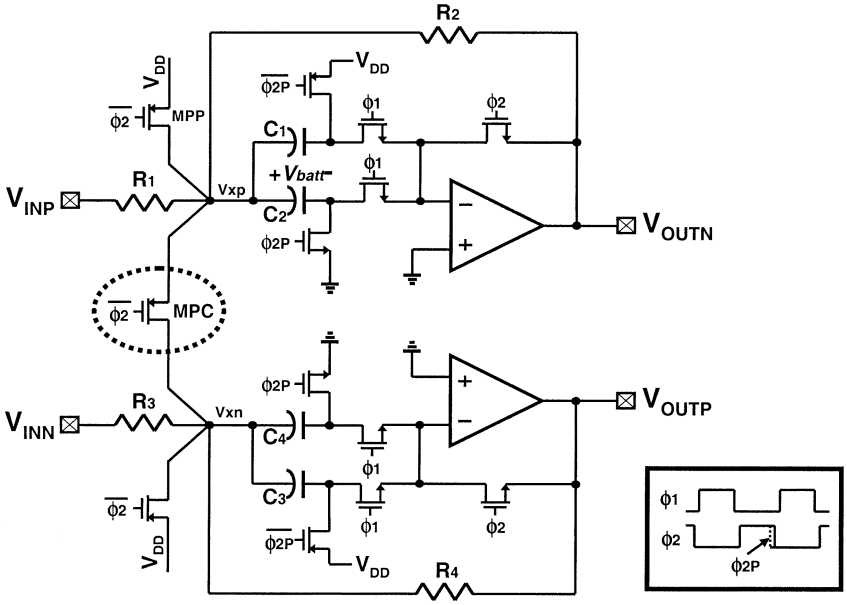

Fig. 2. Input buffering circuit.

version of the circuit. The modifications include using a pseudo-differential configuration and the unity-gain reset structure to apply the ORST. The inverting unity gain of the tracking signal is obtained from a one-to-one resistor ratio. During the reset phase (ϕ_2), $V_{\rm XP}$ is pulled up to $V_{\rm DD}$ while C_1 is precharged to $V_{\rm DD}$ and C_2 is discharged. During the amplification phase (ϕ_1), $V_{\rm XP}$ becomes $V_{\rm DD}/2(V_{\rm batt})$ due to the charge sharing between C_1 and C_2. Assuming that the input common-mode voltage is $V_{\rm DD}/2$, the output common-mode voltage also becomes $V_{\rm DD}/2$ because of the equivalent function of an intermediate virtual ground $V_{\rm XP}$.

During ϕ_2 (ignoring the body effect for simplicity), the resistance of the pMOS switch MPP is

$$R_{\rm MPP} = \frac{1}{\beta\left[(V_{SG} - |V_{TH}|) - V_{SD}\right]} \tag{1}$$

where $\beta = \mu_p C_{\rm OX}(W/L)$. The voltage division between linear R_1 and nonlinear $R_{\rm MPP}$ introduces distortion at $V_{\rm XP}$:

$$V_{\rm XP} = \left(\frac{R_2' R_{\rm MPP}}{R_1 R_2' + R_1 R_{\rm MPP} + R_2' R_{\rm MPP}}\right) V_{\rm INP} + \left(\frac{R_1 R_2'}{R_1 R_2' + R_1 R_{\rm MPP} + R_2' R_{\rm MPP}}\right) V_{\rm DD} \tag{2}$$

where $R_2' = R_2 + (1/g_{m\_\rm opamp})$. The level-shifting voltage $V_{\rm batt}$, nominally $V_{\rm DD}/2$, is a function of $V_{\rm XP}$, while $V_{\rm OUTN}$ is a function of $V_{\rm batt}$. Assuming for simplicity that the opamps have a finite open-loop gain A those voltages are given by

$$V_{\rm batt} = \frac{V_{\rm XP}(C_1 + C_2) - (C_1 V_{\rm DD} + C_2 {\rm GND})}{C_1 + C_2} \tag{3}$$

and

$$V_{\rm OUTN} = \left(1 + \frac{1}{A}\left(1 + \frac{R_2}{R_1}\right)\right)^{-1} \cdot \left(\left(1 + \frac{R_2}{R_1}\right) V_{\rm batt} - \left(\frac{R_2}{R_1}\right) V_{\rm INP}\right). \tag{4}$$

It can be observed that the output harmonic distortion results from the nonlinear fluctuation at $V_{\rm XP}$ caused by $R_{\rm MPP}$ nonlinearity. A straightforward way to reduce this distortion is to increase the size of MPP such that the amount of nonlinearity is suppressed by the ratio between $R_{\rm MPP}$ and R_1. In the proposed circuit, a differential resetting switch MPC is employed instead. It can be made half the size of MPP and achieves the performance equal to doubling the size of MPP. The MPC switch also suppresses any even-order harmonics that are coming from the device mismatches between the two pseudodifferential signal paths. That is because MPC provides a differentially stable $V_{\rm DD}$ reference level to both $V_{\rm XP}$ and $V_{\rm XN}$ during the reset phase.

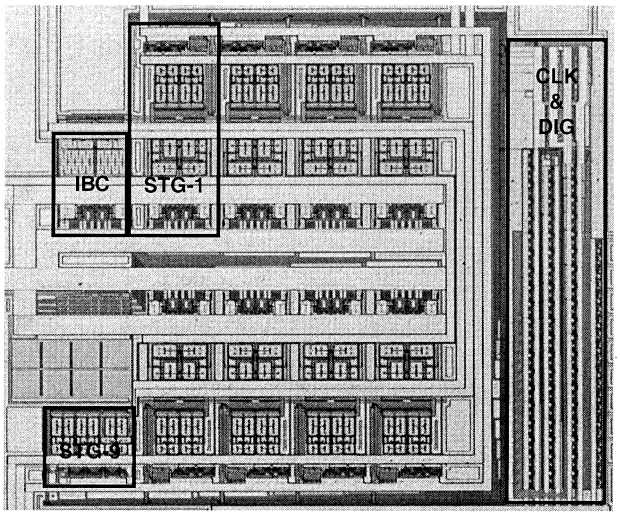

Fig. 3. Die photograph.

III. Measured Results

A prototype ADC, incorporating the circuit details described in the previous sections, was implemented in a 0.35-μm CMOS technology where pMOS and nMOS thresholds are 0.9 and 0.7 V, respectively. The die photograph is shown in Fig. 3. The active die area is 1.6 mm $\times$ 1.4 mm. All analog building blocks including opamps and capacitors are concentrated at the center

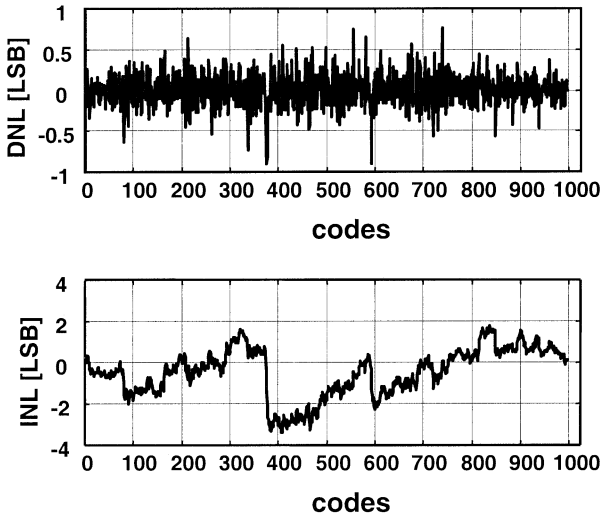

Fig. 4. DNL and INL at 25 MS/s.

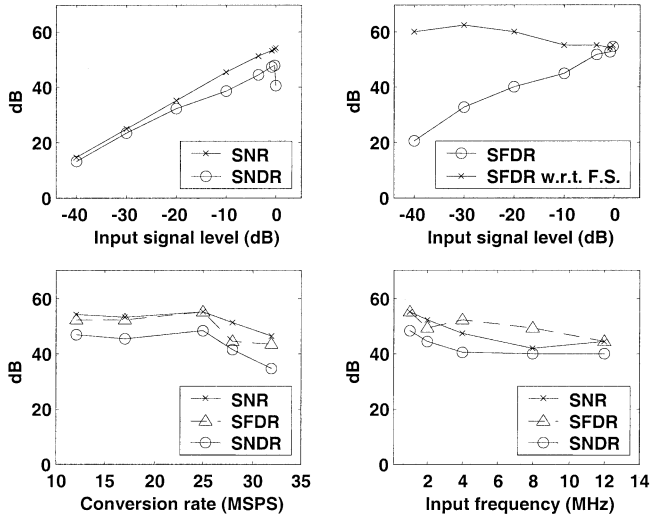

Fig. 5. Dynamic measurements with 1-MHz input and 25 MS/s (unless noted otherwise).

part of the chip while the comparators and digital blocks are along the perimeter. All measurements were obtained with a single 1.4-V power supply.

The prototype was first characterized with a code density test for differential nonlinearity (DNL) and integral nonlinearity (INL) as shown in Fig. 4. The resulting code density histogram was obtained for a 25-MS/s sampling rate with a full-scale 140-kHz sinusoidal input. A total of 2^{15} samples were collected (same for the dynamic measurements). Large INL jumps can be seen at $\pm V_{\rm ref}/4$ which are suspected to be coming from poorly matched capacitors at the first-stage MDAC. This poor matching characteristic can also be found in the dynamic measurements of Fig. 5. The spurious-free dynamic range (SFDR), with respect to the full-scale input, remains relatively fixed for different input signal levels. The ADC operates up to a maximum speed of 32 MS/s as shown in Fig. 5. It also operates (at 25 MS/s) down to a supply voltage of 1.3 V with 5-dB signal-to-noise-plus-distortion ratio (SNDR) degradation. Table I summarizes the measured performance of the ADC.

TABLE I
MEASUREMENT SUMMARY

Technology	0.35-μm 1P 5M CMOS
Resolution	10-bit
Chip size	1.6mm $\times$ 1.4mm
Supply voltage	1.4 V
Conversion rate	25 MSPS
Input signal range	1.4 V_{pp} differential
Input resistance	5 kΩ
Power consumption	21 mW
DNL / INL	0.9 LSB / 3.3 LSB
SFDR / SNR / SNDR	55 dB / 55 dB / 48 dB

IV. CONCLUSION

A switching technique for low-voltage operation has been described. The opamp-reset switching technique does not use boosting, bootstrapping, switched-opamp, or threshold scaling. It is also free from any device reliability issues. The new technique is suitable for high-speed switched-capacitor circuit design and it has been applied to the IC implementation of a 1.4-V 10-bit 25-MS/s pipelined ADC. The proposed technique is expected to be applicable to other high-resolution and ultra low-voltage designs. The prototype IC fabricated in a 0.35-μm CMOS with $|V_{\rm TH,P}| = 0.9$ V operates with a supply voltage down to 1.3 V and occupies 1.6 mm $\times$ 1.4 mm active die area. The measurement results demonstrate 55-dB SNR, 55-dB SFDR, and 48-dB SNDR.

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