

# A 1.8-V 67-mW 10-bit 100-MS/s Pipelined ADC Using Time-Shifted CDS Technique

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**Abstract**—A *time-shifted correlated double sampling (CDS)* technique is proposed in the design of a 10-bit 100-MS/s pipelined ADC. This technique significantly reduces the finite opamp gain error without compromising the conversion speed, allowing the active opamp blocks to be replaced by simple cascoded CMOS inverters. Both high-speed and low-power operation is achieved without compromising the accuracy requirement. An efficient common-mode voltage control is introduced for pseudodifferential architecture which can further reduce power consumption. Fabricated in a 0.18- $\mu\text{m}$  CMOS process, the prototype 10-bit pipelined ADC occupies 2.5 mm<sup>2</sup> of active die area. With 1-MHz input signal, it achieves 65-dB SFDR and 54-dB SNDR at 100 MS/s. For 99-MHz input signal, the SFDR and SNDR are 63 and 51 dB, respectively. The total power consumption is 67 mW at 1.8-V supply, of which analog portion consumes 45 mW without any opamp current scaling down the pipeline.

**Index Terms**—Analog-to-digital converter (ADC), correlated double sampling (CDS), data converter, high speed, low power, low voltage, pipeline.

## I. INTRODUCTION

THE pipelined ADC architecture has been adopted into many high-speed applications including high-performance digital communication systems and high-quality video systems [1], [2]. The rapid growth in these application areas is driving the design of ADCs toward higher operating speed, lower power consumption and smaller die size. The continuing trend of submicron CMOS technology scaling, which is coupled with lower power supply voltages, makes it possible to keep up with the application development. However, this trend poses challenges to conventional pipelined ADC designs which rely on high-gain operational amplifiers to produce high-accuracy data converters. At low power supply voltage, large open-loop operational amplifier (opamp) gain is difficult to realize without sacrificing bandwidth and/or power consumption. As a result, the finite opamp gain is becoming a major hurdle in achieving both high speed and high accuracy.

One way to bypass this issue is to maintain a high opamp gain even at reduced power supply voltages. This is usually realized by multistage opamp structure, gain boost technique, and long channel devices biased at low current density. The price paid for

this approach is complex design, large die area, high power consumption, and/or low bandwidth. The power and speed advantages of submicron CMOS technology are diminished or even completely lost. To avoid this undesirable overhead and to fully exploit the benefits of advanced submicron CMOS processes, it becomes necessary to use a low-gain single-stage opamp instead and to explore efficient circuit techniques which can tolerate the low opamp gain. Various digital self-calibration techniques [3]–[5] can correct the errors due to finite opamp gain as well as capacitor mismatches, but the normal conversion operation has to be stopped during the error measurement (i.e., foreground calibration). To avoid this interruption, background calibration may be used in pipelined ADCs [6]–[9]. However, the implementation tends to become very complex. Moreover, the power consumption and die area increases considerably.

Another solution to this low opamp gain problem is the use of correlated double sampling (CDS) technique [10], [12]. CDS techniques have been used successfully in integrator and amplifier designs. With CDS, the error resulting from the finite opamp gain becomes inversely proportional to the square of the opamp gain. This equivalently doubles the opamp gain in decibels (dB). Furthermore, the opamp offset is removed, and 1/f noise is also suppressed. However, the straightforward implementation of CDS in pipelined ADC design increases load on the opamp and adds one extra clock phase (a detailed discussion is found in Section II). To solve this problem, we present in this paper a *time-shifted CDS* technique [14]. The proposed technique is highly effective for finite opamp gain compensation in the context of low-voltage and high-speed pipelined ADCs. Due to this effective gain compensation, the time-shifted CDS technique enabled a successful implementation of a low-power and high-speed pipelined ADC that uses simple cascoded CMOS inverters in place of traditional opamps.

The rest of this paper is organized as follows: Section II describes the time-shifted CDS technique; Section III describes the circuit implementation of the prototype 10-bit pipelined ADC; and Section IV presents the experimental results. Concluding remarks are given in Section V.

## II. TIME-SHIFTED CDS TECHNIQUE

One of the simplest implementations of pipelined ADCs incorporating digital correction/redundancy is based on the 1.5-bit-per-stage architecture shown in Fig. 1. This architecture is widely used to maximize conversion speed [13]. Fig. 2 shows a typical multiplying digital-to-analog converter (MDAC) used in this type of pipelined ADC architecture. The output of this MDAC at the end of the amplification phase ( $\phi_2$ ) is

$$V_o = \left( \frac{C_s + C_f}{C_f} \right) \cdot V_i - \left( \frac{C_s}{C_f} \right) \cdot V_R + e \quad (1)$$

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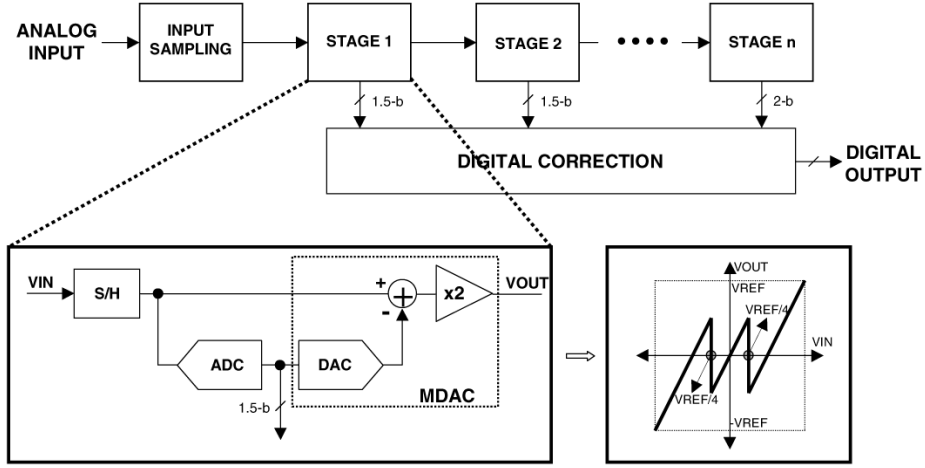


Fig. 1. Typical 10-bit (1.5-bit-per-stage) pipelined ADC.

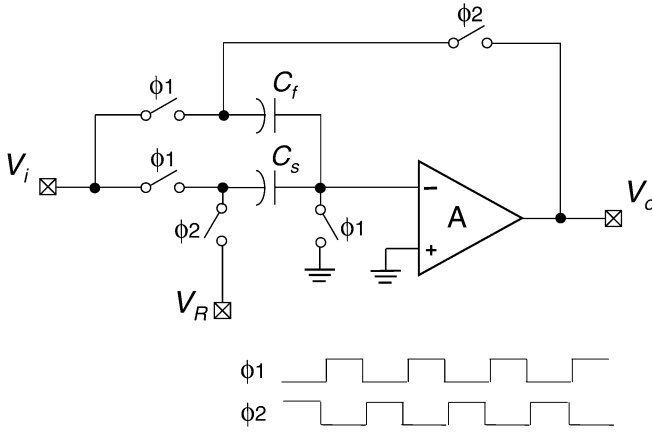


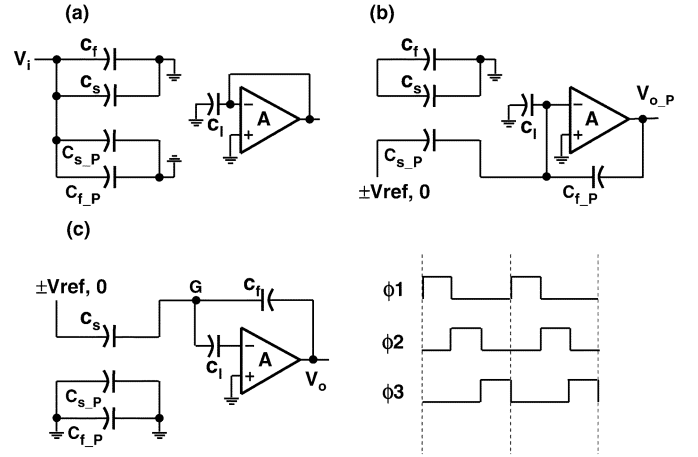
Fig. 2. Typical switched capacitor MDAC.

where  $V_i$  is the sampled input ( $\phi_1$ ),  $V_R$  is  $\{\pm V_{\text{ref}}, 0\}$  which depends on the result of the sub-ADC conversion of the sampled input, and the error resulting from the finite opamp gain is

$$e = \frac{-1}{A} \left( 1 + \frac{C_s}{C_f} \right) \cdot V_o. \quad (2)$$

This error ( $e$ ) is inversely proportional to the opamp gain  $A$ , directly deteriorating the overall linearity of the ADC.

As mentioned earlier, one effective finite opamp gain compensation method is the CDS technique, which mitigates the error due to finite opamp gain, making it inversely proportional to the *square* of the opamp gain. Fig. 3 illustrates one straightforward implementation of the conventional predictive CDS in the context of a 1.5-bit MDAC. Three clock phases and two sets of switches and capacitors are required in this scheme. The capacitors  $C_{s\_P}$  and  $C_{f\_P}$  are for the predictive MDAC operation, and the capacitors  $C_s$  and  $C_f$  are for the real MDAC operation. First, during the sampling phase  $\phi_1$ , all the capacitors are sampled to the input voltage  $V_i$ . Next, during the predictive amplifying phase  $\phi_2$ ,  $C_s$  and  $C_f$  hold the sampled input signal, while  $C_{s\_P}$  and  $C_{f\_P}$  produce the predictive output signal. In the meantime, the nonzero error voltage due to finite opamp gain at the negative input of opamp is stored in  $C_I$ . Finally, during the real amplifying phase  $\phi_3$ ,  $C_s$  and  $C_f$  produce the real output signal. Because  $C_I$  is connected between the negative input of


 Fig. 3. MDAC with conventional CDS. (a) Sampling phase  $\phi_1$ . (b) Pre-amplifying phase  $\phi_2$ . (c) Amplifying phase  $\phi_3$ .

opamp and the common node of  $C_s$  and  $C_f$  (node G), a much more accurate virtual ground is created at node G. The output error due to finite opamp gain is mostly cancelled. Naturally, this cancellation will not be perfect, and the output error after CDS is given by

$$e \approx \frac{-1}{A^2} \left( 1 + \frac{C_s}{C_f} \right) \left[ \left( 1 + \frac{C_s + C_I}{C_f} \right) \cdot V_o(n) - \left( \frac{C_I}{C_f} \right) \cdot V_o(n-1/2) \right] \quad (3)$$

where  $V_o(n)$  is the current output in the main pipeline, and  $V_o(n-1/2)$  is the output of the previous clock phase (predictive pipeline). Note that the error ( $e$ ) is inversely proportional to  $A^2$ . This equivalently doubles the opamp gain in decibels. In a practical design, this equivalent opamp gain boosting may be less significant due to parasitics and other second-order effects, but despite this practical limitation at least 30 dB improvement can be achieved easily. This would be enough for most low-voltage pipelined ADC designs where finite opamp gain is the limiting factor.

Although the CDS scheme described above can nearly eliminate the MDAC's residue error due to finite opamp gain, it comes with a price. Two drawbacks can be observed from the

above illustration. First, one extra clock phase is required in addition to the conventional nonoverlapping two-phase clocking scheme in the switched capacitor (SC) circuit. This implies that either the opamp settling time has to be reduced for the same clock frequency, or the clock frequency has to be reduced to maintain the same opamp settling time. Faster opamp settling time requires larger power consumption. Therefore, either the power consumption or the conversion rate is compromised in this CDS scheme. Second, during the sampling phase  $\phi_1$ , both predictive sampling capacitors and real sampling capacitors are connected to the driving stage output, resulting in double load to the driving stage opamp, assuming all capacitors are the same size. As a direct result of this increased load, the opamp bandwidth gets reduced. If the same bandwidth is to be maintained, more bias current is needed. Once again, either the power consumption or the conversion rate has to be compromised for this opamp gain compensation. These two drawbacks make the CDS technique less suitable for the high-speed pipelined ADC design where the power and speed requirements are stringent. Therefore, it would be highly desirable to find a new method to incorporate the CDS operation into the pipelined ADC so that the large conversion rate and/or power consumption overhead would be avoided.

Such a solution indeed exists, and we refer to it as the time-shifted CDS since this can be implemented by incorporating some timing adjustments to the conventional predictive CDS scheme [14]. The important goals of the time-shifted CDS are to eliminate the one extra clock phase and to realize the pre-sampling and real sampling in different clock phases to avoid added capacitive loading. The two drawbacks of the conventional CDS are to be avoided. This timing change is illustrated in Fig. 4. Fig. 4(a) shows the timing of two cascaded stages in the pipelined ADC using the conventional CDS. Note the necessary overlap between the amplifying phase of stage  $i$  and the sampling/presampling phase of stage  $i + 1$  for correct signal processing. It is not difficult to find that the “preliminary” residue voltage of stage  $i$  is already available for sampling in the pre-amplifying phase. Stage  $i + 1$  can make use of this time slot to do the pre-sampling without any timing conflict. As a result, the double capacitive loading to the output of stage  $i$  is avoided by this separation of the pre-sampling and sampling phases. This new timing scheme is shown in Fig. 4(b). Note that the entire timing of stage  $i + 1$  is shifted one clock phase ahead, and the sampling phase and the pre-amplifying phase share the same time slot. Now it can be seen that the amplifying phase and the pre-sampling phase can be merged into one clock phase since they are totally independent of each other. The resulting time-shifted CDS clock scheme is shown in Fig. 4(c). Only two clock phases are required in this scheme. No extra load is added to the opamp during any clock phase. The speed and/or power consumption overhead in the conventional predictive CDS technique is removed completely.

Fig. 5 shows the proposed 10-bit pipelined ADC architecture employing the time-shifted CDS technique. Conceptually, this architecture realizes two pipelined paths working in parallel for the first few stages. One path represents the *predictive* path which only operates for the first four stages, and the other path represents the main signal path which operates for all nine stages

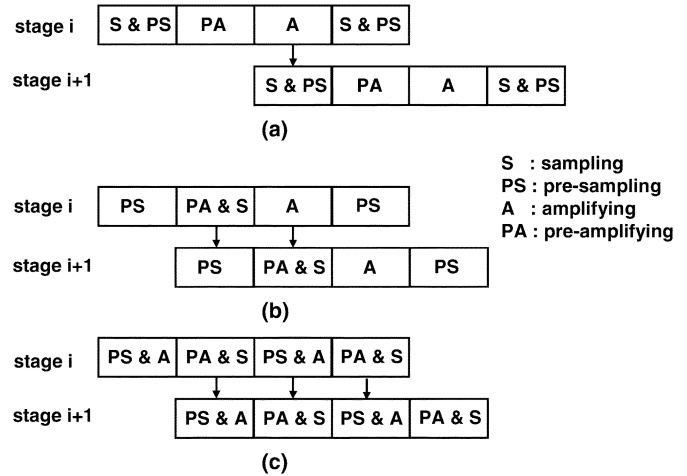


Fig. 4. Timing change from conventional CDS to time-shifted CDS.

necessary for the 10-bit conversion. The first four stages of the main signal path are very similar to their corresponding stages in the predictive path, and they share the same set of active stages (opamps/inverters and comparators), thus there is no duplication of active stages. Both signal paths (main and predictive) process the same input signal from the first sample-and-hold (S/H) stage, but the main signal path is delayed a half clock cycle (one phase) by an additional S/H (actual implementation shares the same opamp/inverter) following the first S/H. The input signal is first processed by the predictive pipeline and the finite opamp gain error is stored on a capacitor. The stored error is used to correct the corresponding stage in the main pipeline in the following clock phase (half clock cycle delay). As both signal paths (predictive and main) share the same opamp/inverter, this operation is easily achieved with added switches and capacitors.

The SC implementation of this MDAC operation merging both the predictive pipeline and the main pipeline is shown in Fig. 6.  $V_i$  and  $V_o$  are the input/output of the main pipeline, and  $V_{i,P}$  and  $V_{o,P}$  are the input/output of the corresponding predictive pipeline. The capacitors are chosen such that  $C_{s,P} = C_{f,P} = C_s = C_f$ . In the proposed time-shifted CDS scheme, the sampling and amplifying operation is actually performed twice. The initial/first operation is done by  $C_{s,P}$  and  $C_{f,P}$ , and the nonzero error voltage due to finite opamp gain at the negative input of opamp is stored in  $C_I$ . The following/second operation is done by  $C_s$  and  $C_f$ , with  $C_I$  connected between the negative input of opamp and the common node of  $C_s$  and  $C_f$  (node G). An accurate virtual ground is created at node G. While the operation of this time-shifted CDS technique may appear to be similar to conventional CDS techniques [10], [11], it performs without the additional capacitive load to the opamp and/or the extra clock phase(s) to the ADC operation. Any possible speed penalty due to CDS operation is completely avoided, which is critical in achieving the low-power and high-speed ADC performance.

Some design considerations of the proposed architecture are described in the following. First, because the inputs of MDAC are not the same for the predictive path and the main path (with the exception of the very first MDAC), the effect of error correction will not be as good as the conventional CDS techniques.

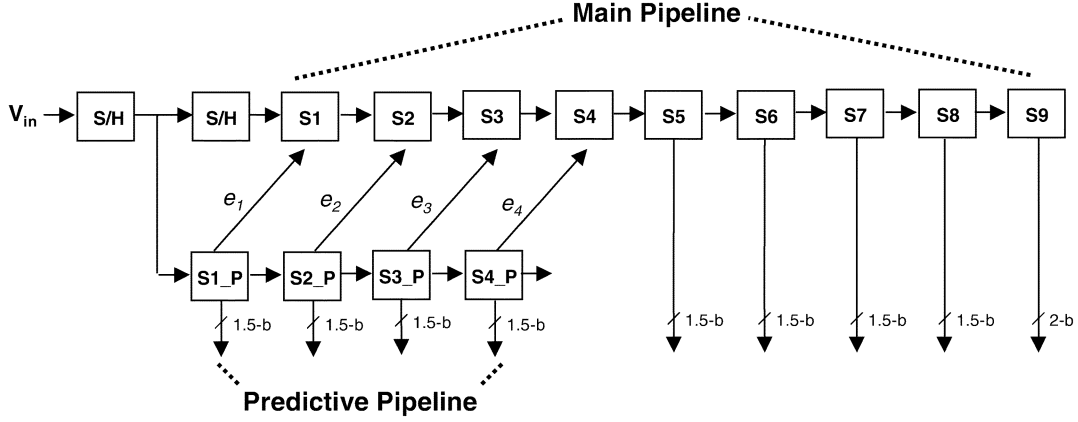


Fig. 5. Proposed 10-bit pipelined ADC architecture.

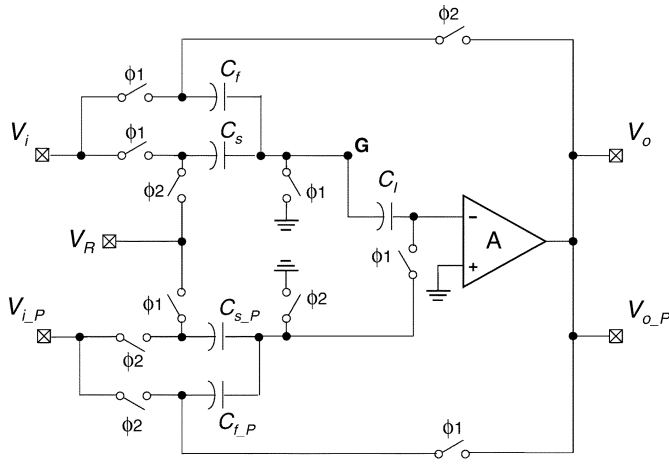


Fig. 6. Feasible MDAC structure with time-shifted CDS.

The output error at stage  $i$  in the main pipeline is approximately given by

$$e_i \approx \frac{-i}{A^2} \left(1 + \frac{C_s}{C_f}\right) \left[ \left(1 + \frac{C_s + C_I}{C_f}\right) \cdot V_{oi}(n) - \left(\frac{C_I}{C_f}\right) \cdot V_{oi}(n - 1/2) \right] \quad (4)$$

where  $V_{oi}(n)$  is the current output in the main pipeline, and  $V_{oi}(n - 1/2)$  is the output of previous clock phase (predictive pipeline). Note that the error is inversely proportional to  $A^2$ . However, this error will increase from stage to stage down the pipeline. This is because the discrepancy between the outputs of the predictive path and the main path will become larger from stage to stage down the pipeline. Fortunately, the accuracy requirement of the pipelined ADC is reduced as the residue signal propagates down the pipeline, and this decreasing accuracy of CDS operation down the pipeline is comfortably tolerated. The second design issue is that the time-shifted CDS will effectively add extra offset to sub-ADCs in the main pipeline. The reason is that the MDACs in the main pipeline need to use the digital code generated by the sub-ADCs in the predictive pipeline. This is equivalent to putting a signal-dependent offset to the sub-ADCs in the main pipeline. Fortunately, digital redundancy of the pipelined ADC is able to correct for the offset, whether signal-

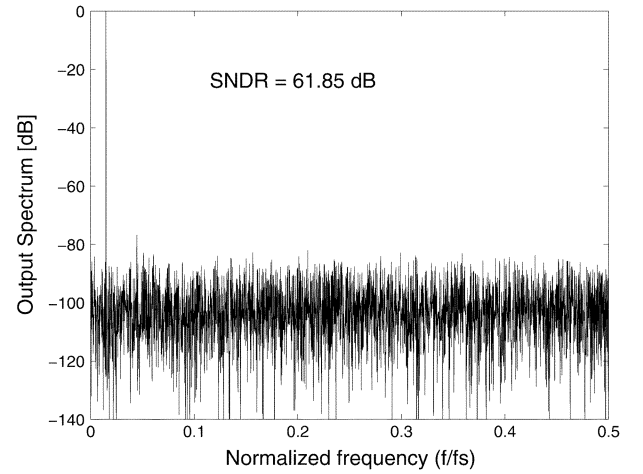


Fig. 7. Pipelined ADC employing conventional CDS technique.

dependent or not, as long as the amount of the offset is within the correctable range ( $\pm V_{\text{ref}}/4$  for 1.5-bit-per-stage MDAC).

Some behavior simulations have been done to verify the effectiveness of the proposed architecture. In simulation, the opamp gain was chosen to be 40 dB, the capacitor mismatch was assumed to be less than 0.1%, and the random offsets of sub-ADCs were assumed to be less than  $\pm V_{\text{ref}}/8$ . Fig. 7 shows the results of the architecture using the conventional CDS technique (recall the extra capacitive load and extra clock phase overhead). Fig. 8 shows the results of the proposed architecture using the time-shifted CDS technique in the first five stages. It can be seen that their performances are very close in terms of SNDR. The third-order harmonic in the time-shifted CDS is found to be a bit higher than in the conventional CDS. This is because the proposed time-shifted architecture does face a small and increasing degradation of error correction down the pipeline, as noted earlier. The larger third harmonic observed is due to insufficient gain error correction for the later stages. The reason this degradation does not significantly degrade the overall performance is because the opamp gain requirement is also reduced down the pipeline as MSBs are resolved. For comparison, the simulation results of the regular pipelined ADC without any gain error correction is shown in Fig. 9. Note that the SNDR is only about 43 dB, which is 16 dB lower than the SNDR of architectures with gain error correction.

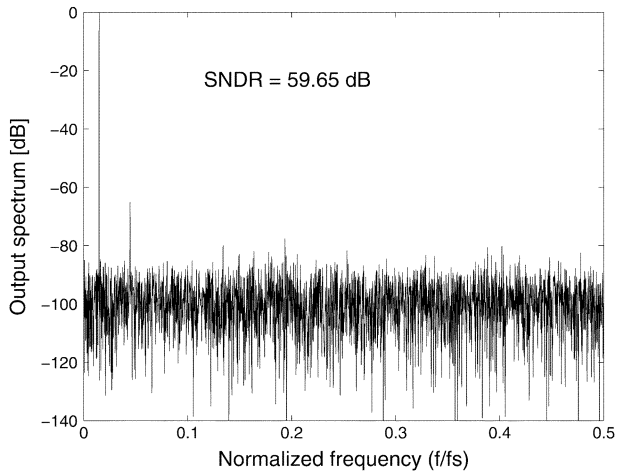


Fig. 8. Proposed pipelined ADC architecture applying time-shifted CDS.

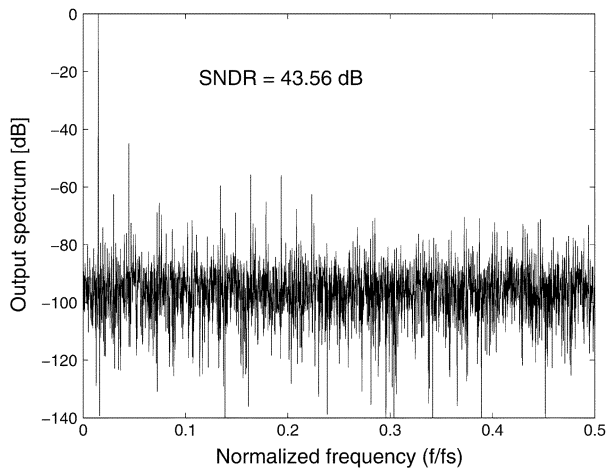


Fig. 9. Pipelined ADC without any gain error correction.

### III. CIRCUIT DESIGN

#### A. CMOS Inverter as Opamp

The opamp is one of the most critical building blocks in pipelined ADCs. The opamp dc gain and bandwidth determine the achievable accuracy and conversion rate. For a 10-bit pipelined ADC, the open-loop opamp gain needs to be well over 60 dB. It is not uncommon to see 80-dB gain in practical design examples. Designing such a high-gain opamp at low supply voltage is quite challenging because traditional stacking of cascode transistors is not feasible. Use of compensated multistage opamps will lead to considerably increased power consumption and reduced speed. In this prototype IC implementation, we used simple cascoded (both the NMOS input and PMOS current source) CMOS inverters, as shown in Fig. 10. Replacing opamps with these inverters allowed large signal swing, large bandwidth, and low power consumption. The simulation results of the designed inverter in 0.18- $\mu\text{m}$  CMOS technology is summarized in Table I. More than 2-GHz gain bandwidth and 1- $V_{pp}$  single-ended signal swing from 1.8-V power supply are achieved with only 1-mA current dissipation, and the open-loop dc gain is 43 dB. This level of dc gain is insufficient for 10-bit accuracy, but we are able to tolerate the low dc gain due to the enhancements achieved from the time-shifted CDS technique described in the above.

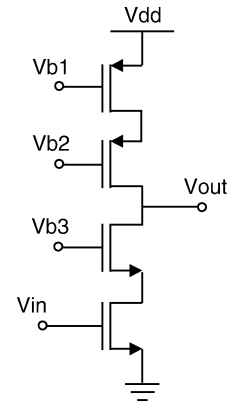


Fig. 10. Simple cascoded CMOS inverter.

TABLE I  
SIMULATION RESULTS OF CMOS INVERTER

Technology	0.18 $\mu\text{m}$ CMOS
Supply Voltage	1.8V
DC gain	43dB
Bandwidth	2.4GHz (0.5pF load)
Signal Swing	1Vpp
Input Cap.	0.2pF
Bias Current	1mA

#### B. Pseudodifferential MDAC

The use of inverters in place of opamps implies inherently single-ended design. We have adopted pseudodifferential configuration throughout the pipelined ADC design to suppress even-order harmonics and supply/substrate noise. In other words, two single-ended MDACs in parallel are used to build the pseudodifferential MDAC. While the pseudodifferential pipelined ADC can achieve lower power consumption than its fully differential counterpart, as demonstrated by Miyazaki [15], it still requires some sort of equivalent common-mode feedback (CMFB) operation. Without the equivalent CMFB function, any common-mode error in the pipeline would be amplified in just the same way that the differential input signal is amplified (residue amplification). This can cause single-ended opamps (inverters) to saturate down the pipeline. To mitigate this issue, a hybrid structure which includes both fully differential stages and pseudodifferential stages was employed in [15]. The price paid is increased power consumption and design complexity due to the use of the fully differential MDAC. In order to fully exploit the low-power advantage of pseudodifferential architecture without implementing a traditional CMFB with power consumption overhead, a new pseudodifferential MDAC that uses a differential *float* sampling scheme is proposed. This is shown in Fig. 11 (time-shifted CDS not shown for simplicity). The differential gain of this MDAC is still two, but the common-mode gain is just one, because one pair of input capacitors ( $C_2$  and  $C_3$ ) is differentially sampled without a specific common-mode reference (thus floating). This equivalent CMFB operation is achieved with no speed penalty. The complete pseudodifferential MDAC incorporating time-shifted CDS is shown in Fig. 12.

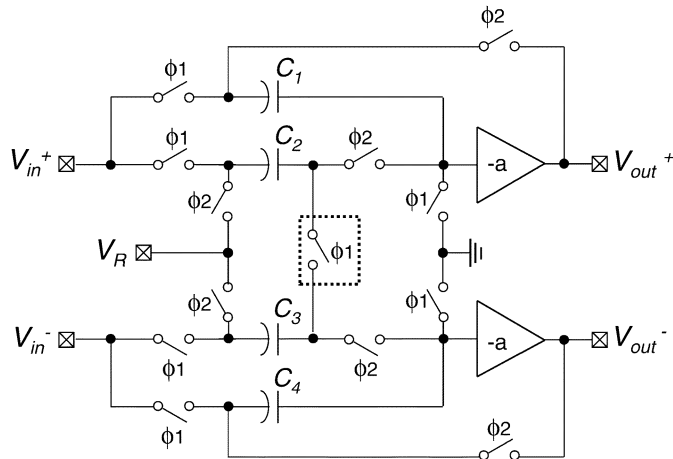


Fig. 11. Pseudodifferential MDAC with common-mode control scheme.

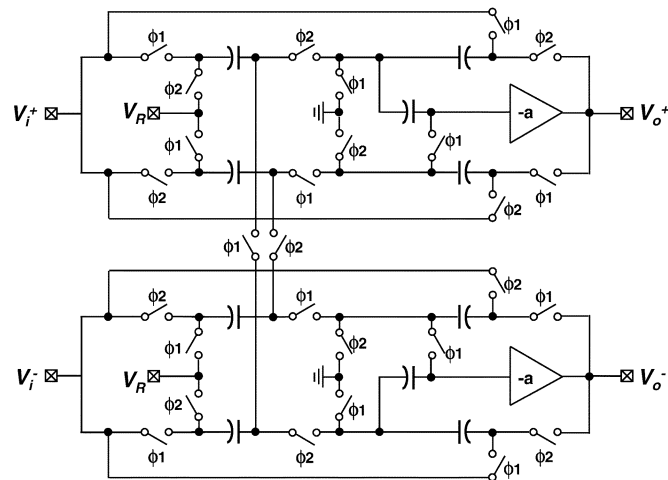


Fig. 12. Pseudodifferential MDAC with time-shifted CDS.

For comparison, another pseudodifferential MDAC that does not suffer from common-mode error amplification is shown in Fig. 13 [16]. Note there is one, doubled in size, dedicated sampling capacitor  $C_s$ , one dedicated feedback capacitor  $C_f$ , and one reference injection capacitor  $C_r$  that had to be added. During the amplifying phase, the bottom plates of the sampling capacitors are connected together to transfer only differential charge to the feedback capacitor. Therefore, this noncapacitor-flip-over pseudodifferential MDAC can decouple the input and output common-mode voltage. However, the opamp feedback factor drops from 1/2 to 1/4 in this structure, resulting in large loop bandwidth reduction. Moreover, the  $kT/C$  noise and opamp noise is also doubled. All these drawbacks make it unsuitable for our high-speed and low-power prototype ADC design.

C. Double-Sampling S/H Stage

A front-end S/H circuit is critical in the design of a high-performance pipelined ADC. It usually takes up a large die area and consumes much power. The S/H also puts limits on linearity and noise. The proposed architecture shown in Fig. 5 indicates that two front-end S/H blocks are required to apply the time-shifted CDS technique. Implementing an extra S/H will not only add power consumption and die area but will also add noise to the input signal. However, we can realize the equivalent function of

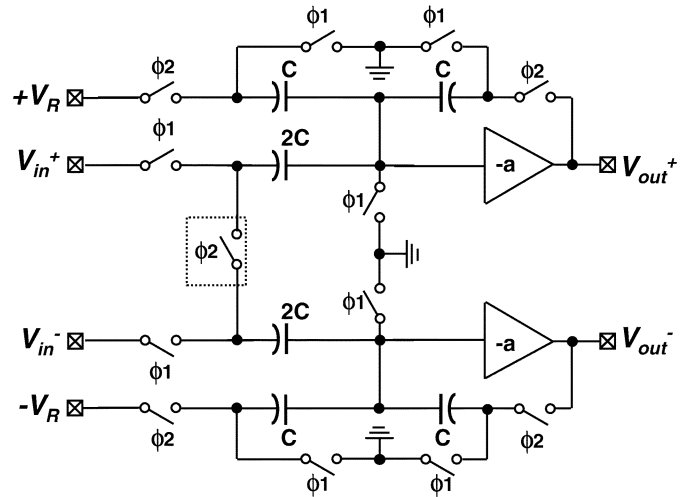


Fig. 13. Noncapacitor-flip-over pseudodifferential MDAC.

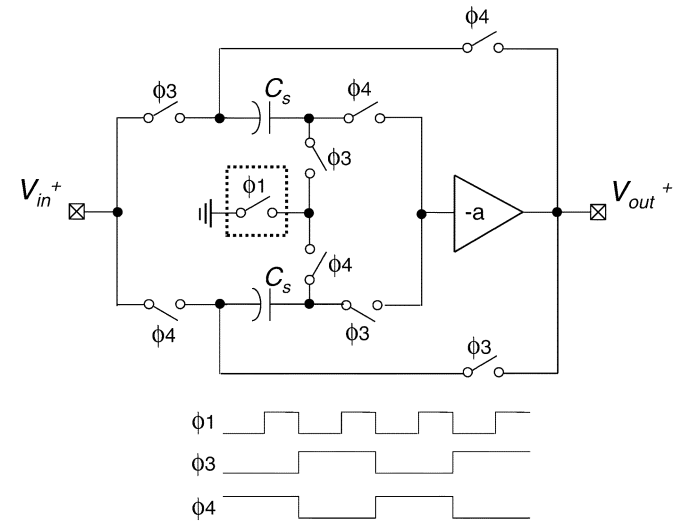


Fig. 14. Timing-skew insensitive double-sampling S/H circuit.

these two S/H circuits by using just one double-sampling S/H. Thus, there will not be any added power consumption, die area, or noise. Fig. 14 shows the double-sampling S/H circuit that is implemented (single-ended illustrated for simplicity) in this prototype IC. There are two sets of sampling switches and capacitors for this time-interleaved operation, and they operate at half the speed of the overall ADC. This S/H circuit will provide a sampled output (hold operation) for two sampling phases of the first-stage pipeline employing the time-shifted CDS. This double-sampling S/H circuit is insensitive to timing skew due to the use of a series master sampling switch [17]. The capacitor mismatches are alleviated due to inherent voltage-mode operation (i.e., sampled input voltage is “flipped” to the output). The opamp offset and gain mismatches (memory) are manageable at the 10-bit level. In this S/H, a CMOS inverter is also employed in place of a conventional opamp to reduce power consumption. Note that we did not use CDS in this S/H circuit. The finite/low gain of the inverter used in the S/H circuit only causes linear gain error, which can be tolerated in most applications, without degrading the linearity of ADC. The linearity of the low-gain inverter was found sufficient for 10-bit accuracy at the specified signal swing.



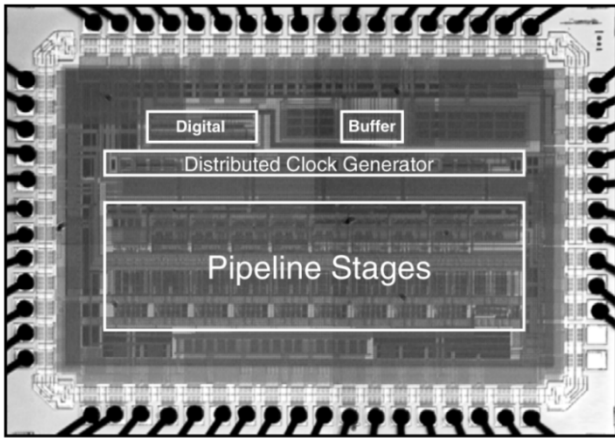


Fig. 18. Die photograph of the prototype ADC.

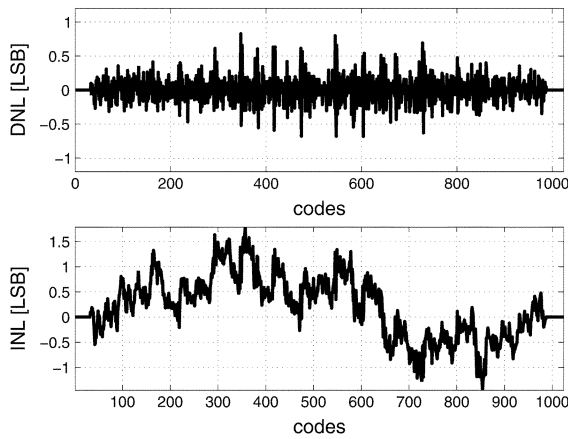


Fig. 19. DNL and INL plot.

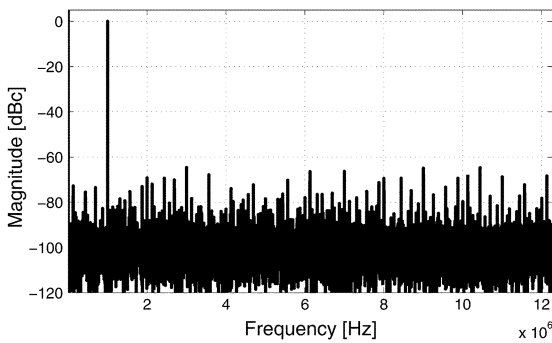


Fig. 20. Measured signal spectrum at 100 MS/s.

analog portion consumes 45 mW. The measured DNL and INL are 0.8 LSB and 1.6 LSB, as shown in Fig. 19. With 1-MHz input and 100 MS/s, the measured SFDR, SNR, and SNDR are 65, 55, and 54 dB, respectively. Fig. 20 shows a typical measured frequency spectrum at 1-MHz input and 100 MS/s (the digital output of the ADC is decimated/downsampled by 4 on chip for testing purposes). Fig. 21 shows the dynamic performance versus the magnitude of 1MHz input at 100 MS/s. Fig. 22 shows the dynamic performance versus input frequency at 100 MS/s. The measured SFDR, SNR, and SNDR at 99-MHz input frequency are 63, 52, and 51 dB, respectively. Fig. 23 shows the dynamic performance versus conversion/clock rate with 1-MHz input signal. Performance degrades past 100 MS/s,

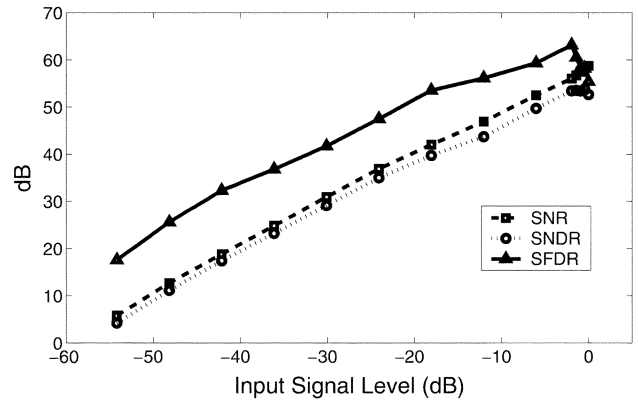


Fig. 21. Measured dynamic performance versus input signal level.

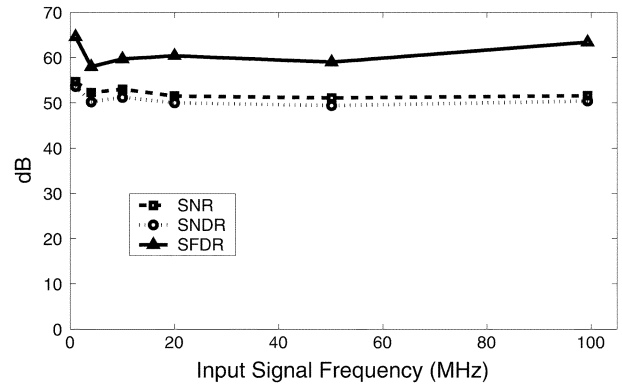


Fig. 22. Measured dynamic performance versus input signal frequency.

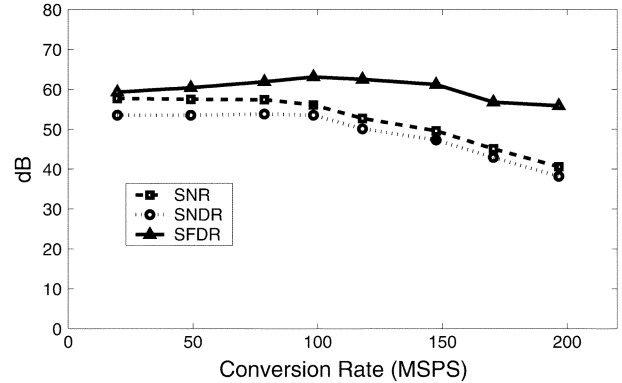


Fig. 23. Measured dynamic performance versus conversion rate.

but continues to operate up to 200 MS/s. The measurement results are summarized in Table II.

### V. CONCLUSION

A time-shifted CDS technique which compensates the finite amplifier gain of an inverter-based pipelined ADC is described. The proposed technique enables low-power and high-speed operation by allowing significantly reduced amplifier gain. Prototype IC measurements demonstrate 67-mW 10-bit 100-MS/s performance. While it is a common practice to scale opamp bias currents and capacitor sizes down the pipeline to reduce power consumption in practical pipelined ADC design [19], [20], no scaling was applied for prototyping convenience. All opamps dissipate the same amount of current throughout the pipelined ADC. It is expected that 20%–30% further reduction of analog



TABLE II  
PERFORMANCE SUMMARY

Resolution	10-bit
Sampling Rate	100MSPS
Technology	0.18 $\mu$ m CMOS
Supply Voltage	1.8V
Power Consumption	67mW (45mW analog)
DNL/INL	0.8LSB / 1.6LSB
SNR/SNDR/SFDR	55dB / 54dB / 65dB
Die Area	1.2mm $\times$ 2.1mm

power consumption can be achieved with proper opamp scaling. The achieved results indicate that a design incorporating an effective CDS techniques (e.g., time-shifted CDS) in combination with simplistic active stages (e.g., inverter) can achieve significant speed improvement, while maintaining, or even lowering, the overall power consumption. This time-shifted CDS technique can be also used in a fully differential implementation of a pipelined ADC. The fully differential implementation may end up being simpler than the pseudodifferential ADC, since a CMFB circuit would be used, completely avoiding the common-mode voltage drift issue. However, a fully differential circuit is likely to have higher power consumption due to the added CMFB circuit. The fully differential opamp signal swing will also have to be reduced with the use of a tail current source, although it would provide better noise rejection. In short, the fully differential implementation would provide a better SNR with an increased power consumption.

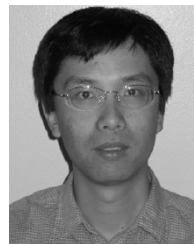
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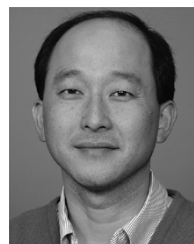
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