LINEARITY IMPROVEMENT TECHNIQUE FOR CMOS CONTINUOUS-TIME FILTERS

BY

UN-KU MOON

B.S., University of Washington, 1987
M.E., Cornell University, 1989

THESIS

Submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy in Electrical Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 1994

Urbana, Illinois

UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

THE GRADUATE COLLEGE

FEBRUARY 1994

WE HEREBY RECOMMEND THAT THE THESIS BY

UN-KU MOON

ENTITLED LINEARITY IMPROVEMENT TECHNIQUE

FOR CMOS CONTINUOUS-TIME FILTERS

BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR

THE DEGREE OF DOCTOR OF PHILOSOPHY

Director of Thesis Research

Head of Department

Committee on Final Examination†

Chairperson

† Required for doctor's degree but not for master's.

O 517

LINEARITY IMPROVEMENT TECHNIQUE FOR CMOS CONTINUOUS-TIME FILTERS

Un-Ku Moon, Ph.D.
Department of Electrical and Computer Engineering
University of Illinois at Urbana-Champaign, 1994
Bang-Sup Song, Advisor

A linearity improvement technique using a combination of passive resistors and current-steering MOS transistors as a variable resistance element is applied in the implementation of low-distortion continuous-time filters in complementary metal-oxide-semiconductor (CMOS) technology. This work is motivated by the fact that to date, most of the techniques in continuous-time, electronically tunable filters perform quite poorly in linearity. The proposed technique relies on the linearity of the passive resistors and the tunability of the current-steering MOS transistors operating in the triode region. By novel application of systematic feedback loops and by placing the nonlinear elements inside the feedback, the distortion resulting from the nonlinear devices is greatly reduced by the filter loop gain. Theoretical and experimental results, in agreement, show a significant improvement in linearity. For an audio-band (22-kHz) fifth-order Bessel filter implementation, linearity better than -90 dB THD is demonstrated given a 2 kHz, 4 V_{p-p} signal in a 5-V system. The filter implementation includes a simple and novel automatic frequency-tuning method, which employs a switched-capacitor reference resistor instead of applying a conventional phase-locked loop technique or its variations. Also included in the filter implementation is a linear programming approach to optimize the dynamic range, under the constraint of a fixed capacitor area that is assumed to be the dominant factor in the total chip area.

ACKNOWLEDGMENTS

I would like to thank Professor Bang-Sup Song, my advisor, for his close and insightful guidance throughout the course of my Ph.D. studies. His standards were the best in the field and his insights were always correct. I hope I have become a highly effective engineer and a better person as a whole because of the knowledge and experience that I have gained working with him.

I also thank Professors Ibrahim Hajj, Douglas Jones, and Sung Mo Kang, my committee members, for their generous availability and kind patience. My special thanks to Professor Jones for his encouragement and enthusiasm throughout my studies. I especially appreciated his consideration of my well-being at the personal level.

I appreciate the help of Paul Ferguson and his team at Analog Devices, Seung-Hoon Lee at Sogang Unversity, Korea, for the use of IC layout and circuit simulation tools, and Pat Rakers and Christ Lash at Motorola for testing of my prototype IC.

I extend thanks to my officemates and to everyone in the Digital and Analog Circuits group in the Coordinated Science Laboratory. I could not have completed my work without their support. I have benefited much from the discussions with Seung-Hoon Lee, Eric Shu, and Kevin Kwak. The practical help that I have received from Terry Lee, George Stamoulis, and Carolyn Genzel was significant.

Much credit is due to my family members for their continued interest and some healthy pressure to keep me going. My heartfelt appreciation goes to my deceased father Mugil

Moon who taught me valuable and absolute principles in life by the example of his overwhelming joy and deepest appreciation for daily living, and to my beloved mother Ducleon Chun who has demonstrated to me her unconditional love.

Thanks to my immediate friends who are close by and elsewhere, and to the Body of Christ with a particular gratitude towards the local Christian and Missionary Alliance church members and the people of Campus Crusade for Christ. They have fostered me, comforted me, fed me, and prayed for me.

Many thanks to my best friend Kathleen Schirra for her genuine care and understanding. Her words have lightened my spirit and brought the broad view of life back in perspective.

Finally, full and complete credit is due my Father in Heaven, for all the blessings that I hold today. The words of Jesus ”For what shall it profit a man, if he shall gain the whole world, and lose his soul?” have newly established the deepest meaning in my life.

TABLE OF CONTENTS

CHAPTER **PAGE**

CHAPTER 1

INTRODUCTION

The history of electrical filters, dating back to about 1915, reveals many drastic changes in the design approaches as well as the advancement of available technology [1]. This has yielded many sophisticated and clever designs leading to highly efficient (economically as well as electrically) and accurate filters. Perhaps one of the major shifts in the design of electrical filters was established by Sallen and Key in the 1950s when the design of active RC filters was made feasible using low-gain amplifiers [2]. The design of active RC filters using high-gain operational amplifiers (op amps) followed [3]-[5], and by the early 1970s Hybrid Integrated Circuit (HIC) active filters were made [6]-[8]. By this time a major achievement in reducing the size and the cost of electrical filters was established by the complete elimination of the large inductors that were essential in general LC filters. Many intriguing design techniques were also used in an attempt to avoid the use of inductors. Such techniques include the gyrator [9]-[14], the Frequency-Dependent Negative Resistor (FDNR) [15]-[18], and Negative Impedance Converter (NIC) [19]-[21].

1.1 Motivation

Today, as nearly all filter implementations are realized in monolithic ICs as some form of an active filter (e.g., RC, Gm-C, and MOSFET-C), the size reduction and the integratability of these filters have now made them a very economical and electrically desirable solution. With ever-increasing levels of integration, many system designs are placed on

a single chip, and fully integrated active filters have practically become a “standard cell.” While thriving on the great advantages of monolithic ICs, filter design faces a few obstacles. One of the most critical issues in practical applications is the RC time-constant variation (inversely proportional to the -3 dB corner frequency) due to process variation, temperature drift and aging. At extreme conditions, the integrated filter can vary up to a maximum of $\pm 50\%$ in the -3 dB corner frequency [27], [28].

The continuous-time filter approach typically compensates for this problem with the “tunable” filter, by electronically varying the time-constant which defines the -3 dB corner frequency of the filter. However, these designs have the drawbacks of significant nonlinearities introduced by the tunable element and unwanted control voltage feedthrough which appears transposed on the output signal. The switched-capacitor filter approach, on the other hand, avoids this time-constant variation problem by relying on the product of capacitor ratios and the reference clock, which can be a highly accurate crystal oscillation frequency. But switched-capacitor filters are not necessarily ideal because they inherently implement a discrete-time filter which generally requires analog anti-aliasing and/or smoothing filters.

The work to be described herein focuses on overcoming the RC time-constant variation by investigating a tunable continuous-time filter that is nearly free from the influence of the nonlinearities typically resulting from tunable elements. Also, a unique filter tuning method will be used which greatly simplifies the implementation and minimizes the control voltage feedthrough to a negligible amount.

1.2 Existing Continuous-Time Filters

Numerous design techniques have been proposed to improve the linearity while trying to maintain the tunability of continuous-time filters. Many schemes attempt to "linearize" the inherently nonlinear components [22]-[40]. Most of the filter design techniques fall into a few categories: (i) filters using variable transconductance stages as tunable elements; (ii) transconductance stages composed of fixed transconductance/resistance in combination with a current steering (typically a multiplier) block for tuning; and (iii) wafer trimmed or electronically (digitally) trimmed resistors and capacitors which define the -3 dB corner frequency of the filter. Some filters have employed a combination of the above techniques for an extended frequency tuning range (usually an additional digital tuning capability for "gear shifting" or "zoning") [30], [32].

Despite the enhancements and drawbacks of these techniques, the common underlying problem is the limited linearity performance. Even though the class (iii) filters are less likely to suffer from this linearity problem, a wafer trimming process can be very expensive if precise components such as laser-trimmed thin-film resistors are used. For the case of electronic (digital) trimming of multiple resistors and capacitors, the chip area must accommodate a growing number of components as the tuning range is increased and the resolution of the step size is made smaller. A recent result of a straightforward digital trimming method demonstrates exceptionally high linearity performance by trimming weighted capacitors in parallel [27]. Automatic tuning maintains a fixed -3 dB corner frequency of the filter. Despite the high linearity performance of this filter, switching of the energy stor-

ing elements prohibits the presence of signal while the digital tuning is being performed. No detailed analysis of the transient effects of this kind of signal modulation has been reported. On the other hand, this kind of analysis could prove to be unnecessary if the filter is trimmed only at certain allowed time slots. In any event, the signal is either modulated by the digital switching, or the operation of the filter has to be interrupted to create these regular time slots for the frequency tuning. The best option, if feasible, would be to avoid this problem all together.

Among the various forms of electronically tunable filters under class (i), MOSFET-C filters in particular have become well-known, partly because of their simplicity. They are easily implemented with operational amplifier blocks while maintaining close architectural similarities to an active RC filter [26], [28]. These MOSFET-C filters, implemented in a standard CMOS process, utilize the linearized model behavior of an MOS transistor operating in the triode region instead of a passive resistor. Devices such as these have been proposed as linear tunable resistor elements in monolithic integrated circuits [26], [28], [41]-[44]. However, due to the mismatch and the inherent nonlinear behavior of a MOSFET in triode, THD in the range of only 40-60 dB has been achieved with a volt-level signal swing in a single 5-V system. With an on-going interest in building highly linear tunable continuous-time filters, and given the existing switched-capacitor filters that demonstrate good linearity performance [45], [46], it is desirable to investigate new options for improving linearity that can provide a very low distortion continuous-time tunable filter in a standard CMOS technology.

1.3 Proposed Work

In comparison to the well-known MOSFET-C filter, the linearity improvement technique herein moves the nonlinear transconductance element inside a feedback loop for a significant improvement of distortion. This systematic feedback approach greatly suppresses the distortion originating from the inherently nonlinear components. Furthermore, the actual voltage swing applied to the nonlinear elements is scaled down for operation more closely within their linear range. This voltage-scaled portion will be referred to as the R-MOSFET variable resistor, which can be generally applied in any analog signal processing (i.e., multiplier/divider and integrator).

In conjunction with the linearity improvement technique, this work also includes an automatic tuning method which utilizes an accurate switched-capacitor reference resistor instead of the conventional phase-locked-loop methods, and dynamic range optimization via linear programming which operates under a fixed chip-area constraint. Even though this thesis considers only a specific, narrow application, these two additional methods can be applied in any kind of design for a continuous-time filter with a self-tuning feature.

CHAPTER 2

LINEARITY IMPROVEMENT

A novel yet delightfully simple approach for substantially improving the linearity of a tunable resistor, referred to as the R-MOSFET, and an integrator/filter implementation, referred as the R-MOSFET-C, will be presented in this chapter. Many previous efforts attempt to cancel the nonlinear effects by mathematical approaches such as adding or subtracting unwanted harmonics by additional linearity correction circuits or by exploiting creative symmetries and arrangements of nonlinear devices. It will be shown that the R-MOSFET/R-MOSFET-C technique evolves from a more global, systematic approach of scaling (reducing) the voltage swing across nonlinear components and of placing all nonlinear components inside feedback loops for reduction of distortion.

2.1 R-MOSFET Linearity-Improved Variable Resistor

The final implementation of the R-MOSFET variable resistor is best described starting from the standard MOSFET resistor (MOSFET operating in the triode region) shown in Fig. 2.1. The common node (ground) indicates the location of the summing nodes of an operational amplifier (op amp) when the variable resistor is used in conjunction with an op amp with a feedback network. Some typical arrangements are the multiplier (resistive feedback) and the integrator (capacitive feedback) configurations. Many successful analyses, designs, and IC implementations have been based on the MOSFET resistor shown in Fig. 2.1. In reality, however, given the desire to build a highly linear variable resistor, this

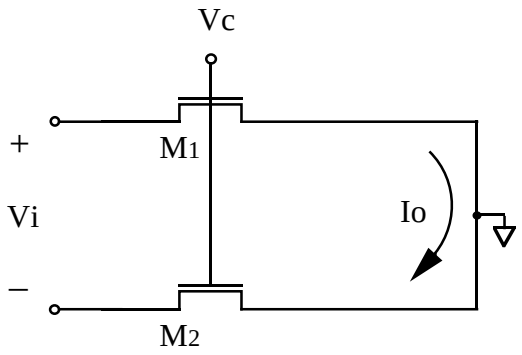


Figure 2.1 MOSFET Resistor

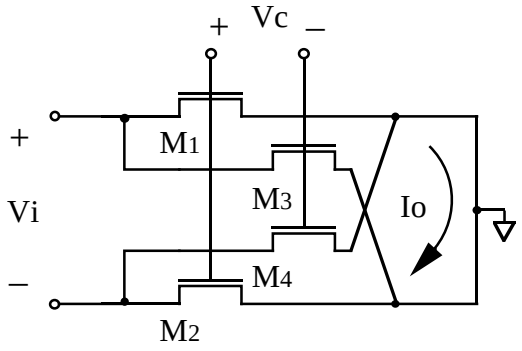


Figure 2.2 Cross-Coupled MOSFET Resistor

MOSFET resistor suffers from device ratio (W/L) mismatch, mobility (μ) mismatch, and threshold voltage (V_{th}) mismatch, all of which contribute to the nonlinearity of this variable resistance stage. Even with much effort placed in the design and careful layout for good matching and linearity, the linearity is limited to about -60 dB total harmonic distortion (THD).

A nice improvement, at least in theory, can be made to the MOSFET resistors by cross-coupling them with additional transistors as shown in Fig. 2.2. This technique is found in [41]-[44]. Without getting into the detailed analysis derived in [44], it is sufficient to note

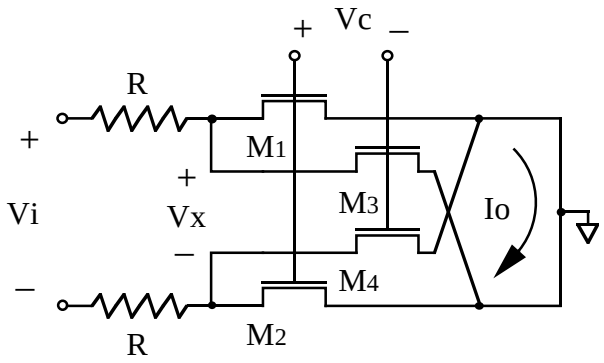


Figure 2.3 R-MOSFET Resistor

that this cross-coupled setup compensates for the threshold voltage variation in the transistors [41], and under a perfect matching condition even the odd harmonics are cancelled in theory [44]. But just as in the setup of the two single MOSFET resistors, this cross-coupled stage also suffers from the device ratio mismatch and the mobility mismatch. Because of these limitations, what is very attractive (actually ”perfect”) in theory cannot in reality perform to expectation. The linearity performance should be better, but given the increased number of variances (more transistors) and the limitation of the mismatch, the linearity performance still cannot exceed the -60 dB THD ceiling [43].

Realizing the advantageous current-steering capability for tuning implemented in the cross-coupled stage, even greater improvements can be made. Shown in Fig. 2.3 is the R-MOSFET variable resistor. The current-steering capability of the cross-coupled MOSFETs is used for tuning but most of the input voltage is dropped across the passive resistors. The total nonlinearity due to this stage is then approximately proportional to the amount of voltage swing across the nonlinear elements, labeled in the figure as V_X. This kind of *scaling* of the input voltage is simply the direct result of a local feedback, identical to the

well-known emitter degeneration in the Bipolar Junction Transistor (BJT).

To compare the similarity and the distinction between the cross-coupled MOSFET stage and the R-MOSFET stage, the equations for the first-order variable resistances are first identified. The current-steering cross-coupled MOSFET stage of Fig. 2.2 has an equivalent resistance given by

$$R_{eq} = \frac{1}{G_{1,2} - G_{3,4}} = \frac{1}{KV_C}, \tag{2.1}$$

where G_i is the triode region channel conductance of M_i defined by

$$G_i = \mu_i C_{OXi} \frac{W_i}{L_i}(V_{GSi} - V_{thi}) = K_i(V_{GSi} - V_{thi}). \tag{2.2}$$

Each subscript for K_i is in place simply to denote the fact that the devices are mismatched, but we may simply consider the average intrinsic transconductance of the four transistors M_1, M_2, M_3 and M_4 as K. Equation (2.1) implies that the equivalent conductance is linearly controlled by the control voltage V_C.

The improved version of this, the R-MOSFET stage as shown in Fig. 2.3, has a very similar expression describing the linear control of the variable resistance (inherently conductance). This R-MOSFET stage has an equivalent resistance of

$$R_{eq} = \frac{1}{G_{1,2} - G_{3,4}} F = \frac{F}{KV_C}, \tag{2.3}$$

where the voltage scale factor, F, is defined by

$$F = \frac{V_i}{V_X} = 1 + 2\overline{G}R, \tag{2.4}$$

and the average conductance of M_1, M_2, M_3 and M_4 is

$$\overline{G} = \frac{(G_{1,2} + G_{3,4})}{2}. \tag{2.5}$$

This yields the appropriate design value for the voltage scale factor, F, because the quantity $2\overline{G} = (G_{1,2} + G_{3,4})$ represents the equivalent conductance of the MOSFETs in parallel combination seen at V_X. As a result of the voltage scaling given by (2.4), the distortion improves as the signal swing across the MOSFETs decreases. Unlike the conventional balanced resistor (cross-coupled MOSFETs) which relies on transistor matching for high linearity, given the unavoidable level of imperfect balance and device mismatches, the R-MOSFET stage systematically improves linearity in proportion to the amount of voltage scaling. The MOSFET devices in this arrangement can be viewed as current-steering devices, operating in the triode region, rather than as "resistors."

2.1.1 R-MOSFET multiplier/divider

One of the analog signal processing applications of this linearity-improved R-MOSFET stage is the highly linear multiplier, divider, or multiplier-divider combination. The arrangement of the multiplier-divider combination is shown in Fig. 2.4. With an R-MOSFET variable resistor as the input resistor to an op amp with another R-MOSFET resistive feedback network, both multiplication and division are performed. Assuming that the amount of voltage scaling (the ratio between the voltage swing across the whole R-MOSFET combination and the MOSFET portion) is fixed for the both sets of R-MOSFET stages, the overall transfer function is given by

$$V_o = \left(\frac{R_2}{R_1}\right) \frac{V_{\mathrm{X}} V_y}{V_z}. \tag{2.6}$$

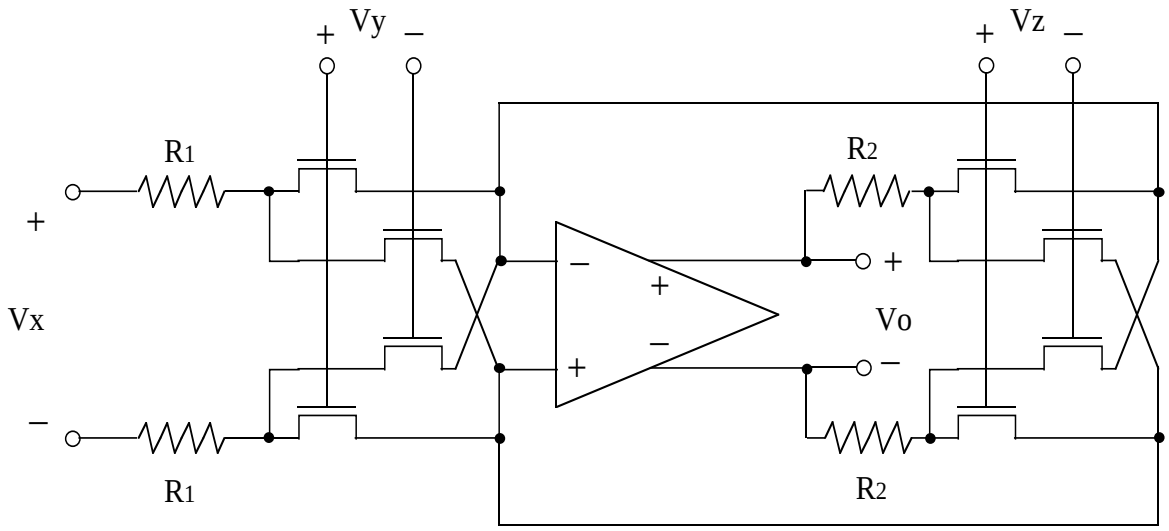


Figure 2.4 R-MOSFET-R Multiplier/Divider

The input V_X and the two control voltages V_y and V_z form a diverse multiplication-division relationship. As discussed before, the linearity of this multiplier-divider combination is improved by the voltage scale factor, F, in comparison to the implementation using standard cross-coupled MOSFETs as the tunable resistor.

Observing the multiplier transfer function as shown in Fig. 2.5, isolating the V_X for input and the V_y control voltage for gain (V_z is fixed), one can see visually the distinct linearity improvement for the R-MOSFET multiplier (dotted lines) in comparison to the standard cross-coupled MOSFET multiplier (solid lines). The proper operation of the R-MOSFET multiplier in the time-domain is also displayed in Fig. 2.6. The amplitude-modulated signal

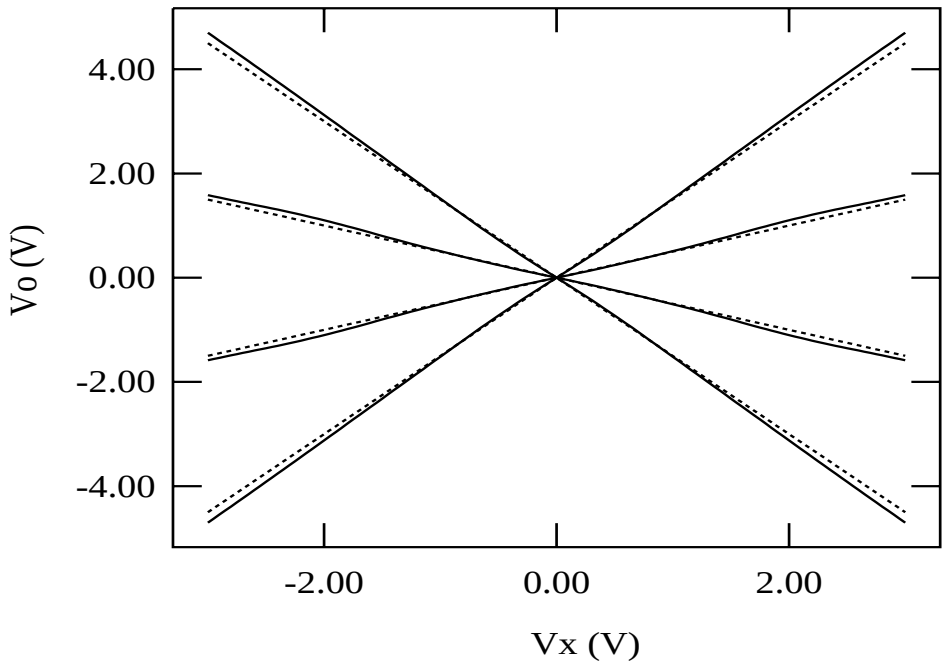


Figure 2.5 Multiplier Transfer Characteristic

at the output V_o is due to the presence of a triangular-wave gain-control voltage at V_y and a sinusoidal input at the input V_{X}.

Observing the multiplier transfer function in a similar setup isolating V_z and V_y (V_{X} fixed) produces the divider transfer function shown in Fig. 2.7 for multiple control voltages at V_y. For the display of the time-domain operation, a sinusoidal input at V_{X} is modulated by the control of the triangular wave at V_z. The result is shown in Fig. 2.8. In this case the triangular-wave control voltage does not cross zero in order to keep a finite gain from the input V_{X} to the out V_o. Thus these simulation results confirm the convenient feasibility of a linearity-improved R-MOSFET multiplier/divider.

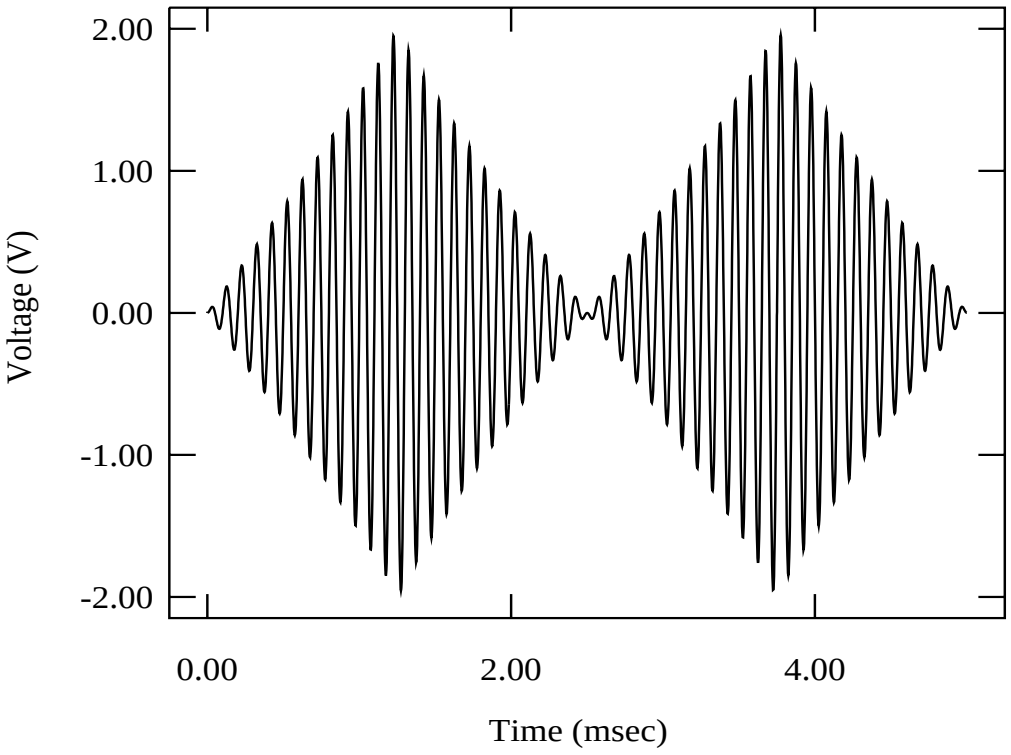


Figure 2.6 Multiplier Operation in Real Time

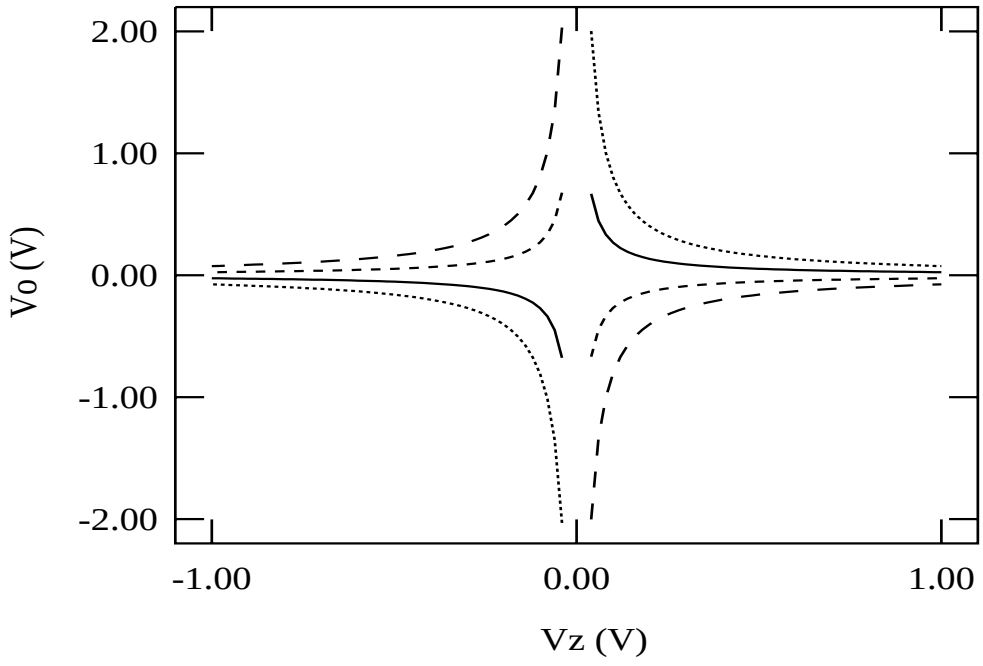


Figure 2.7 Divider Transfer Characteristic

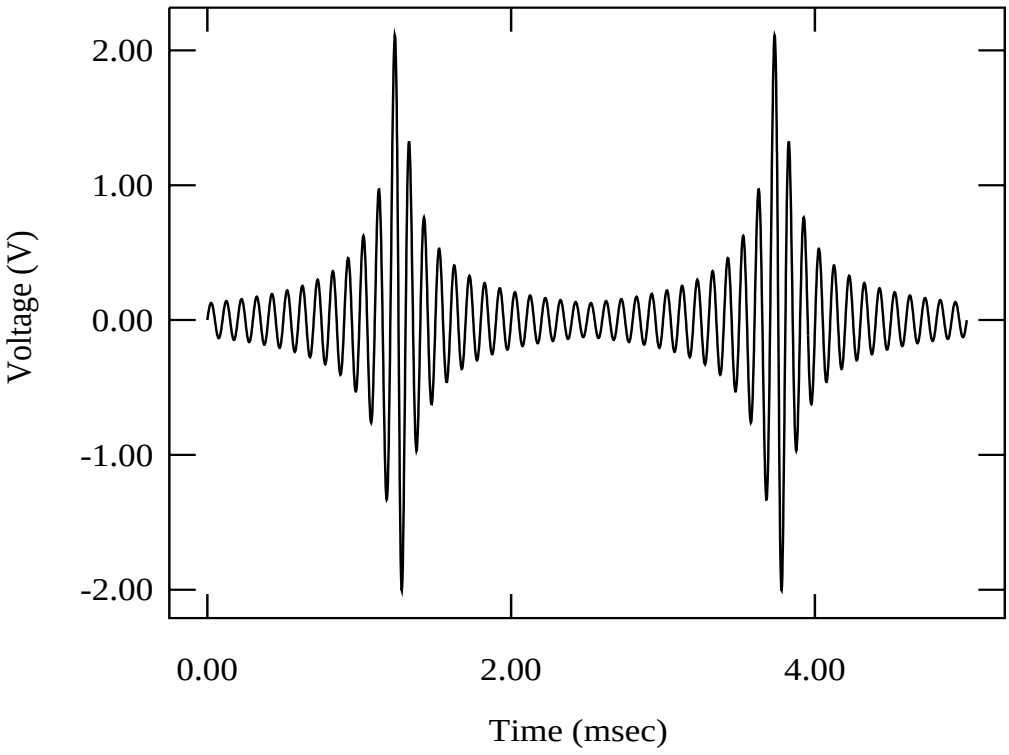


Figure 2.8 Divider Operation in Real Time

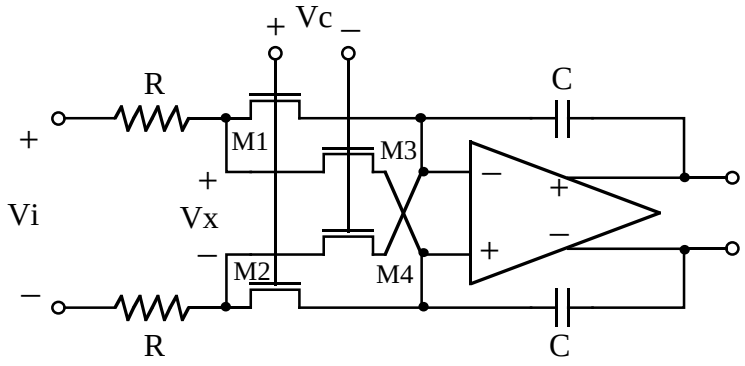


Figure 2.9 Improved R-MOSFET-C Integrator

2.2 R-MOSFET-C Linearity-Improved Integrator

A typical Miller capacitance integrator is formed by combining a variable resistor circuit block with an op amp with feedback capacitors. In the same way, an R-MOSFET-C integrator is formed by using the R-MOSFET variable resistor as shown in Fig. 2.9. This configuration contains the identical variable resistor of Fig. 2.3 and behaves just as described in Equations (2.3)-(2.5). In addition, the integrator displays a linearly controlled unity-gain frequency

$$\omega_{unity} = \frac{G_{1,2} - G_{3,4}}{FC} = \frac{KV_C}{FC}. \tag{2.7}$$

This integrator function is closely related to the standard MOSFET-C integrator in Fig. 2.10. This MOSFET-C integrator behaves identically to the R-MOSFET-C without the added voltage scaling by F, as shown in comparison in Equations (2.1)-(2.2) and (2.3)-(2.5), for the MOSFET resistor and the R-MOSFET resistors, respectively. Thus, the MOSFET-C integrator shown in Fig. 2.10 also displays a linearly controlled unity-gain frequency

$$\omega_{unity} = \frac{G_{1,2} - G_{3,4}}{C} = \frac{KV_C}{C}. \tag{2.8}$$

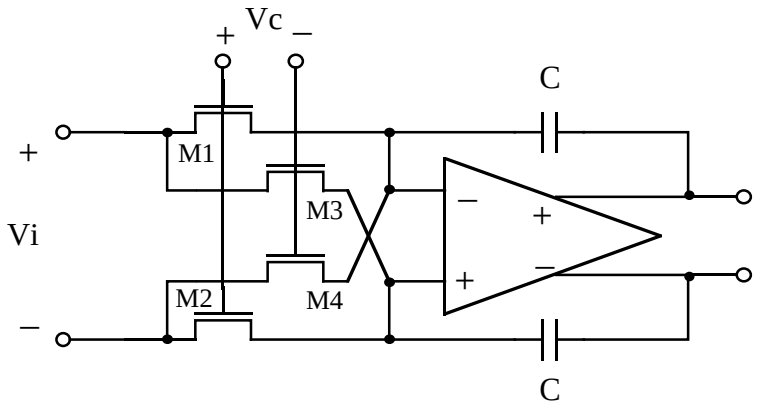


Figure 2.10 Balanced MOSFET-C Integrator

2.2.1 Current-dumping configuration

Although the *criss-cross* integrator of Fig. 2.9 has a desirable symmetry in generating a more linear input resistance, it reduces the effective dc gain and bandwidth of the integrator and enhances the unity-gain frequency sensitivity to component mismatches. In addition to the filter's overall performance error due to the lower effective gain and bandwidth [47], [48], and the increased sensitivity [44], another practical limit is an increase in noise due to low-resistance paths between the summing nodes of the operational amplifier. That is, equivalent current noise generators in the low resistance paths degrade the dynamic range of the filter. As a result, a slight modification on this topology is made to improve the noise performance as shown in Fig. 2.11.

In this *current-dumping* configuration, the bypassing current from the input is not fed to the opposite side but dumped to the ground (conceptually in a single-ended configuration) instead. The advantage of this arrangement is approximately an increase by a factor of four in the resistance between the summing nodes of the operational amplifier. Deferring

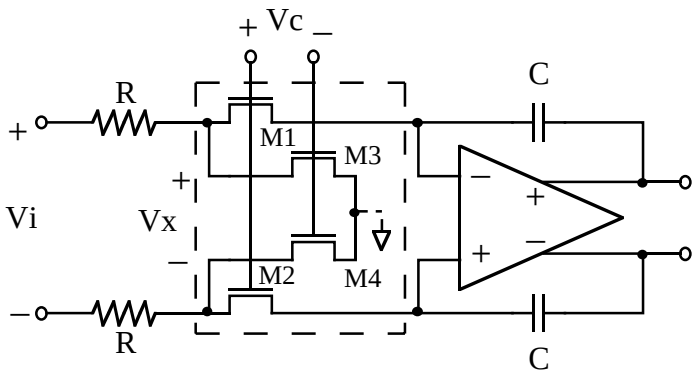


Figure 2.11 Improved Current-dumping R-MOSFET-C Integrator

detailed analysis of the current-dumping integrator to the following section, simple inspection of the criss-cross (Fig. 2.10) and the current-dumping (Fig. 2.11) integrators indicates that the resistances between the summing nodes of the op amp, $R_{(+/-)}$, are approximately $(R_{1,2} + R_{3,4})/2$ and $2(R_{1,2} + R_{3,4})$ for the criss-cross and the current-dumping integrators, respectively. (Note the implied notations $R_{1,2} = 1/G_{1,2}$ and $R_{3,4} = 1/G_{3,4}$.) This improvement for the current-dumping integrator comes with a slight sacrifice in the balance of the electrical symmetry at the variable resistance cell. In reality, the symmetry is not as critical in the linearity-improved filter implementation because the set of MOSFETs is merely being used as a current-steering element with a small voltage swing across it.

Due to this modification, Equations (2.3) and (2.7) are also modified as follows for the current-dumping integrator.

$$R_{eq} = \frac{F}{G_{1,2}} = \frac{F}{K\hat{V}_C} \quad \text{and} \tag{2.9}$$

$$\omega_{unity} = \frac{G_{1,2}}{FC} = \frac{K\hat{V}_C}{FC}, \tag{2.10}$$

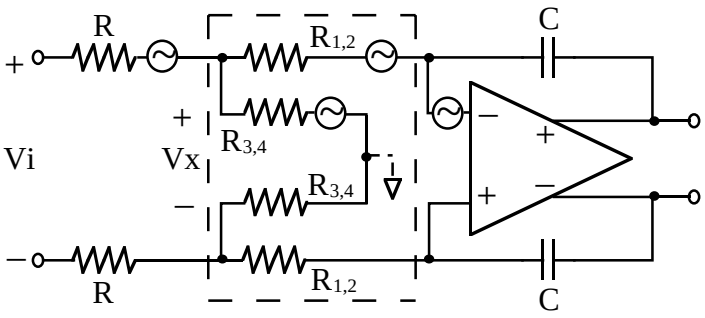


Figure 2.12 Independent Noise Sources

where

$$\hat{V_C} = \frac{V_C}{2} + (V_{CM} - V_{th}) \text{ and } V_{CM} = \text{common-mode control voltage.}$$

The added component of the controlling voltage function is that the common-mode portion of the control voltage appears as a dc offset in the unity-gain frequency control. The range of the control voltage V_C has simply been shifted and stretched from the 0 to $V_{C,peak}$ range for Equation (2.7) to a -$V_{C,peak}$ to $V_{C,peak}$ range for Equation (2.10).

2.2.2 Noise considerations

Studying the sources of noise in detail for the current-dumping configuration of Fig. 2.11 (the resistors, MOSFETs, and the operational amplifier), the integrator is first analyzed by recognizing the independent noise sources as shown in Fig. 2.12. At low frequencies, the equivalent input referred noise of the current-dumping integrator is given by

$$\frac{\overline{V_{eq}{}^2}}{\Delta f} = 4kT \left\{ 2R + \left(\frac{R}{R_{3,4}} \right)^2 2R_{3,4} + \left(\frac{R + R_{3,4}}{R_{3,4}} \right)^2 (2R_{1,2} + R_i) \right\}, \qquad (2.11)$$

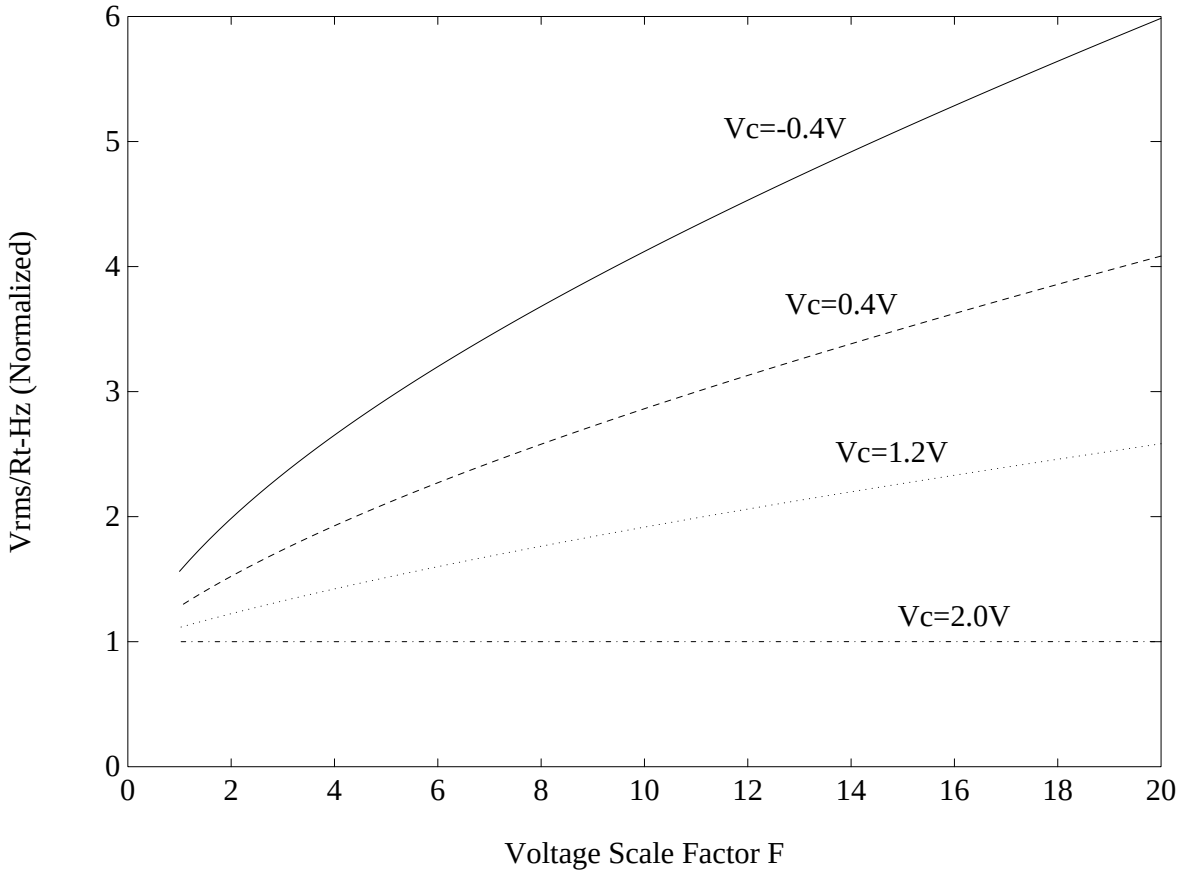


Figure 2.13 Input Referred Noise vs. F

where R_i is an equivalent input noise resistance of the op amp. For an ordinary active RC filter, the equivalent input referred noise would be simply

$$\frac{\overline{{V_{eq}}^2}}{\Delta f} = 4KT[2R_{eq} + R_i] = 4KT[2R_{1,2}F + R_i]. \tag{2.12}$$

To observe the effects of the control voltage V_C and the voltage scaling factor F on noise, the normalized rms noise referred to input is plotted in Figs. 2.13 and 2.14, where rms noise referred to the input for a conventional active RC filter corresponds to F=1. Figure 2.13 shows that noise increases as the voltage scale factor, F, increases according to (2.11), because the input series resistor R increases in comparison to the MOSFET parallel

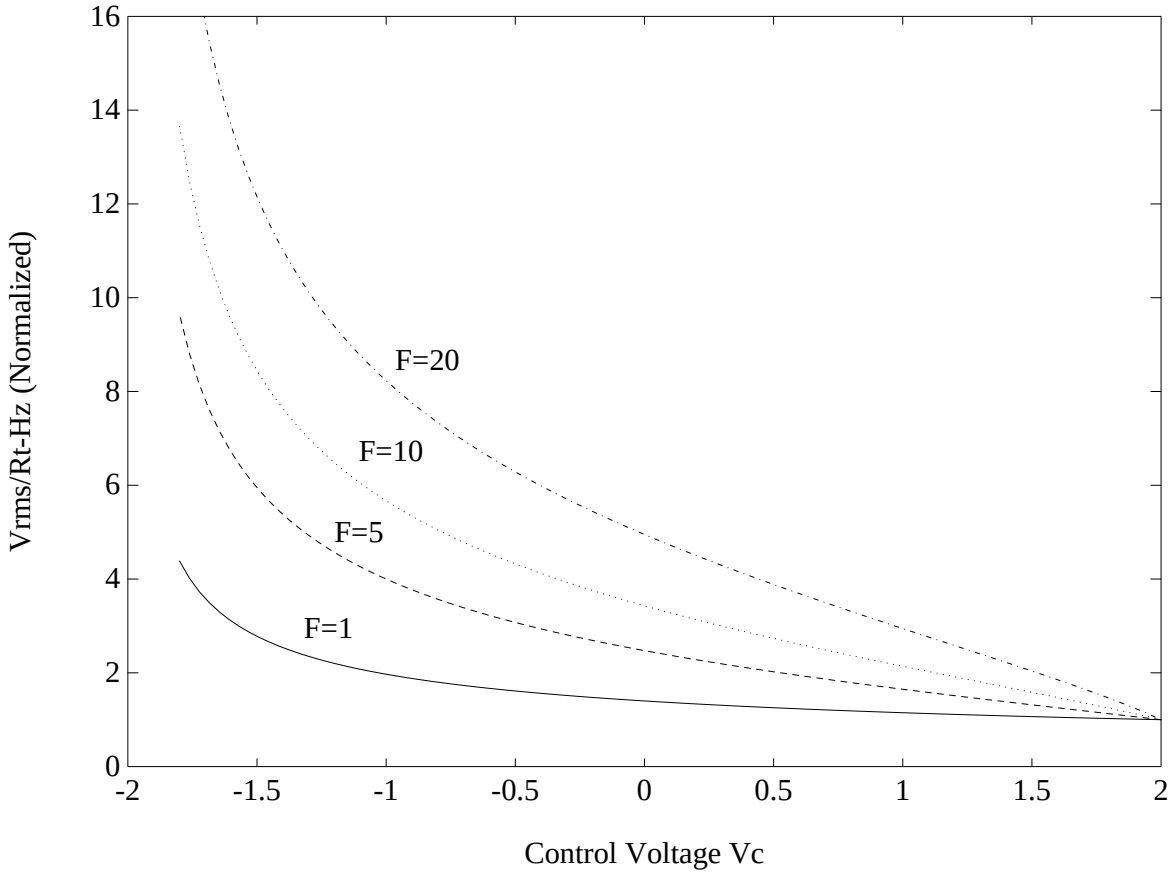


Figure 2.14 Input Referred Noise vs. Vc

combination $R_X = R_{1,2}||R_{3,4}$. The noise dependence with respect to the control voltage V_C is shown in Fig. 2.14, where the decrease in V_C implies decreasing $R_{3,4}$ in comparison to $R_{1,2}$. The understanding of these trends in noise characteristics, which are a function of F and V_C, is important in making the right trade-offs in the design. Since the linearity improves as the dynamic range is degraded with an increasing voltage scale factor F, a linearity versus noise trade-off is necessary in the design when choosing an optimum value for F.

Another way of scaling the input voltage swing has been suggested in [28] where the input is pre-divided by a factor (3 in their setup) and the output is post-multiplied by the same factor to reduce distortion. This kind of input scaling directly trades off THD with S/N. For example, an effective voltage scaling of F=5 would experience 14 dB noise increase, while improving linearity by approximately the same amount. Observation of Figs. 2.13 and 2.14 suggests that the noise increase due to the voltage scaling of F=5 is about 5 dB for the worst case. For the prototype filter implemented, using a set of varied voltage scaling factors F=2.5-5 (discussed in Chapter 5), the noise increase due to this technique is about 2.3 dB in simulation as shown in Fig. 2.15. This result comes from the worst-case condition for a tuning range of $\pm$50%. Considering a very significant reduction of distortion by feedback loop gain (detailed discussion will follow in Section 2.3), this relatively higher noise floor can be offset by the larger undistorted signal that this technique provides.

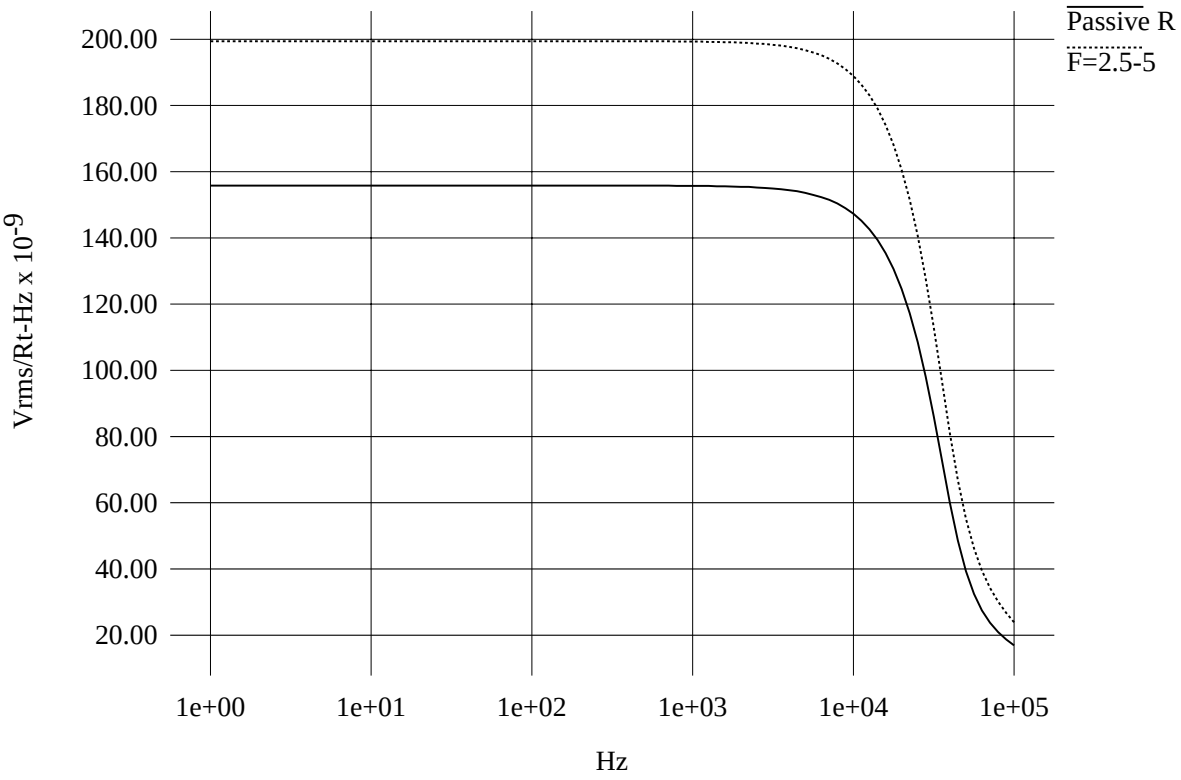


Figure 2.15 Eq Noise at the Output (F=2.5-5)

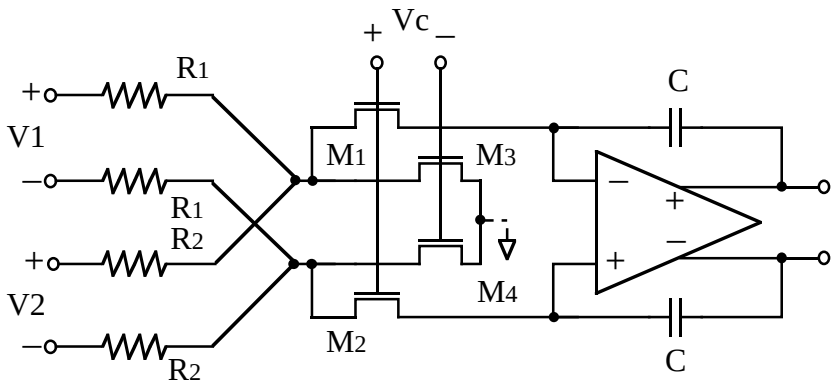


Figure 2.16 Multiple-input Balanced Integrator

2.2.3 Multiple-input integrator

In the case of a multiple-input implementation for the integrator, the inputs are arranged with multiple resistors but with only one current-steering quad (four MOSFET devices operating in the triode region) per integrator. The implementation for a dual-input setting is shown in Fig. 2.16.

It would seem natural that each resistor in a standard active RC integrator should be replaced by an R-MOSFET variable resistor combination as shown in the first step of Fig. 2.17. However, the tunable current-steering portion (the “MOSFET quad” in the differential setting) becomes redundant for the multiple inputs and can be simplified to only a single current-steering set. This change is noted in the second transition (step two) of Fig. 2.17. Even though the simplification at this point appears only to have reduced the number of transistors, it will be shown in the following section that this simplification allows the nonlinear tunable elements to reside in a feedback loop in the R-MOSFET-C filter implementation. The net result is a proportionally significant amount of linearization by the

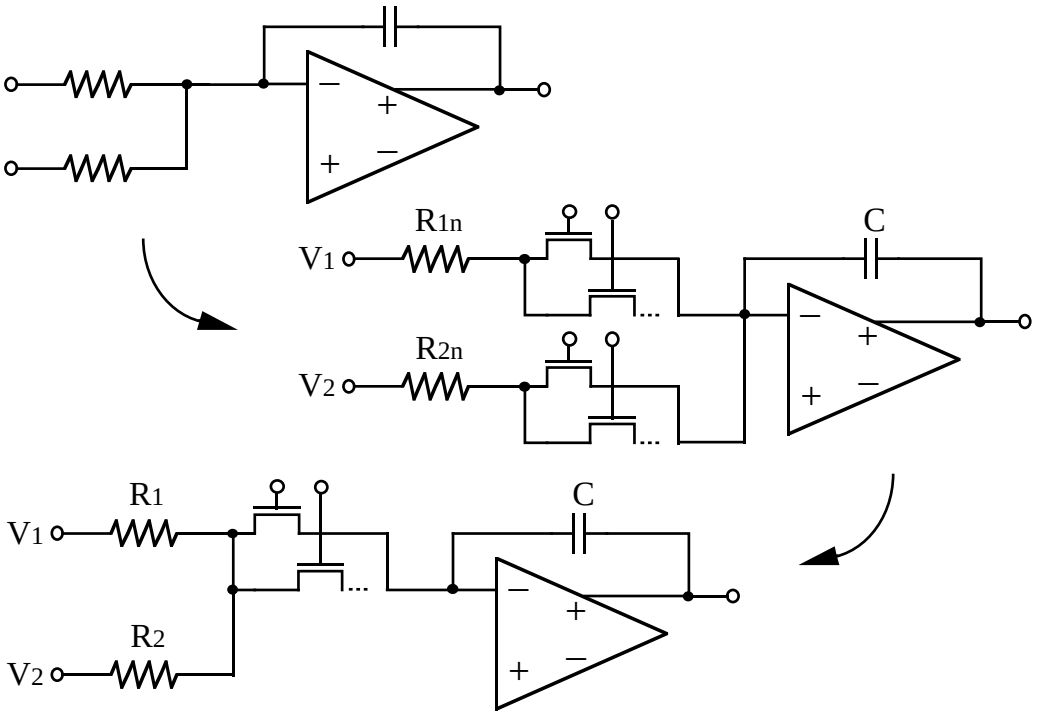


Figure 2.17 Multiple-input RC to R-MOSFET-C

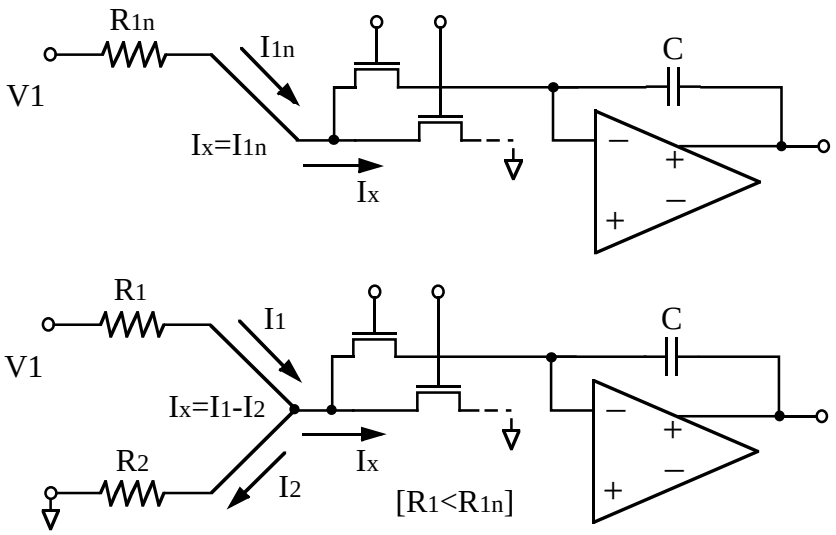


Figure 2.18 Dual-input Loading Effect

amount of the loop-gain in placing the nonlinear components in a feedback loop.

While the simplification and reduction of the tunable elements are quite naturally arranged for the multiple-input setting, an appropriate loading effect of the multiple inputs should be taken into account when the resistor values are chosen. As illustrated in Fig. 2.18 for the dual-input setting, because of the extra loading of the second input, a fraction of the input current I_1 is subtracted before the current flows through the MOSFETs. Only for the single-input integrator, the current I_{1n} coming from the resistor R_{1n} flows directly into the tuning elements (MOSFETs) as the current I_{X}. The amount of current that flows through the MOSFETs, I_{X}, is the net current $I_1 - I_2$. Thus the loading effect calls for a reduced input passive resistor R_1 from the original value R_{1n}.

Analysis of the loading effect of a dual-input stage shows that the actual resistances, R_1 and R_2, are related to the nominal values of R_{1n} and R_{2n} by

$$R_1 = R_{1n}\frac{1 - S_{1n}S_{2n}}{1 + S_{2n}} \text{ and } R_2 = R_{2n}\frac{1 - S_{1n}S_{2n}}{1 + S_{1n}}, \tag{2.13}$$

where the constants are

$$S_{1n} = \frac{1}{2\overline{G}R_{1n}} \text{ and } S_{2n} = \frac{1}{2\overline{G}R_{2n}}.$$

Similarly for a triple-input stage, the actual resistances R_1, R_2, and R_3 are

$$\begin{aligned} R_1 &= R_{1n}\frac{1 - S_{1n}S_{2n} - S_{1n}S_{3n} - S_{2n}S_{3n} - 2S_{1n}S_{2n}S_{3n}}{1 + S_{2n} + S_{3n} + S_{2n}S_{3n}}, \\ R_2 &= R_{2n}\frac{1 - S_{1n}S_{2n} - S_{1n}S_{3n} - S_{2n}S_{3n} - 2S_{1n}S_{2n}S_{3n}}{1 + S_{1n} + S_{3n} + S_{1n}S_{3n}}, \text{ and} \\ R_3 &= R_{3n}\frac{1 - S_{1n}S_{2n} - S_{1n}S_{3n} - S_{2n}S_{3n} - 2S_{1n}S_{2n}S_{3n}}{1 + S_{1n} + S_{2n} + S_{1n}S_{2n}}, \end{aligned} \tag{2.14}$$

where the constants are

$$S_{1n} = \frac{1}{2\overline{G}R_{1n}}, \; S_{2n} = \frac{1}{2\overline{G}R_{2n}}, \text{ and } S_{3n} = \frac{1}{2\overline{G}R_{3n}}.$$

The derivations for the results above are detailed below. As shown in the dual-input loading condition of Fig. 2.18, the amount of current going into the parallel combination of the MOSFETs, I_{X}, is reduced from the input current I_1. To insure that the current $I_{\mathrm{X}} = I_{1n}$ of the single input condition is preserved for the current $I_{\mathrm{X}} = I_1 - I_2$ of the dual-input loading condition, appropriate adjustments for the passive resistors must be made. Another way to view this required adjustment is that the voltage across the MOSFETs, V_X, for the single input case (we may call this "ideal" since no loading takes place) as well as for the

dual-input case (call this “loading”) is identical in proportion to the input V_1 (i.e., voltage scale factor F is preserved).

First consider the single input “ideal” case. The expression for the voltage across the MOSFETs is

$$V_X = \frac{R_X V_1}{R_X + R_{1n}} = \frac{V_1}{1 + 2\overline{G}R_{1n}}, \tag{2.15}$$

where the parallel combination of the MOSFETs, $R_X = 1/2\overline{G}$, has already been defined in (2.5). Now consider the dual-input “loading” case, in which the voltage across the MOSFETs is given as

$$V_X = \frac{(R_X||R_2)V_1}{(R_X||R_2) + R_1} = \frac{V_1}{1 + 2\overline{G}R_1\left(1 + \frac{1}{2\overline{G}R_2}\right)}. \tag{2.16}$$

From observing (2.15) and (2.16), for the case in which the loading effect of the dual input is compensated completely, the nominal resistance R_{1n} of the single input is equal to $R_1(1 + 1/2\overline{G}R_2)$. Thus we have

$$R_1 = \frac{R_{1n}}{1 + \frac{1}{2\overline{G}R_2}}, \tag{2.17}$$

and a similar derivation yields

$$R_2 = \frac{R_{2n}}{1 + \frac{1}{2\overline{G}R_1}}. \tag{2.18}$$

Because the expressions in (2.17) and (2.18) have to be complete in terms of only the nominal values R_{1n} and R_{2n}, the denominators require further adjustments. Take for example the expression for R_1. The denominator displays a simple expression

$$D_{D1} = 1 + S_2, \tag{2.19}$$

where

$$S_2 = \frac{1}{2\overline{G}R_2}.$$

With additional definitions

$$S_1 = \frac{1}{2\overline{G}R_1}, \quad S_{1n} = \frac{1}{2\overline{G}R_{1n}}, \quad \text{and} \quad S_{2n} = \frac{1}{2\overline{G}R_{2n}},$$

and using Equations (2.17) and (2.18), S_1 and S_2 become

$$S_1 = S_{1n}(1 + S_2) = S_{1n}D_{D1} \quad \text{and} \tag{2.20}$$

$$S_2 = S_{2n}(1 + S_1). \tag{2.21}$$

Expanding (2.19) by replacing terms from (2.20) and (2.21), D_{D1} becomes

$$\begin{aligned} D_{D1} &= 1 + S_{2n}(1 + S_1) \\ &= 1 + S_{2n}(1 + S_{1n}D_{D1}), \end{aligned} \tag{2.22}$$

$$D_{D1} = \frac{1 + S_{2n}}{1 - S_{1n}S_{2n}}. \tag{2.23}$$

A similar set of derivations leads to the denominator corresponding to the second input:

$$D_{D2} = \frac{1 + S_{1n}}{1 - S_{1n}S_{2n}}. \tag{2.24}$$

Placing (2.23) and (2.24) into (2.17) and (2.18), we have the complete correction terms for the dual-input loading effect expressed in (2.13).

The triple-input loading effect derivation follows a very similar approach, but with extra algebra. Recall that we already have an expression for V_X resulting from the single input "ideal" voltage scaling in (2.15). Now for the the triple-input loading, we have

$$V_X = \frac{(R_X||R_2||R_3)V_1}{(R_X||R_2||R_3) + R_1} = \frac{V_1}{1 + 2\overline{G}R_1\left(1 + \frac{1}{2\overline{G}R_2} + \frac{1}{2\overline{G}R_3}\right)}. \tag{2.25}$$

Extracting resistance relationship from (2.15) and (2.25), the complete compensation of the loading effect becomes

$$R_1 = \frac{R_{1n}}{1 + \frac{1}{2\overline{G}R_2} + \frac{1}{2\overline{G}R_3}}, \tag{2.26}$$

and similar derivations yield

$$R_2 = \frac{R_{2n}}{1 + \frac{1}{2\overline{G}R_1} + \frac{1}{2\overline{G}R_3}} \quad \text{and} \tag{2.27}$$

$$R_3 = \frac{R_{3n}}{1 + \frac{1}{2\overline{G}R_1} + \frac{1}{2\overline{G}R_2}}. \tag{2.28}$$

As before, the denominator has to be further expanded in terms of the nominal resistance values R_{1n}, R_{2n}, and R_{3n}. With the following definitions

$$S_1 = \frac{1}{2\overline{G}R_1}, \quad S_2 = \frac{1}{2\overline{G}R_3}, \quad S_3 = \frac{1}{2\overline{G}R_3},$$

$$S_{1n} = \frac{1}{2\overline{G}R_{1n}}, \quad S_{2n} = \frac{1}{2\overline{G}R_{3n}}, \quad \text{and} \quad S_{3n} = \frac{1}{2\overline{G}R_{3n}}, \tag{2.29}$$

and using (2.26)-(2.29), the resulting set of equations regarding the denominator expansion is

$$D_{T1} = 1 + S_2 + S_3, \tag{2.30}$$

$$S_1 = S_{1n}(1 + S_2 + S_3) = S_{1n}D_{T1}, \tag{2.31}$$

$$S_2 = S_{2n}(1 + S_1 + S_3), \quad \text{and} \tag{2.32}$$

$$S_3 = S_{3n}(1 + S_1 + S_2). \tag{2.33}$$

Combining (2.30)-(2.33),

$$D_{T1} = 1 + S_{2n}(1 + S_{1n}D_{T1} + S_3) + S_{3n}(1 + S_{1n}D_{T1} + S_2)$$

$$
\begin{aligned}
&= 1 + S_{2n}(1 + S_{1n}D_{T1}) + S_{3n}(1 + S_{1n}D_{T1}) \\
&\quad + S_{2n}S_{3n}(1 + S_{1n}D_{T1} + S_2) + S_{3n}S_{2n}(1 + S_{1n}D_{T1} + S_3) \\
&= 1 + S_{2n}(1 + S_{1n}D_{T1}) + S_{3n}(1 + S_{1n}D_{T1}) \\
&\quad + S_{2n}S_{3n}(1 + S_{1n}D_{T1}) + S_{3n}S_{2n}(1 + S_{1n}D_{T1}) \\
&\quad + S_{2n}S_{3n}(D_{T1} - 1). \qquad (2.34)
\end{aligned}
$$

This reduces to

$$
D_{T1} = \frac{1 + S_{2n} + S_{3n} + S_{2n}S_{3n}}{1 - S_{1n}S_{2n} - S_{1n}S_{3n} - S_{2n}S_{3n} - 2S_{1n}S_{2n}S_{3n}}. \qquad (2.35)
$$

A similar set of derivations leads to the denominator expressions corresponding to the second and third inputs

$$
D_{T2} = \frac{1 + S_{1n} + S_{3n} + S_{1n}S_{3n}}{1 - S_{1n}S_{2n} - S_{1n}S_{3n} - S_{2n}S_{3n} - 2S_{1n}S_{2n}S_{3n}} \quad \text{and} \qquad (2.36)
$$

$$
D_{T3} = \frac{1 + S_{1n} + S_{2n} + S_{1n}S_{2n}}{1 - S_{1n}S_{2n} - S_{1n}S_{3n} - S_{2n}S_{3n} - 2S_{1n}S_{2n}S_{3n}}. \qquad (2.37)
$$

Placing these terms (2.35)-(2.37) into (2.26)-(2.28), we have the complete correction terms for the triple-input loading effect as expressed in (2.14).

Looking at the final results of the loading correction terms given in Equations (2.13) and (2.14) and the details of derivations described so far, it seems feasible that general expressions for the correction terms for any number of multiple inputs may be found. Even though this kind of generalization in loading-effect calculation might appear useful at first to the designer in building a multiple-input R-MOSFET stage, most active filter applications require calculations for only the dual-input and the triple-input stages. Specifically,

for the two standard approaches in building active filters, use of multiple biquads and the transformation of an active LC ladder resulting in the "leapfrog" configuration, there are no more than three inputs per integrator. If a special application would arise where more than three inputs are needed, the resources for a similar derivation of the loading effects are already in place. On an interesting note, because the loading effects of these multiple inputs are recursive in nature (the "new" value wanted for the *first* input is a function of the "old" value and the "new" values of the rest of the inputs, each of which needs its "old" value and the "new" values of the rest that include the "new" value of the *first* input), a simple iterative program would do the job in calculating the loading correction terms. Two- or three-input loading effect calculations by the iterative method show fast convergence within a few iterations, and at most ten to twenty iterations for high accuracy.

2.3 Linearity Improvement by Loop Gain

The discussions so far have shown that the linearity improvement technique reduces distortion due to the scaling of the input signal swing by a voltage scale factor F. In an active filter configuration, however, the second input (and third inputs in some cases in the implementation of an active LC ladder transformation) to the integrator forms a feedback loop. Shown in Fig. 2.20 is the linearity-improved version (R-MOSFET-C) of the first-order filter in contrast to the first-order filter using nonlinear MOSFET resistors (MOSFET-C) shown in Fig. 2.19. The topology shown in Fig. 2.20 has a better THD than the conventional topology of Fig. 2.19, because the MOSFETs are operating with a reduced V_{DS}. Furthermore, distortion is improved by a greater factor because the nonlinear components

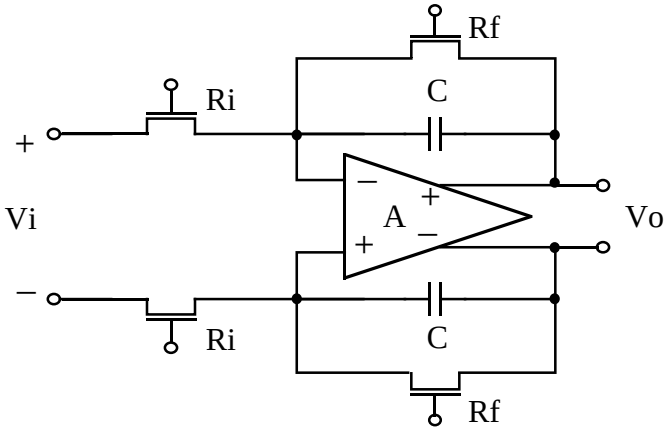


Figure 2.19 MOSFET-C 1st-order Filter

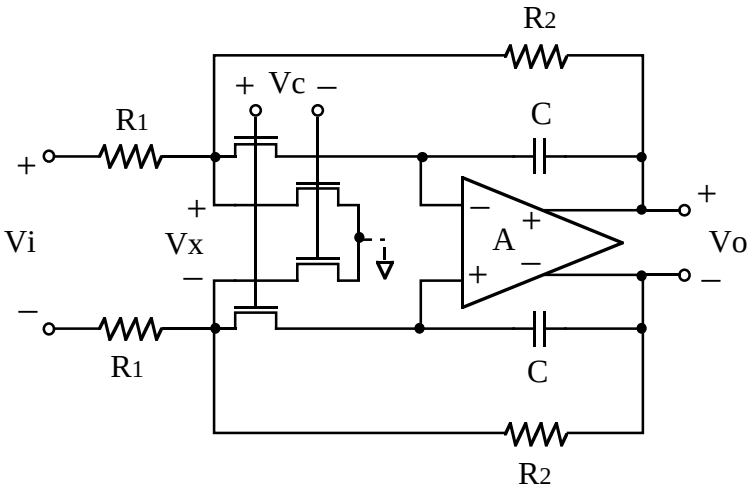


Figure 2.20 Linearity Improvement Technique (1st-order Filter)

(current-steering MOSFETs) are now inside the feedback loop. This is the key concept to be discussed in detail in this section. Under rudimentary circuit analysis, the R-MOSFET-C filter shown in Fig. 2.20 displays a loop gain of $\overline{A}f$ at low frequencies, if the transfer function of the MOSFET-C integrator inside the loop is $\overline{A}$ (with the same dc gain of the op amp) and f is defined by

$$f \approx \frac{(R||R_X)}{(R||R_X)+R} = \frac{1}{F}, \quad \text{where} \quad R_X = \frac{1}{G_{3,4}+G_{1,2}} = \frac{1}{2\overline{G}}. \tag{2.38}$$

This result assumes $R = R_1 = R_2$. As a result, MOSFET nonlinearities are reduced by this loop gain within the filter bandwidth. Detailed analysis will further show that the loop gain decreases as the input frequency passes the dominant pole of the integrator $\overline{A}$. Thus the distortion reduction by the feedback approaches its minimum at the filter pass-band edge.

2.3.1 Systematic view of linearity improvement

The concept of the linearity improvement by the feedback loop gain in an R-MOSFET-C filter implementation can be illustrated by the description of a few systematic blocks as shown in Figs. 2.21 and 2.22. The standard active filter implementation shown in Fig. 2.21 yields the transfer function

$$\frac{V_o}{V_i} = \frac{-A_o G_1}{1+A_o G_2}. \tag{2.39}$$

If the transconductance elements G_1 and G_2 were linear components such as passive resistors, the overall transfer function would see only a small amount of nonlinearity due to the forward path in the loop, A_o. The nonlinearity of this stage in the loop is diminished drastically because of the large loop gain this component experiences. (The mathematical

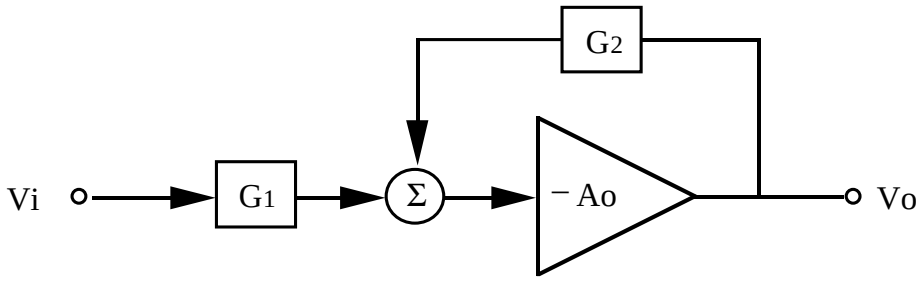


Figure 2.21 Standard Active Filter Approach

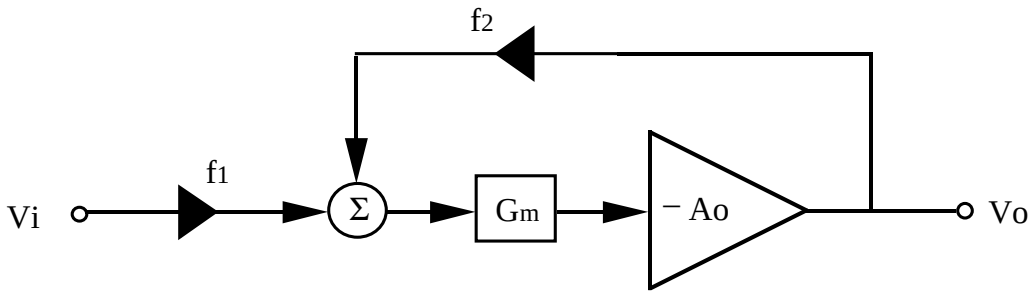


Figure 2.22 R-MOSFET-C Filter Approach

details of this effect will be discussed later in this section.) This phenomenon is quite common in the usage of most op amps under a large amount of linear feedback. However, when a variable control is added to the transconductance elements G_1 and G_2 for filter tuning, a large amount of nonlinearity coming from these tunable components is unavoidable. These components do not reside on the forward path inside a feedback loop, so there is no help in reducing the distortion by a feedback loop gain.

An implementation to maintain the tunability yet reap the benefits of linearity improvement by the feedback loop-gain is shown in Fig. 2.22. The systematic block diagram equivalent to an R-MOSFET-C filter implementation shown in Fig. 2.22 yields the transfer func-

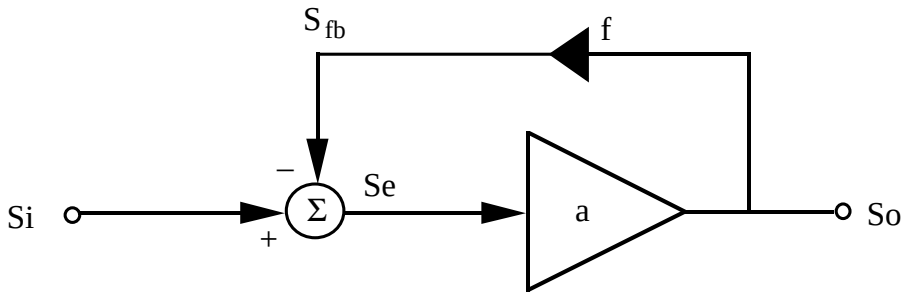


Figure 2.23 Nonlinear Function in a Linear Feedback

tion

$$\frac{V_o}{V_i} = \frac{-A_o G_m f_1}{1 + A_o G_m f_2}. \tag{2.40}$$

Because all nonlinear blocks reside on the forward path inside a feedback loop, the nonlinearities are suppressed by the amount of feedback loop gain. Another way to note this linearity improvement by loop gain is simply to observe the transfer function. As shown in (2.40), the nonlinear functions are lumped together in a such a way that the transfer function has the format of $k\ X/(1+X)$. The k is simply a constant and the term $X/(1+X)$ shows that the nonlinear term X resides on the forward path inside the feedback loop.

Let us now consider a general case of a nonlinear system block and the linearity improvement under a linear feedback by applying the power series nonlinear analysis. The added complexity of the Volterra series including the high-frequency effects is really unnecessary in the general understanding of the linear feedback loop for the reduction of distortion. Shown in Fig. 2.23 is the general block diagram of a closed-loop system where a linear feedback is applied to a nonlinear open-loop block.

First, without the linear feedback ($f = 0$), $S_e = S_i$, the open-loop characteristic from

the input S_i to the output S_o can be assumed to have a general nonlinear power series relationship

$$S_o = a_1 S_i + a_2 S_i^2 + a_3 S_i^3 + \ \ldots \ \ . \tag{2.41}$$

When a sinusoidal signal $S_i = S_{iM} cos(wt)$ is applied at the input, the output becomes

$$\begin{aligned} S_o &= a_1 S_{iM} cos(wt) + a_2 S_{iM}^2 cos^2(wt) + a_3 S_{iM}^3 cos^3(wt) + \ \ldots \\ &= a_1 S_{iM} cos(wt) + a_2 S_{iM}^2 \frac{1}{2}(cos(2wt) + 1) \\ &\quad + a_3 S_{iM}^3 \frac{1}{4}(cos(3wt) + 3cos(wt)) + \ \ldots \ \ . \end{aligned} \tag{2.42}$$

The first term is completely linear, but the rest of the terms add directly to the harmonics of the input frequency. If the terms above S_i^3 are neglected, one can define a measure for the second harmonic distortion

$$HD_2 \equiv \frac{\text{second harmonic}}{\text{fundamental}} \approx \frac{a_2 S_{iM}^2 \frac{1}{2}}{a_1 S_{iM}} = \frac{1}{2}\frac{a_2}{a_1} S_{iM}. \tag{2.43}$$

Similarly, the third harmonic measure is

$$HD_3 \equiv \frac{\text{third harmonic}}{\text{fundamental}} \approx \frac{a_3 S_{iM}^3 \frac{1}{4}}{a_1 S_{iM}} = \frac{1}{4}\frac{a_3}{a_1} S_{iM}^2. \tag{2.44}$$

When these results are referred to the output with a magnitude approximation $S_{oM} \approx a_1 S_{iM}$, they become

$$HD_2 \approx \frac{1}{2}\frac{a_2}{a_1^2} S_{oM} \ \text{ and } \ HD_3 \approx \frac{1}{4}\frac{a_3}{a_1^3} S_{oM}^2. \tag{2.45}$$

Further detailed analysis including the intermodulation (IM) of double or triple frequencies and the cross modulation (CM) of AM (amplitude modulation) carrier frequencies can

be performed in a similar manner with an appropriate combination of signals S_i other than just a single sinusoidal input [49]. Because the effects of the linear feedback loop on any kind of distortion are very similar, the mathematics herein will only cover the derivation of HD_2 and HD_3.

When the nonlinear open-loop function operates in a linear feedback loop as shown in Fig. 2.23, the previous Equation (2.41) becomes

$$S_o = a_1 S_e + a_2 S_e^2 + a_3 S_e^3 + \ \ldots, \quad \text{where} \tag{2.46}$$

$$S_e = S_i - S_{fb} = S_i - f S_o.$$

With the expanded form of the open-loop portion

$$S_o = a_1(S_i - f S_o) + a_2(S_i - f S_o)^2 + a_3(S_i - f S_o)^3 + \ \ldots, \tag{2.47}$$

and the generalized form of the closed-loop configuration

$$S_o = b_1 S_i + b_2 S_i^2 + b_3 S_i^3 + \ \ldots, \tag{2.48}$$

these two terms for S_o can be equated to solve for the closed-loop coefficients b_1, b_2, and b_3 in terms of the open-loop coefficients a_1, a_2, and a_3. Doing so, we have

$$\begin{aligned} S_o &= b_1 S_i + b_2 S_i^2 + b_3 S_i^3 + \ \ldots \\ &= a_1(S_i - f b_1 S_i - f b_2 S_i^2 - f b_3 S_i^3 - \ \ldots) \\ &\quad + a_2(S_i - f b_1 S_i - f b_2 S_i^2 - f b_3 S_i^3 - \ \ldots)^2 \\ &\quad + a_3(S_i - f b_1 S_i - f b_2 S_i^2 - f b_3 S_i^3 - \ \ldots)^3 + \ \ldots \quad . \end{aligned} \tag{2.49}$$

From the equation above we may extract a few equalities of interest

$$\begin{aligned} b_1 S_i &= a_1(S_i - f b_1 S_i), \\ b_2 S_i^2 &= -a_1 f b_2 S_i^2 + a_2(S_i - f b_1 S_i)^2, \text{ and} \\ b_3 S_i^3 &= -a_1 f b_3 S_i^3 + a_3(S_i - f b_1 S_i)^3 - 2a_2(1 - f b_1)(f b_2) S_i^3. \end{aligned} \tag{2.50}$$

Solving the equations above, the closed-loop coefficients are found as

$$\begin{aligned} b_1 &= \frac{a_1}{1 + a_1 f}, \quad b_2 = \frac{a_2}{(1 + a_1 f)^3}, \text{ and} \\ b_3 &= \frac{a_3(1 + a_1 f) - 2a_2^2 f}{(1 + a_1 f)^5} \approx \frac{a_3}{(1 + a_1 f)^4}. \end{aligned} \tag{2.51}$$

Using the expressions for HD_2 and HD_3 given in Equation (2.45), and applying them to this closed-loop function,

$$HD_2 \approx \frac{1}{2}\frac{b_2}{b_1^2} S_{oM} = \left[\frac{1}{2}\frac{a_2}{a_1^2} S_{oM}\right] \frac{1}{1 + a_1 f} \text{ and}$$

$$\begin{aligned} HD_3 \approx \frac{1}{4}\frac{b_3}{b_1^3} S_{oM}^2 &= \left[\frac{1}{4}\frac{a_3}{a_1^3} S_{oM}^2\right] \frac{1}{1 + a_1 f} \left[1 - \frac{2a_2^2 f}{a_3(1 + a_1 f)}\right] \\ &\approx \left[\frac{1}{4}\frac{a_3}{a_1^3} S_{oM}^2\right] \frac{1}{1 + a_1 f}. \end{aligned} \tag{2.52}$$

The conclusion to draw from the derivation above is that the harmonics generated by the nonlinear functions in the open-loop configuration are greatly reduced by the amount of linear feedback applied to the closed loop. Referring back to Fig. 2.22, it is exactly this phenomenon, shown by mathematical derivation, that improves the linearity in the R-MOSFET-C filter approach. This observation can be directly transferred to the actual circuit implementation of the R-MOSFET-C filter implementation shown in Fig. 2.20.

2.3.2 Transfer function of standard MOSFET-C

To observe the changes in the feedback loop configuration for this low distortion R-MOSFET-C filter, as an exemplary comparison, we can observe first the transfer function of the first-order standard MOSFET-C filter as shown in Fig. 2.19. Observing the single-ended case for simplification of analysis, some algebra yields the closed-loop transfer function

$$-\frac{V_o}{V_i} = \frac{Z_f}{R_i}\frac{A(\frac{R_i}{R_i+Z_f})}{1+A(\frac{R_i}{R_i+Z_f})} \text{ where } Z_f = R_f||C. \tag{2.53}$$

This can also be expressed as

$$-\frac{V_o}{V_i} = \frac{R_f}{R_i}\frac{A\{\frac{R_i||C(1+A)}{R_i||C(1+A)+R_f}\}}{1+A\{\frac{R_i||C(1+A)}{R_i||C(1+A)+R_f}\}} = \frac{R_f}{R_i}\frac{A\{\frac{R_i}{R_i+R_f+sCR_iR_f(1+A)}\}}{1+A\{\frac{R_i}{R_i+R_f+sCR_iR_f(1+A)}\}}. \tag{2.54}$$

It can be observed from the transfer function that the right half of the expression, in the format of $X/(1+X)$, is highly linear inside the bandwidth of the filter because of the linearity improvement by the feedback loop gain. Thus the distortion in this MOSFET-C filter is dominated by the nonlinear R_f/R_i ratio. This ratio R_f/R_i can never be sufficiently linear because R_f and R_i are directionally nonlinear, meaning that nonlinearity of the MOSFET is a function of V_{DS}, not $|V_{DS}|$, including both even and odd harmonics. And even though a fully differential architecture can cancel much of the even harmonics, the mismatch of transistors limits the linearity performance. Limited linearity achieved by this kind of configuration can vary over the range of input frequencies and has been discussed for a biquad example in [50].

2.3.3 Transfer function of linearity-improved R-MOSFET-C

Now we may observe the feedback loop configuration used in the R-MOSFET-C linearity improvement technique as shown in Fig. 2.20. The loop-gain is $\overline{A}f$ if the transfer function of the MOSFET-C integrator inside the loop is $\overline{A} \approx G_{1,2}/sC$ (with the same dc gain of the op amp), and the transfer function (for single-ended) is

$$-\frac{V_o}{V_i} = \frac{R_2}{R_1}\frac{\overline{A}(\frac{R_1||Z_X}{R_1||Z_X+R_2})}{1+\overline{A}(\frac{R_1||Z_X}{R_1||Z_X+R_2})}, \text{ where } Z_X = \frac{1}{G_{3,4}}|| \left\{\frac{1}{G_{1,2}} + \frac{1}{sC(1+A)}\right\}. \quad (2.55)$$

Note that

$$f = \frac{R_1||Z_X}{R_1||Z_X+R_2} \approx \frac{R_1||R_X}{R_1||R_X+R_2}, \text{ where } R_X = \frac{1}{G_{3,4}+G_{1,2}} = \frac{1}{2\overline{G}}, \quad (2.56)$$

and for the condition where $R_1 = R_2$, $f \approx 1/F$. It is clear from the transfer function that the ratio R_2/R_1 is linear, fully depending upon the linearity of passive resistors, and the right half of the expression is in the format $T/(1+T)$. This means that all nonlinear functions are inside the feedback loop where the loop-gain, $T = \overline{A}(R_1||Z_X)/(R_1||Z_X+R_2)$, reduces distortion within the bandwidth of the filter. The reduction of distortion approaches a minimum as the input frequency approaches the corner frequency of the filter where the magnitude of the loop-gain T becomes unity.

A graphical illustration of the implementation above is shown in Fig. 2.24. As the MOSFET-C integrator inside the feedback loop has a unity gain frequency that is greater than the R-MOSFET-C path by the fixed factor F according to the voltage scaling, the loop-gain $\overline{A}f \approx \overline{A}/F$ simply sees a scaled portion of the gain that the MOSFET-C integrator $\overline{A}$ experiences. The plot of the loop gain is simply a shifted version of that of the MOSFET-C

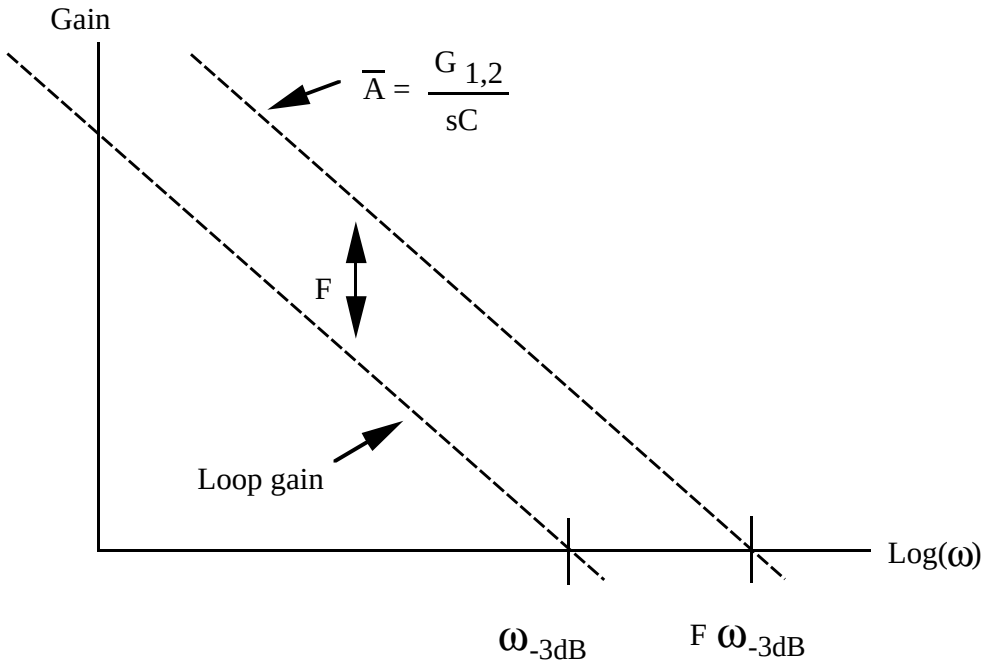


Figure 2.24 Loop Gain in R-MOSFET-C Filter

integrator, with a unity gain crossing at the -3 dB bandwidth of the R-MOSFET-C filter.

This effect of feedback on filter linearity is more conveniently understood in the simulation result of a fifth-order Bessel filter as shown in Fig. 2.25, where the R-MOSFET-C filter achieves about 50 dB improvement over the conventional MOSFET-C filter at 2 kHz input. (The prototype R-MOSFET-C filter has a set of varied voltage scale factors, F=2.5-5, the details of which are discussed in Chapter 5.) The simulation was performed with a fixed level of all component mismatches including the MOSFET resistor mismatches. For visual identification of this improvement, Figs. 2.26 and 2.27 show the simulation results displaying a significant change in the harmonics due to the 2 kHz 4-V_{p-p} differential sinusoidal input, for the standard MOSFET-C implementation and the linearity-improved R-MOSFET-C implementation, respectively.

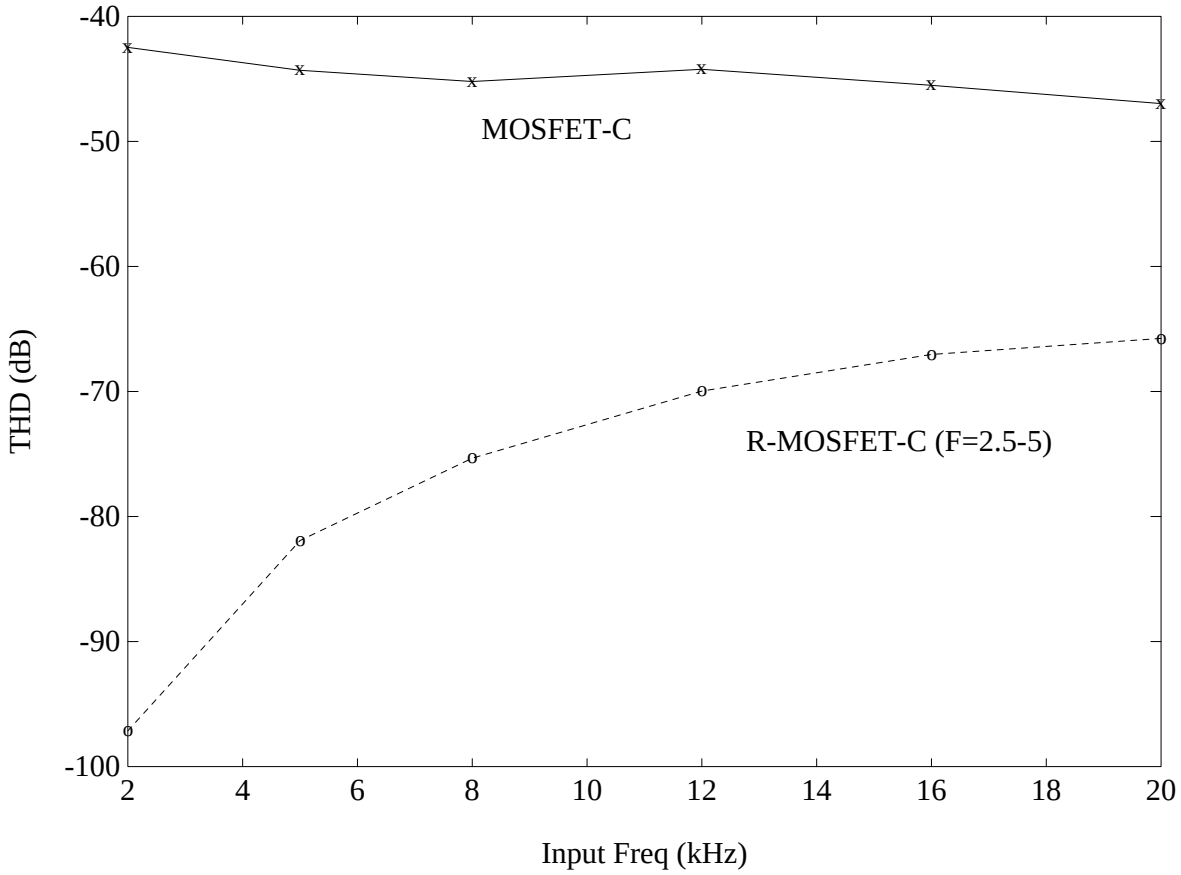


Figure 2.25 THD Improvement vs. Frequency

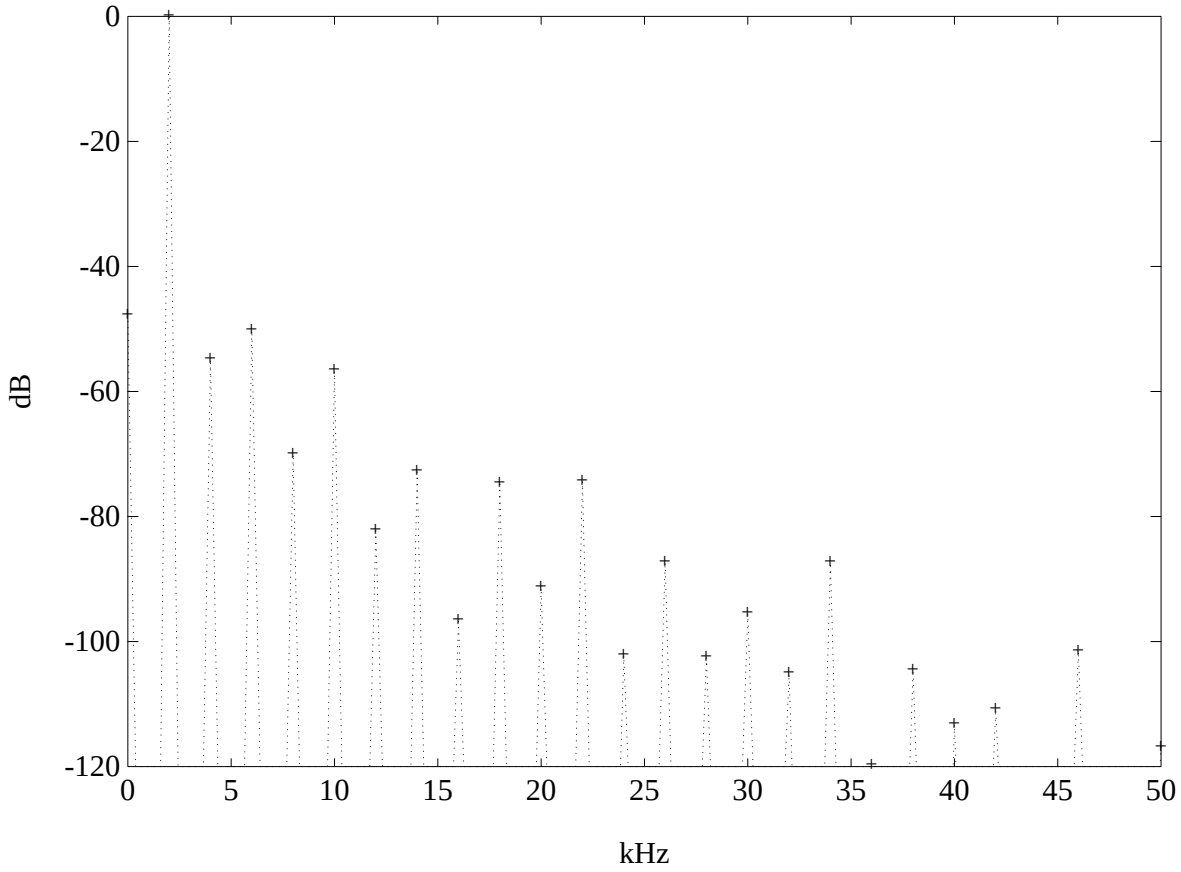


Figure 2.26 Harmonic Distortion (MOSFET-C)

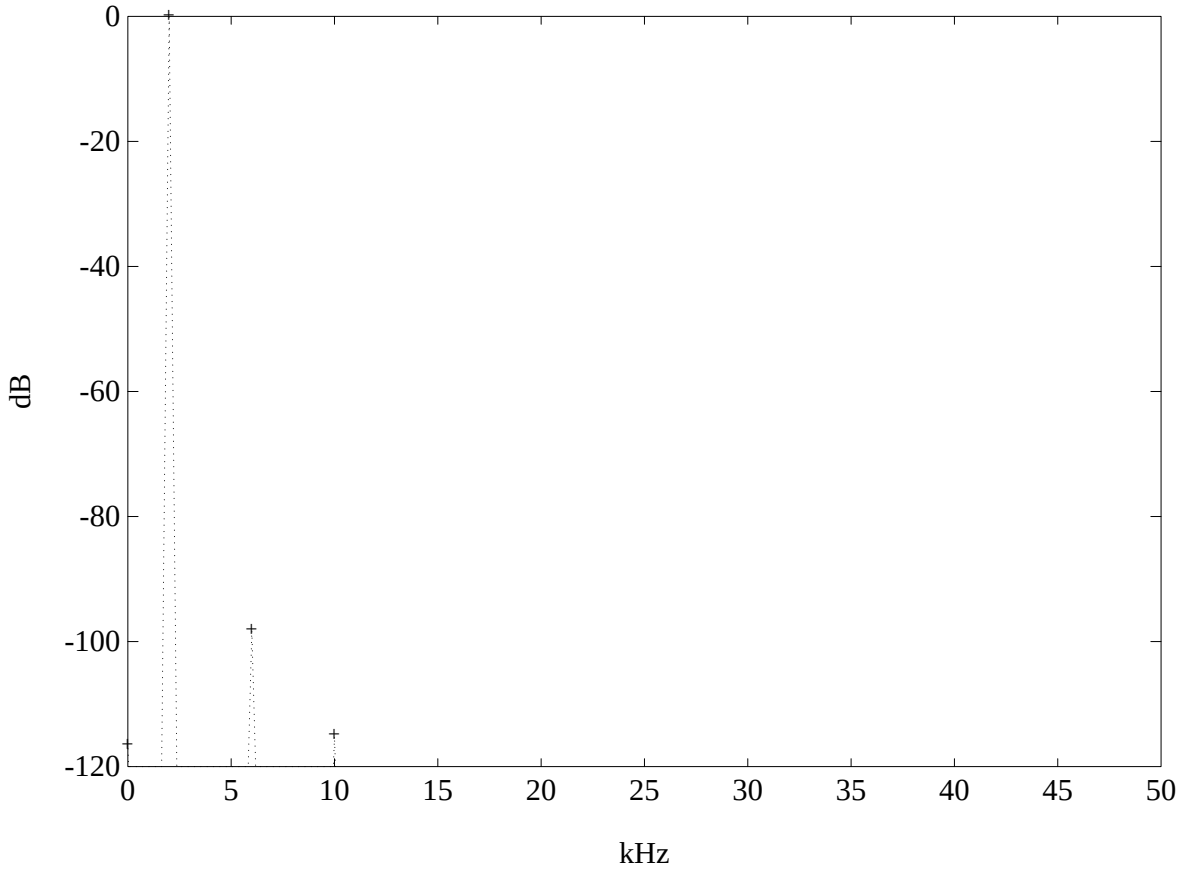


Figure 2.27 Harmonic Distortion (F=2.5-5)

Analyzing in detail the plot in Fig. 2.25, the implementation using the conventional MOSFET-C integrators of Fig. 2.19 exhibits a constant THD independent of the frequencies in the passband. But the improved implementation using the linearity-improved R-MOSFET-C integrators of Fig. 2.20 exhibits a much lower THD, particularly at lower frequencies due to the increased effect of the feedback loop gain on distortion. Near the passband edge where the loop gain is minimized, this linearity improvement disappears, but the R-MOSFET voltage scaling still maintains THD lower than the conventional filter by a factor of F.

CHAPTER 3

SELF-TUNING CIRCUIT IMPLEMENTATION

3.1 Automatic Tuning Fundamentals

In order to control accurately the RC time-constant of a filter, an electronically tunable component is automatically tuned to a fixed reference of a known accuracy. In the case of R-MOSFET-C design, a control voltage can vary the effective resistance of the R-MOSFET portion to a desired value so that the time constant of the filter which defines the -3 dB frequency of the filter will result in an accurate value. For the prototype filter implemented, an accurate 22-kHz audio-band low-pass filter is desired.

Automatic tuning methods may be separated into two categories, *direct* and *indirect*. Indirect tuning is quite advantageous over the direct tuning method because of its inherent setup for background adjustment. Many well-known implementations have used the indirect tuning methods [22], [25]-[27], [33]. Figure 3.1 shows a simple block diagram describing the indirect automatic tuning implementation. As seen in the figure, the tuning is performed in the background, allowing the filter (the *slave*) to operate at all times. Only the *master* portion is used to compare to the accurate reference. The drawback resides in the master-slave matching relationship itself, which relies heavily on good component matching between the two circuit blocks. Any mismatch between the master and the slave will directly affect the accuracy of the desired corner frequency for the filter (the slave).

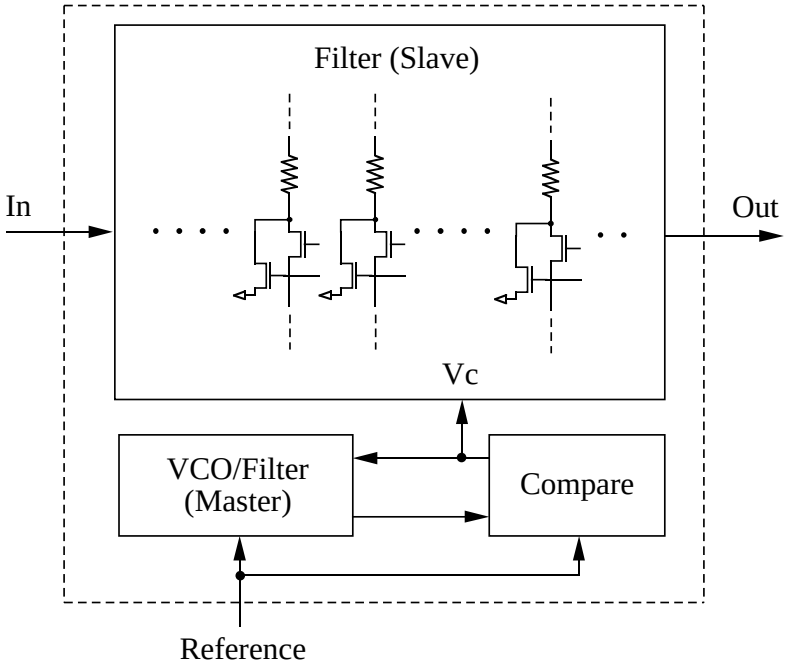


Figure 3.1 Indirect Automatic Tuning

The inaccuracy resulting from the mismatch can be minimized by applying the direct tuning method as shown in Fig. 3.2. Unlike indirect tuning, the direct tuning method uses the main circuit block itself to tune to an accurate reference. Because the filter itself (slave in the indirect method) is tuned to the accurate reference, the inherent mismatch problem in the master-slave configuration is eliminated. The main drawback in the direct tuning method, on the other hand, is the foreground nature of the tuning process. Because of this, given component variation (time-constant variation) due to temperature and aging, the necessity of re-tuning the filter requires an interruption of the filter operation. Unless a redundant circuit block is used to mask the circuit to appear as if the operation is uninterrupted (which would require an increased circuit implementation with higher cost), this direct tuning cannot provide background adjustment.

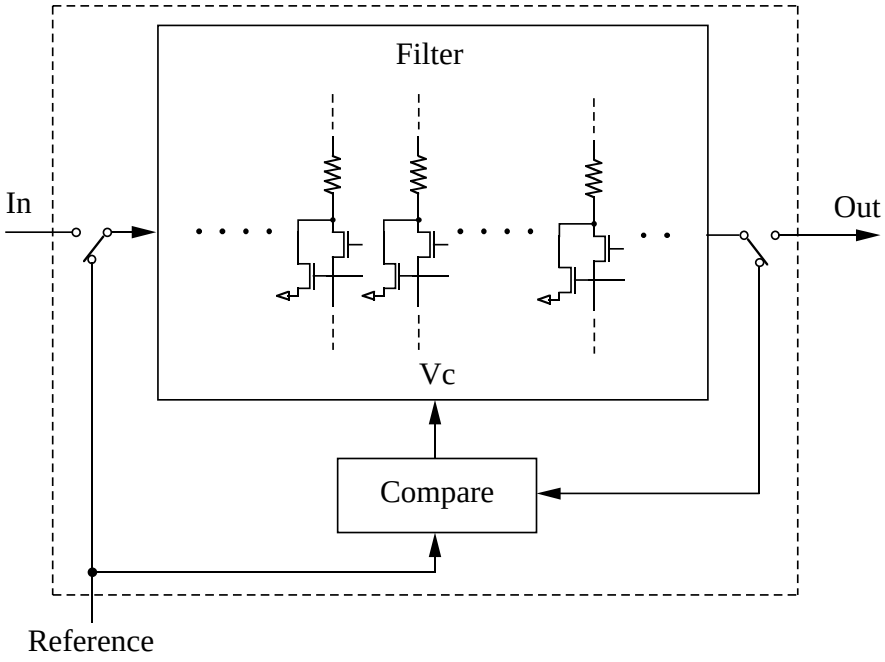


Figure 3.2 Direct Automatic Tuning

Many conventional approaches reveal the use of a phase-locked control loop in a master-slave configuration [22], [25], [26], [33]. The master is often a voltage-controlled oscillator (VCO) or a small low-order filter that is tuned by phase locking to an external reference frequency. This master is then used to indirectly tune the slave, which is the filter. This method has successfully demonstrated reliable performance, but with an unnecessary complexity.

3.2 Switched-Capacitor and Continuous-Time Paths Matching

A new automatic tuning approach to be described herein takes advantage of the switched-capacitor network accuracy to implement a reference time constant [51]. The time constant in a switched-capacitor network depends solely on capacitor matching. This switched-

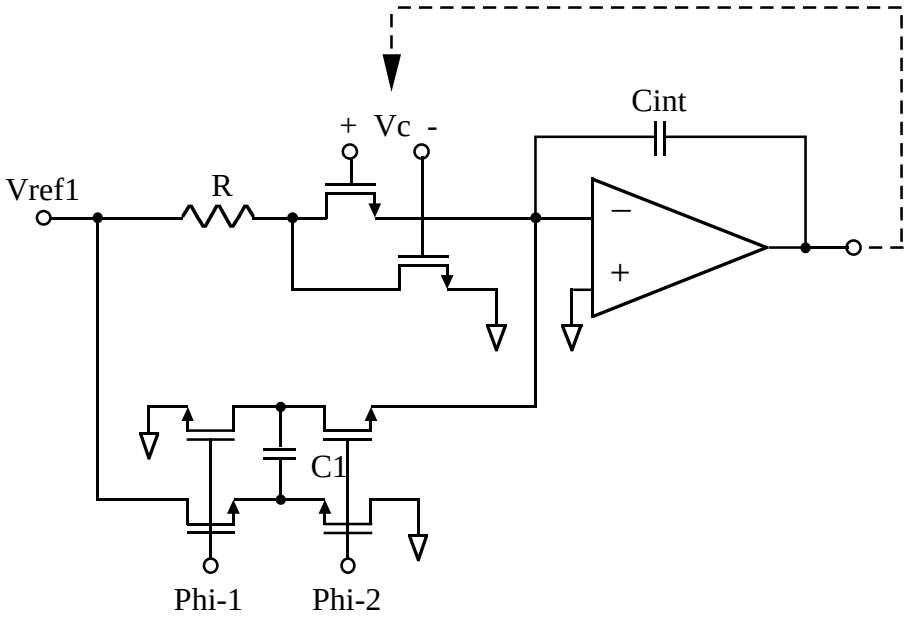


Figure 3.3 Time Constant Matching Integrator

capacitor tuning method is no different from the conventional indirect tuning method in that it tunes the filter in the master-slave configuration where an equally satisfactory component matching is required for an equivalent accuracy of filter tuning. However, replacing the core of the complex tuning circuitry with a mere RC time-constant-matching circuit greatly simplifies the task. No VCO or low-order filter is required in the master portion.

Shown in Fig. 3.3 is the time-constant-matching integrator of the linearity-improved continuous-time path (R-MOSFET) and the switched-capacitor path. The time constant of the continuous-time path is $R_{eq}C_{int}$ and that of the switched-capacitor path is $C_{int}/(f_{clk}C_1)$. The mismatch of the two time constants, which simplify as the mismatch of R_{eq} and $1/(f_{clk}C_1)$, is reflected at the output of the integrator. That voltage is then translated to the control voltage of the current-steering MOSFETs. Equilibrium is reached when $R_{eq} =$

$1/(f_{clk}C_1)$. Even though illustrated with the tunable R-MOSFET resistor (continuous-time path), note that this time-constant-matching circuit is generally applicable to comparisons of all continuous-time and switched-capacitor paths.

3.2.1 Differential and common-mode control voltages

The overall schematic of the tuning circuitry used in the self-tuning R-MOSFET-C filter is shown in Fig. 3.4. The lower portion of the schematic is the tuning circuitry for the common-mode control voltage. This common-mode control voltage V_{CM} maintains the designed voltage scale factor F. The reference for the ratio F is simply established by the voltage divider, and the settled common-mode voltage V_{CM} merges with the differential control voltage V_C at the input of the op amp on the upper right portion of the schematic. The actual time-constant matching, given the common-mode portion of the control voltage resulting from an independent loop, is accomplished by varying the differential control voltage, $V_C = V_{C+} - V_{C-}$. Placing a dominant pole in the control loop by choosing a very large product $R_{LP}C_{LP}$ (alternately a large C_{int} can be used) establishes a stable control. Figure 3.5 shows the transient settling of these control voltages with a low-pass time-constant of approximately 2 msec. Among the fabricated prototype filters, the pass-band f_{-3dB} standard deviation (in percent of the nominal f_{-3dB}) is 5%, measured under a fixed capacitance, C_1, and the same reference frequency, f_{clk}. If a greater accuracy of the corner frequency is desired, a fine adjustment can be provided by means of either digitally trimming the capacitor, C_1, or varying the clock frequency, f_{clk}. Having replaced the capacitor C_1 by a set of binary-weighted capacitors for digital tuning as shown in Fig. 3.6,

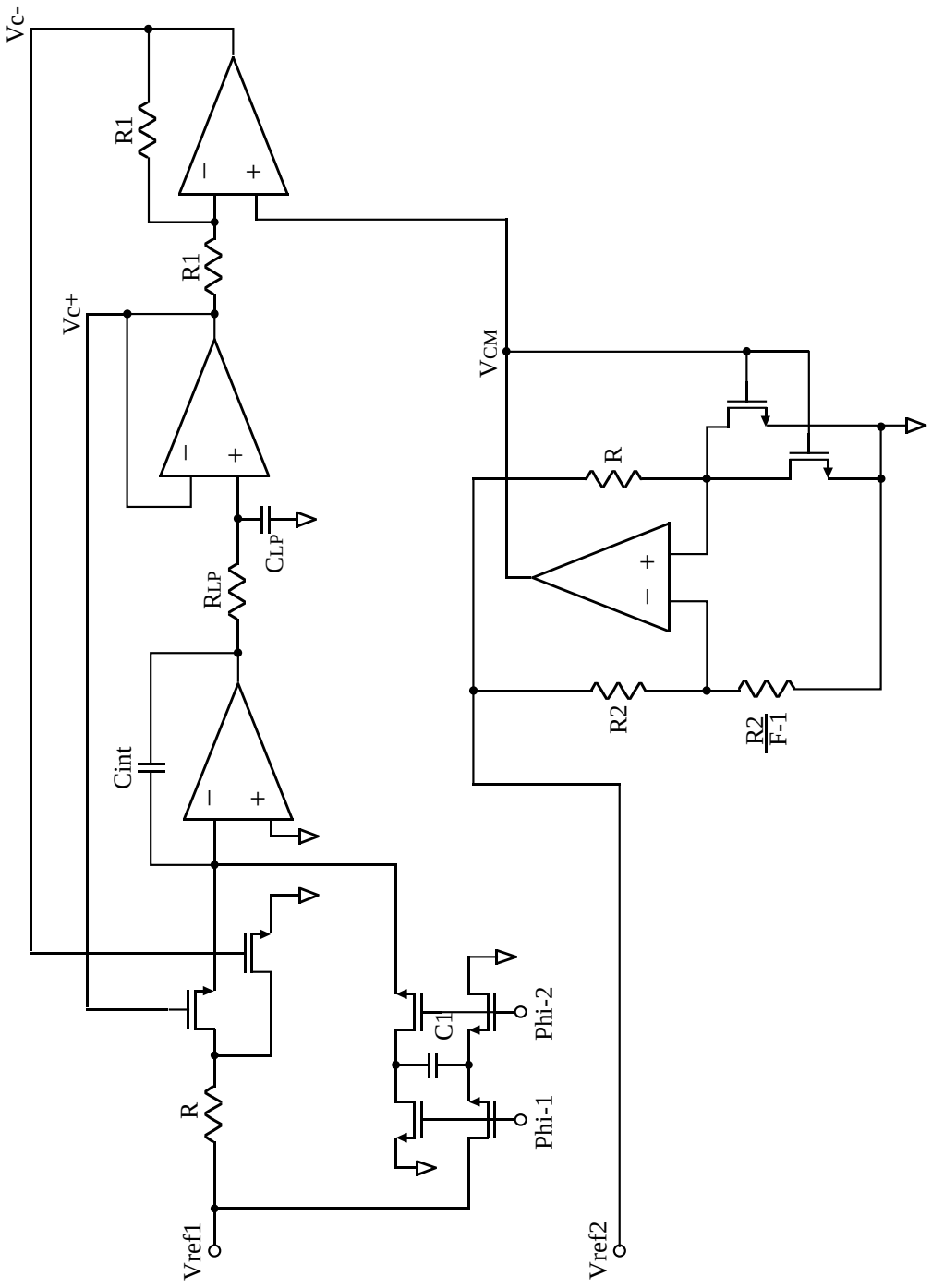


Figure 3.4 Frequency Tuning Circuitry

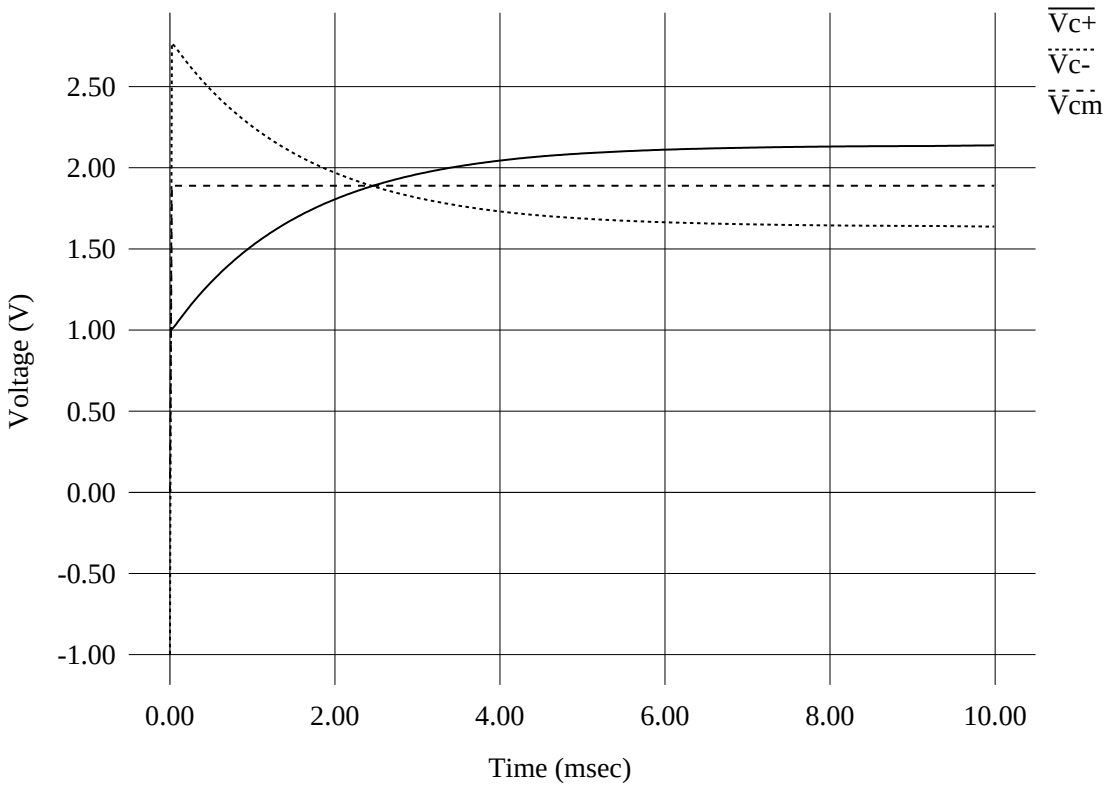


Figure 3.5 Control Voltage Settling

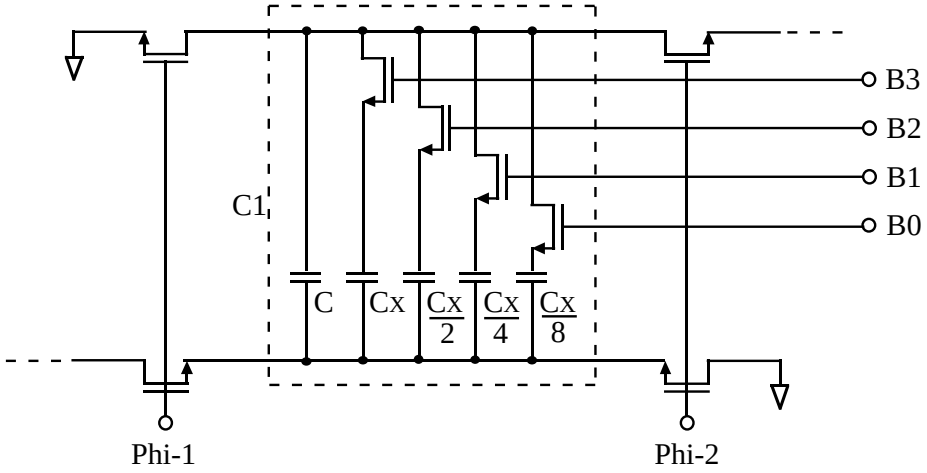


Figure 3.6 Digital Control for Tuning

the fine tuning for the desired corner frequency of the prototype filter can be accomplished within a ±1% absolute accuracy.

CHAPTER 4

DYNAMIC RANGE OPTIMIZATION

In addition to the many techniques used for improving the dynamic range of an active filter, as concisely summarized in [52], the dynamic range can be further improved after node-voltage scaling by an optimization method which uses the chip area as the constraint condition. Simply increasing all capacitances and reducing all resistances by the same proportion in an active filter will maintain the identical frequency response and improve the dynamic range by an equal proportion, but there is no true net gain in this kind of dynamic range improvement because the chip area taken up by the capacitors is typically dominant, especially in low-frequency filters. Thus a better focus is to maximize the dynamic range per total chip area (approximately the total capacitance). This approximation results from neglecting the silicon area taken up by the resistors in comparison to the area occupied by the capacitors. This optimization problem naturally leads to a linear programming problem.

4.1 Linear Programming Conditions

In all active RC filters, in order for a filter to maintain a given frequency response as designed, each time constant for all of the integrating signal paths has to be fixed. Shown in Fig. 4.1 is the schematic of a fifth-order Bessel filter obtained from an LC ladder to active RC filter transformation and node-voltage scaling [53]-[57]. A total of eleven time constants exist in this fifth-order Bessel filter example. The time-constants are $\tau_1 = R_1C_k$, $\tau_2 = R_2C_k$, $\tau_3 = R_3C_k$, up to $\tau_{11} = R_{11}C_k$, where C_k is one of the five capacitors

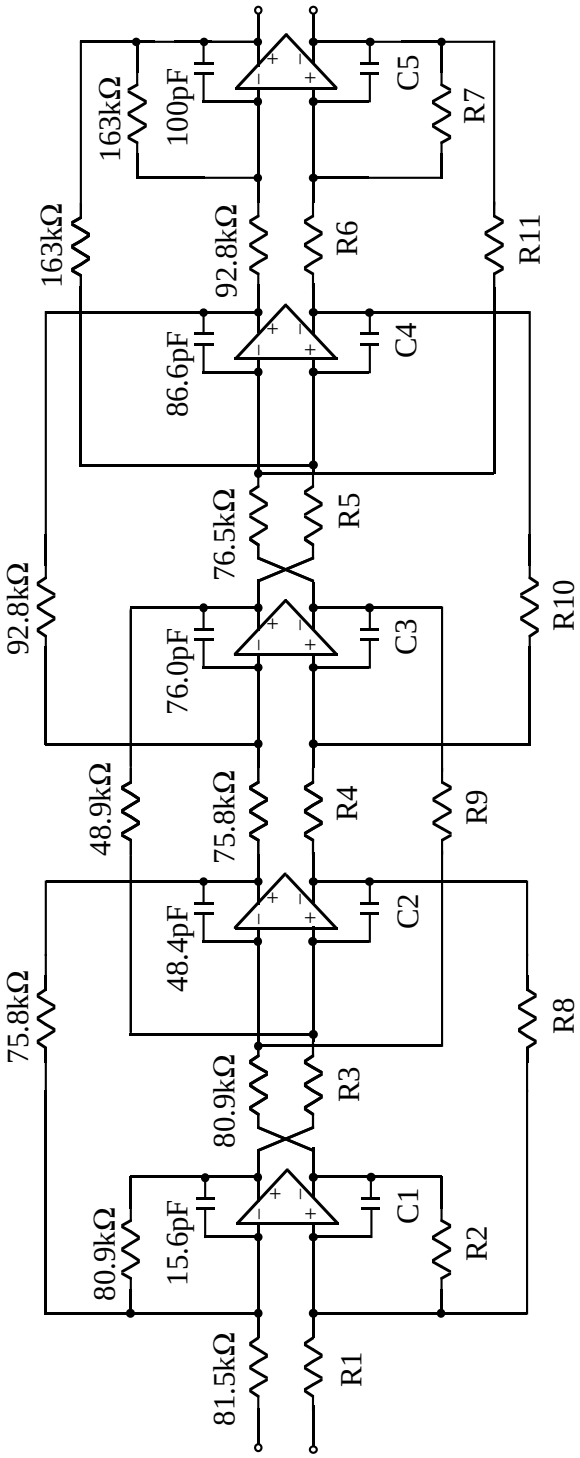


Figure 4.1 RC 5th-order Bessel (Node Scaled)

connected to the given resistor at a summing node. For example, C_1 is connected to R_1, R_2, and R_8 at the summer node of the first operational amplifier.

As each equivalent noise voltage source in series with a resistor has a different gain to the output of the filter, the total noise power of the filter at the output is proportional to a cost function defined by

$$Cost = \sum_{i=1}^{11} R_i {A_i}^2, \tag{4.1}$$

where

$$A_i = \text{Gain from } R_i \text{ to the output.}$$

The constraint condition on the other hand is

$$C_{total} = C_1 + C_2 + C_3 + C_4 + C_5, \tag{4.2}$$

where C_{total} is a constant (i.e., fixed area). Each C_k can also be replaced by terms in R_i and fixed time constant τ_i. Also note the fact that A_i corresponding to each resistor is a constant value at any fixed frequency, because the time constant for each RC path does not change from the optimization (linear programming), maintaining the identical frequency response. Even though the A_i for each resistor should represent a value proportional to the integral sum for the entire band to be precise, for simplicity, a dc gain value for each of the resistors is used. Simulation results verify that this approximation is sufficient.

4.2 Simplification of Linear Programming Conditions

In order to set up the linear programming problem with the simplest possible set of function variables, only five variables may be used (corresponding to five capacitors/op

amps) in this fifth-order Bessel filter example. According to the schematic in Fig. 4.1, arbitrarily choose R_1, R_3, R_4, R_5, and R_6, each corresponding to C_1 to C_5, respectively, as the variables for the cost and constraint functions. The rest of the parameters (resistances) can be written in terms of these chosen five variables because the ratios between the pairs of resistors merging at the common summing node are also fixed just as the time constant for each RC combination is fixed. The ratios are

$$k_2 = \frac{R_2}{R_1}, \quad k_8 = \frac{R_8}{R_1}, \quad k_9 = \frac{R_9}{R_3},$$

$$k_{10} = \frac{R_{10}}{R_4}, \quad k_{11} = \frac{R_{11}}{R_5}, \quad \text{and} \quad k_7 = \frac{R_7}{R_6}. \tag{4.3}$$

Using the ratios above, the rest of the parameters (resistances) are defined in terms of the five variables as

$$R_2 = k_2 R_1, \quad R_8 = k_8 R_1, \quad R_9 = k_9 R_3,$$

$$R_{10} = k_{10} R_4, \quad R_{11} = k_{11} R_5, \quad \text{and} \quad R_7 = k_7 R_6. \tag{4.4}$$

Another set of fixed terms, as previously mentioned, is the set of time constants, which are

$$\tau_{c1} = \tau_1 = R_1 C_1, \quad \tau_{c2} = \tau_3 = R_3 C_2, \quad \tau_{c3} = \tau_4 = R_4 C_3,$$

$$\tau_{c4} = \tau_5 = R_5 C_4, \quad \text{and} \quad \tau_{c5} = \tau_6 = R_6 C_5. \tag{4.5}$$

Combining these definitions together with the original expression for *Cost* and C_{total} leaves a simplified expression

$$\begin{aligned} \textit{Cost} = {} & R_1(A_1^2 + k_2 A_2^2 + k_8 A_8^2) + R_3(A_3^2 + k_9 A_9^2) + R_4(A_4^2 + k_{10} A_{10}^2) \\ & + R_5(A_5^2 + k_{11} A_{11}^2) + R_6(A_6^2 + k_7 A_7^2) \quad \text{and} \end{aligned} \tag{4.6}$$

$$C_{total} = \frac{\tau_{c1}}{R_1} + \frac{\tau_{c2}}{R_3} + \frac{\tau_{c3}}{R_4} + \frac{\tau_{c4}}{R_5} + \frac{\tau_{c5}}{R_6}. \tag{4.7}$$

The cost and the constraint functions are now expressed in terms of the five chosen variables, R_1, R_3, R_4, R_5, and R_6.

4.3 Linear Programming Approach and Result

Before a standard linear programming approach such as Karmarkar's method [58] is applied to given cost and constraint functions, some sort of linearization is necessary if there are any functions that are not linear. As observed in Equation (4.7), the constraint function, in the case of fixed total capacitance, is a nonlinear function. This constraint function can be linearized by a first-order Taylor's approximation before a standard linear programming technique is applied. With the Taylor's approximation expanded about $\vec{x} = \vec{x}_{(0)}$, the constraint function results in the form

$$\begin{aligned} f(\vec{x}) &= f(x_1) + f(x_2) + f(x_3) + f(x_4) + f(x_5) \\ &\approx f(x_{1(0)}) + f'(x_{1(0)})(x_1 - x_{1(0)}) + f(x_{2(0)}) + f'(x_{2(0)})(x_2 - x_{2(0)}) \\ &\quad + f(x_{3(0)}) + f'(x_{3(0)})(x_3 - x_{3(0)}) + f(x_{4(0)}) + f'(x_{4(0)})(x_4 - x_{4(0)}) \\ &\quad + f(x_{5(0)}) + f'(x_{5(0)})(x_5 - x_{5(0)}), \end{aligned} \tag{4.8}$$

where

$$f(x_1) = \frac{\tau_{c1}}{x_1} = \frac{\tau_{c1}}{R_1}, \quad f(x_2) = \frac{\tau_{c2}}{x_2} = \frac{\tau_{c2}}{R_3}, \quad f(x_3) = \frac{\tau_{c3}}{x_3} = \frac{\tau_{c3}}{R_4},$$

$$f(x_4) = \frac{\tau_{c4}}{x_4} = \frac{\tau_{c4}}{R_5}, \quad f(x_5) = \frac{\tau_{c5}}{x_5} = \frac{\tau_{c5}}{R_6},$$

$$f'(x_1) = -\frac{\tau_{c1}}{x_1^2}, \quad f'(x_2) = -\frac{\tau_{c2}}{x_2^2}, \quad f'(x_3) = -\frac{\tau_{c3}}{x_3^2},$$

$$f'(x_4) = -\frac{\tau_{c4}}{x_4^2}, \text{ and } f'(x_5) = -\frac{\tau_{c5}}{x_5^2}. \tag{4.9}$$

Expanding Equation (4.8) by replacing terms with expressions from (4.9) reveals

$$\begin{aligned} C_{total} &= f(\vec{x}) \\ &= 2f(\vec{x}_{(0)}) - \left(\frac{\tau_{c1}x_1}{x_{1(0)}^2} + \frac{\tau_{c2}x_2}{x_{2(0)}^2} + \frac{\tau_{c3}x_3}{x_{3(0)}^2} + \frac{\tau_{c4}x_4}{x_{4(0)}^2} + \frac{\tau_{c5}x_5}{x_{5(0)}^2} \right). \end{aligned} \tag{4.10}$$

Because $2f(\vec{x}_{(0)}) = 2C_{total}$ from the initial condition, (4.10) reduces to

$$C_{total} = \left(\frac{\tau_{c1}}{x_{1(0)}^2} \right) x_1 + \left(\frac{\tau_{c2}}{x_{2(0)}^2} \right) x_2 + \left(\frac{\tau_{c3}}{x_{3(0)}^2} \right) x_3 + \left(\frac{\tau_{c4}}{x_{4(0)}^2} \right) x_4 + \left(\frac{\tau_{c5}}{x_{5(0)}^2} \right) x_5. \tag{4.11}$$

From (4.9) note that $x_1 = R_1$, $x_2 = R_3$, $x_3 = R_4$, $x_4 = R_5$, and $x_5 = R_6$. The $x_{1(0)}$, $x_{2(0)}$, $x_{3(0)}$, $x_{4(0)}$, and $x_{5(0)}$ simply refer to the set of initial values to be used for the next iteration (loop) in the execution of the linear program.

In summary, having applied the first-order Taylor's approximation to linearize the constraint function, we now have a simple set of linear relationships describing the cost and constraint functions as follows:

$$\vec{c}^{\,t}\vec{x} = \textit{Cost} \text{ and } \mathbf{A}\vec{x} = C_{total}, \tag{4.12}$$

where

$$\vec{c} = \begin{bmatrix} A_1^2 + k_2 A_2^2 + k_8 A_8^2 \\ A_3^2 + k_9 A_9^2 \\ A_4^2 + k_{10} A_{10}^2 \\ A_5^2 + k_{11} A_{11}^2 \\ A_6^2 + k_7 A_7^2 \end{bmatrix}, \tag{4.13}$$

$$\mathbf{A} = \left[\frac{\tau_{c1}}{x_{1(0)}^2}, \frac{\tau_{c2}}{x_{2(0)}^2}, \frac{\tau_{c3}}{x_{3(0)}^2}, \frac{\tau_{c4}}{x_{4(0)}^2}, \frac{\tau_{c5}}{x_{5(0)}^2} \right], \text{ and} \tag{4.14}$$

$$\vec{x}^{\,t} = [x_1,\ x_2,\ x_3,\ x_4,\ x_5]\,. \tag{4.15}$$

Using the simplified and linearized cost and constraint functions in the above, and linearizing the constraint equation by the first-order Taylor's approximation at each step of the iteration, we may apply a modified Karmarkar's Rescaling Algorithm [58]. The steps of the iteration algorithm are outlined as follows:

Step 1: Calculate null-space projection.

$$\text{Projection} = P = \vec{c} - \left[\mathbf{A}^t(\mathbf{A}\mathbf{A}^t)^{-1}\mathbf{A}\right]\vec{c}.$$

Step 2: Update function vector (variables).

$$\vec{x}_{(k+1)} = \vec{x}_{(k)} - wP, \quad \text{where} \quad w = \text{weight}.$$

Step 3: Modify updated variable x_5.

$$x_{5(k+1)} = \tau_{c5}\left[C_{total} - \frac{\tau_{c1}}{x_{1(k+1)}} - \frac{\tau_{c2}}{x_{2(k+1)}} - \frac{\tau_{c3}}{x_{3(k+1)}} - \frac{\tau_{c4}}{x_{4(k+1)}}\right]^{-1}.$$

Step 4: Re-linearize constraint function (then go back to Step 1).

$$\mathbf{A} = \left[\frac{\tau_{c1}}{x^2_{1(k+1)}},\ \frac{\tau_{c2}}{x^2_{2(k+1)}},\ \frac{\tau_{c3}}{x^2_{3(k+1)}},\ \frac{\tau_{c4}}{x^2_{4(k+1)}},\ \frac{\tau_{c5}}{x^2_{5(k+1)}}\right].$$

Note that the modification in Step 3 is necessary in order to preserve the fixed C_{total} in the next set of linearized initial conditions established in Step 4.

Directly applying the steps of the algorithm outlined in the above, using the initial values labeled in the schematic of Fig. 4.1, a new fifth-order Bessel filter with the optimized dynamic range via linear programming is calculated as shown in the Fig. 4.2. Note that

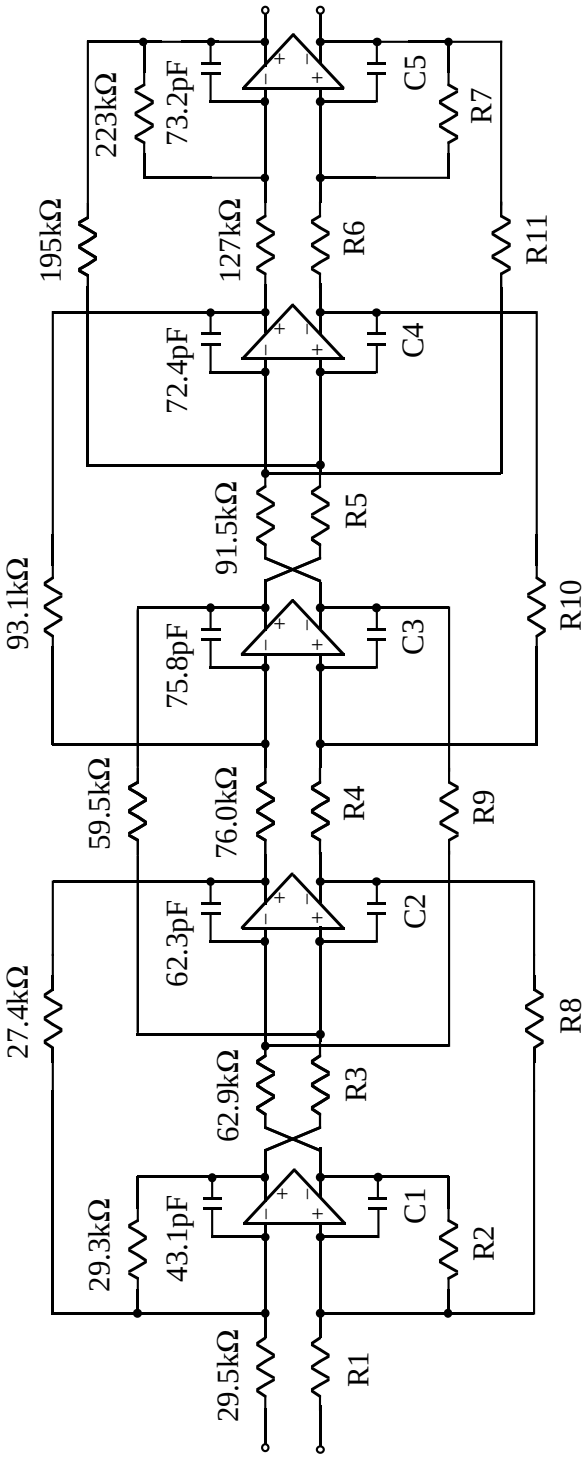


Figure 4.2 RC 5th-order Bessel (Optimized)

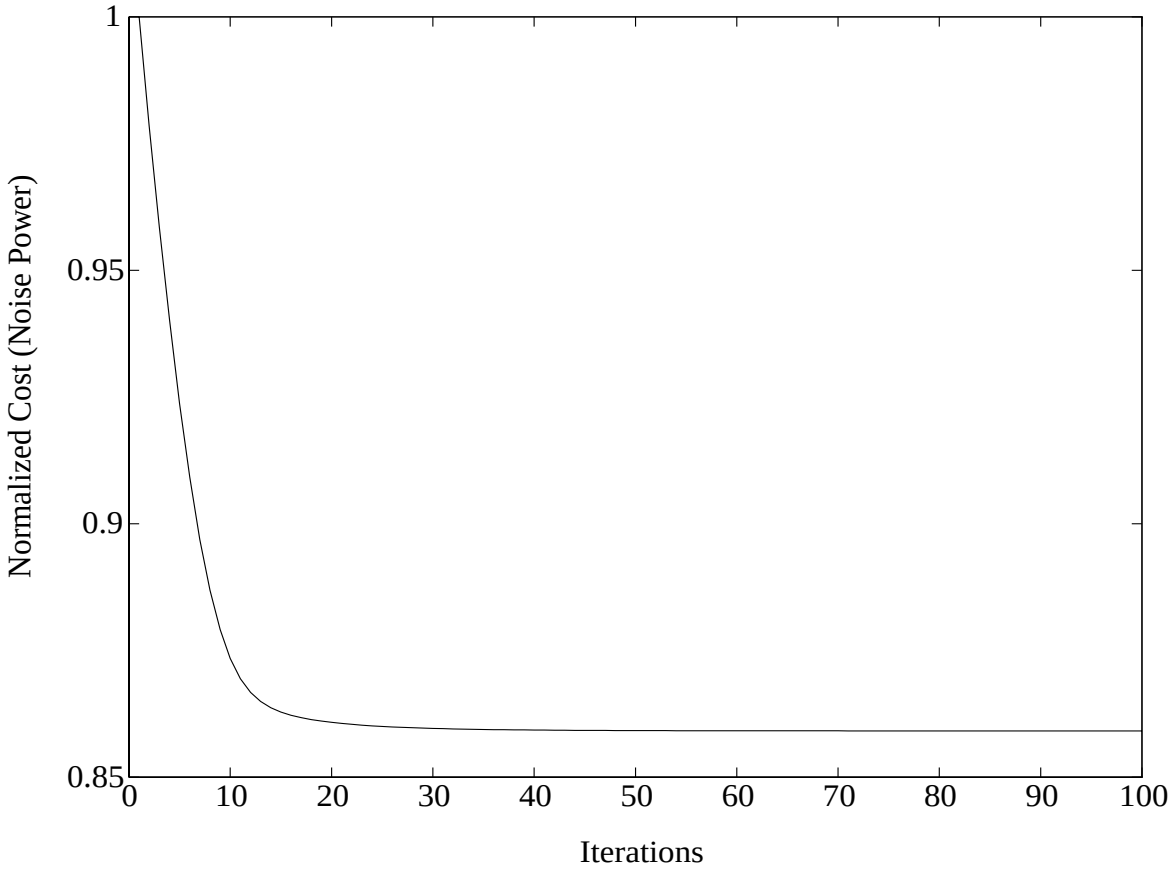


Figure 4.3 Optimization Convergence

despite changes in the sizes of resistors and capacitors (and total capacitance unchanged), the filter displays exactly the same frequency response as the previous filter shown in Fig. 4.1. The rapid convergence of this linearized optimization technique is shown in Fig. 4.3, which displays an incremental improvement in the total noise power.

The equivalent noise at the output of the optimized filter is plotted in Fig. 4.4. The plot shows a further improvement of about 0.7 dB over the standard node-voltage scaled filter. Even though the improvement is not very large, it partly compensates for the incremental reduction of the dynamic range resulting from the linearity improvement technique at no

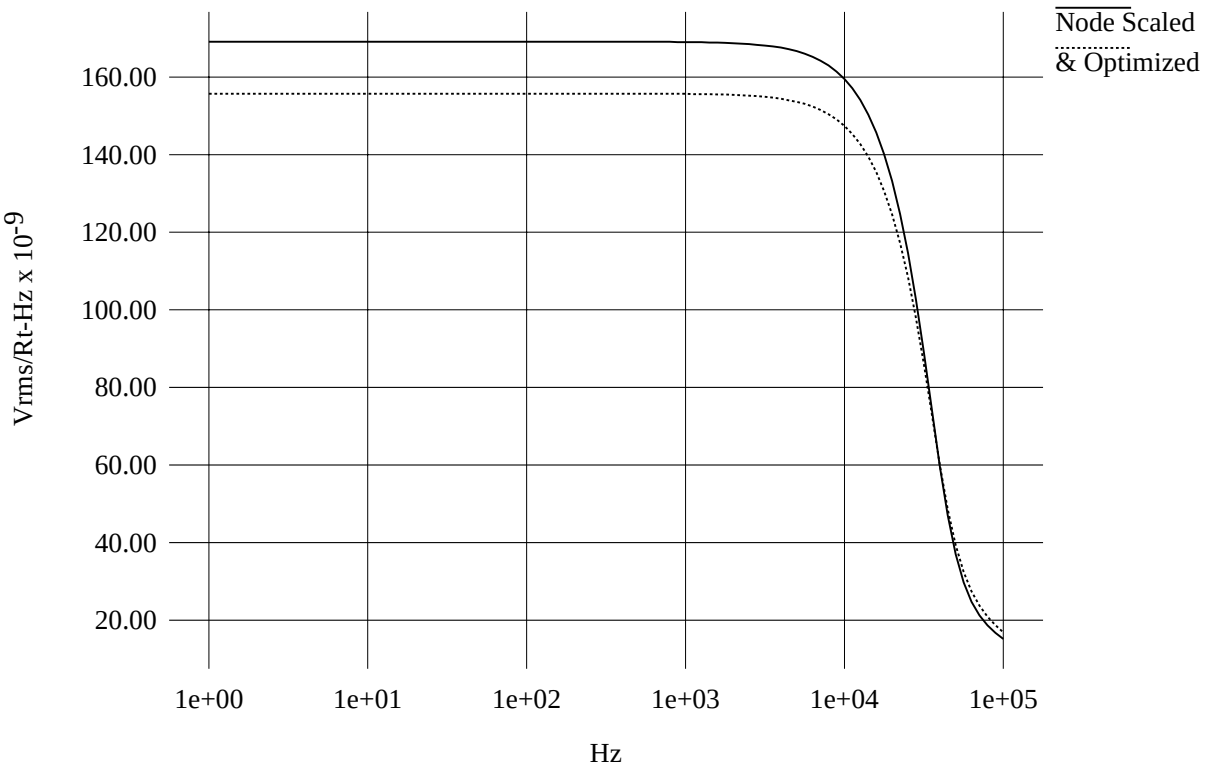


Figure 4.4 Eq Noise at the Output (Optimized)

other cost. A more rigorous linear programming approach can also be implemented by considering the area taken up by the resistors and the influence of the voltage scaling, F, by including the information in the constraint and cost functions. As a whole, this optimization method has shown that, in general, the dynamic range of an active filter can be improved by applying a commonly used linear programming approach with a flexible user-defined constraint function (in this example a fixed total capacitance).

CHAPTER 5

DESIGN OF FIFTH-ORDER BESSEL FILTER

Taking the standard design approach of an active RC filter, derived from the passive LC ladder filter implementation, and then applying newly added transformations and adjustments required for the low-distortion R-MOSFET-C filter implementation, an audio-band (22-kHz) fifth-order Bessel filter is designed and implemented. The filter implementation, down to the level of sizing polygons (layout), had to consider the detailed specification of the Orbit 2-μm Double-Poly N-Well process to appropriately take into account the process and temperature variations of the device parameters. This insures that the designed tunable filter can be self-tuned to a 22-kHz pass band. In the prototype filter, the voltage-scaled factor F varied between 2.5 to 5 (a fixed value for each of the integrators) is implemented for the purpose of THD optimization. Adequate details of the design process will be discussed in this chapter starting from the description of the standard active filter implementation that is familiar to many, continuing to the illustrations for the newly added steps in the design process unique to this R-MOSFET-C filter. Finally, some circuit details such as op amp and bias circuits (automatic tuning circuit already discussed in Chapter 3) will be discussed with corresponding simulation results extending to the overall filter characteristic.

5.1 Standard Active Filter Design

Among the many active filter design methods, the most commonly used configurations consist of cascaded biquads which is built based on a given set of pole locations, and an

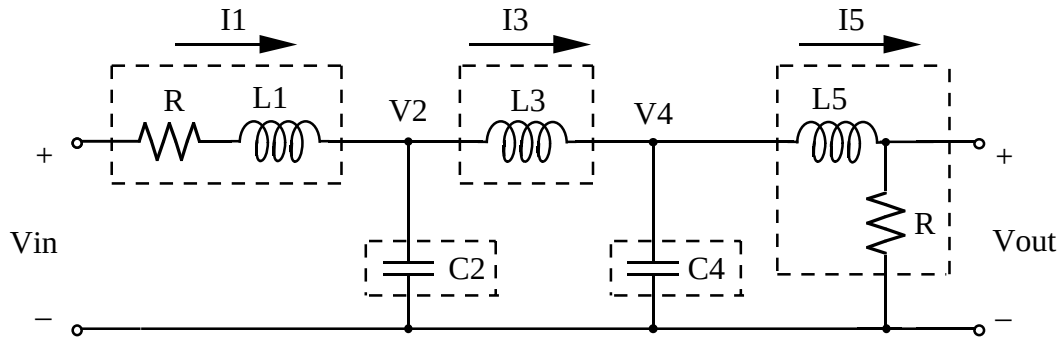


Figure 5.1 Fifth-order LC Ladder Filter

active RC filter derived from the passive LC ladder filter coefficients that are easily obtained from numerous references [53]-[55]. For the prototype filter implemented, the approach derived from the passive LC ladder filter is used. This LC ladder filter implementation is commonly used because of its reduced sensitivity to circuit parameter and coefficient uncertainties [59], [60].

5.1.1 LC ladder to active RC transformation

The fifth-order Bessel LC ladder filter is shown in Fig. 5.1, where the coefficients can be obtained from [53]-[55]. In the LC-ladder-to-active-RC transformation, each of the blocks delineated by dotted lines in the figure is analyzed in detail. Expressing each circuit description in terms of the key variables I_1, V_2, I_3, V_4, and I_5,

$$I_1 = \frac{1}{R + sL_1}\left[V_{in} - V_2\right],$$

$$V_2 = \frac{1}{sC_2}\left[I_1 - I_3\right],$$

$$I_3 = \frac{1}{sL_3}\left[V_2 - V_3\right],$$

$$V_4 = \frac{1}{sC_4}\left[I_3 - I_5\right],$$

$$I_5 = \frac{1}{R + sL_5}\left[V_4\right], \text{ and}$$

$$V_{out} = R\left[I_5\right]. \tag{5.1}$$

For the normalized coefficients, where $R = 1$, these simplify further to

$$I_1 = \frac{1}{1 + sL_1}\left[V_{in} - V_2\right],$$

$$V_2 = \frac{1}{sC_2}\left[I_1 - I_3\right],$$

$$I_3 = \frac{1}{sL_3}\left[V_2 - V_3\right],$$

$$V_4 = \frac{1}{sC_4}\left[I_3 - I_5\right],$$

$$I_5 = \frac{1}{1 + sL_5}\left[V_4\right], \text{ and}$$

$$V_{out} = I_5. \tag{5.2}$$

The systematic configuration equivalent to the expressions given in the above can be arranged in the "leapfrog" configuration as shown in Fig. 5.2. The schematic composed of these symbolic functional blocks and summing nodes (equivalently a signal-flow graph may be used) is mathematically identical to the description of the LC ladder filter from which the equations were derived. From the leapfrog configuration, we can observe that there are two types of unique functional blocks. One is a simple integrator in the form of $1/sC$ and the other is $1/(1 + sC)$. The latter form refers to the transfer function of a damped integrator. The circuit implementation examples for the integrator and the damped integrator are shown in Figs. 5.3 and 5.4. For the integrator shown in Fig. 5.3, using the

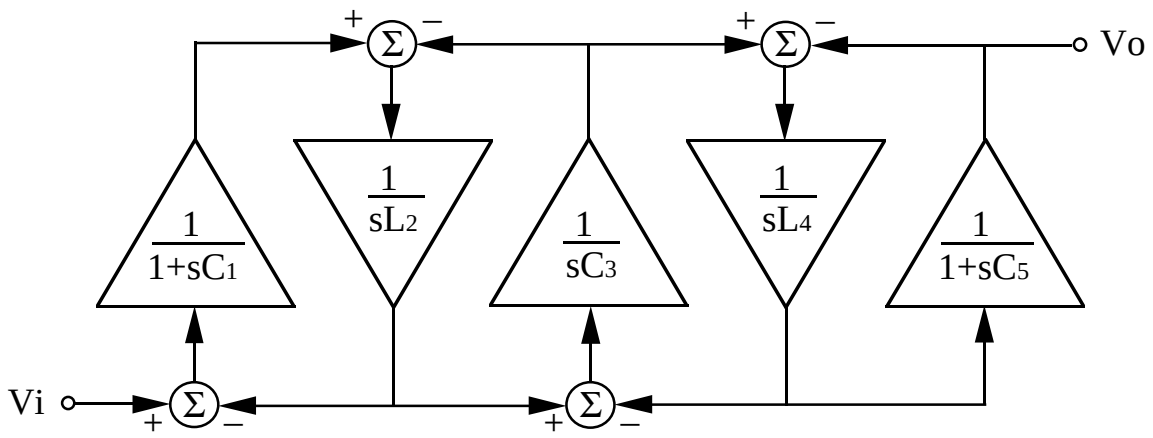


Figure 5.2 Leapfrog Configuration/Implementation

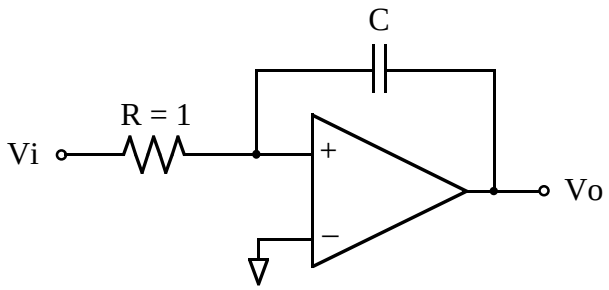


Figure 5.3 Standard Active Integrator

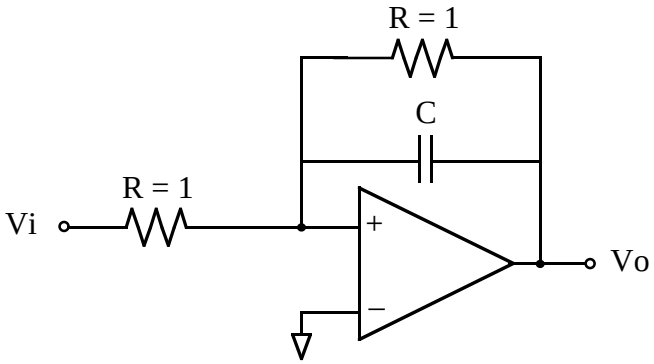


Figure 5.4 Standard Damped Integrator

normalized resistor value $R = 1$, the input-to-output voltage transfer function is $V_o/V_i = 1/sC$, and for the damped integrator shown in Fig. 5.4, the transfer function is $V_o/V_i = 1/(1 + sC)$, again using normalized resistors of $R = 1$.

Table 5.1 Fifth-order Bessel LC Ladder Filter Coefficients

	Normalized LC
R	1.0
L1	0.1743
C2	0.5072
L3	0.8040
C4	1.1110
L5	2.2582

By placing circuit blocks duplicating these two integrators in the corresponding places with the correct coefficient adjustments, one can build an active RC network describing the exact filtering function equal to the LC network of Fig. 5.1. The fifth-order active RC (single-ended version) filter is shown in Fig. 5.5. The inverting (-1) functional blocks intended to maintain the correct polarity can be implemented by a simple inverting configuration of a resistive feedback op amp resulting in unity gain. In the case of a fully differential filter implementation, these extra inverting stages are no longer needed because the fully differential architecture provides and uses both the inverting and noninverting terminals simultaneously.

The normalized coefficients given for a fifth-order Bessel filter, extracted from [54], are shown in Table 5.1. When transformed to the active RC configuration as previously discussed, the inductor and capacitor coefficients shown in Table 5.1 really refer to the capacitors in the active RC setup. In addition, an adjustment has to be made to the capacitors and resistors in order to scale the corner frequency to some value other than 1 rad/sec as given in the normalized LC. The adjustment can be made to either one or both sets of re-

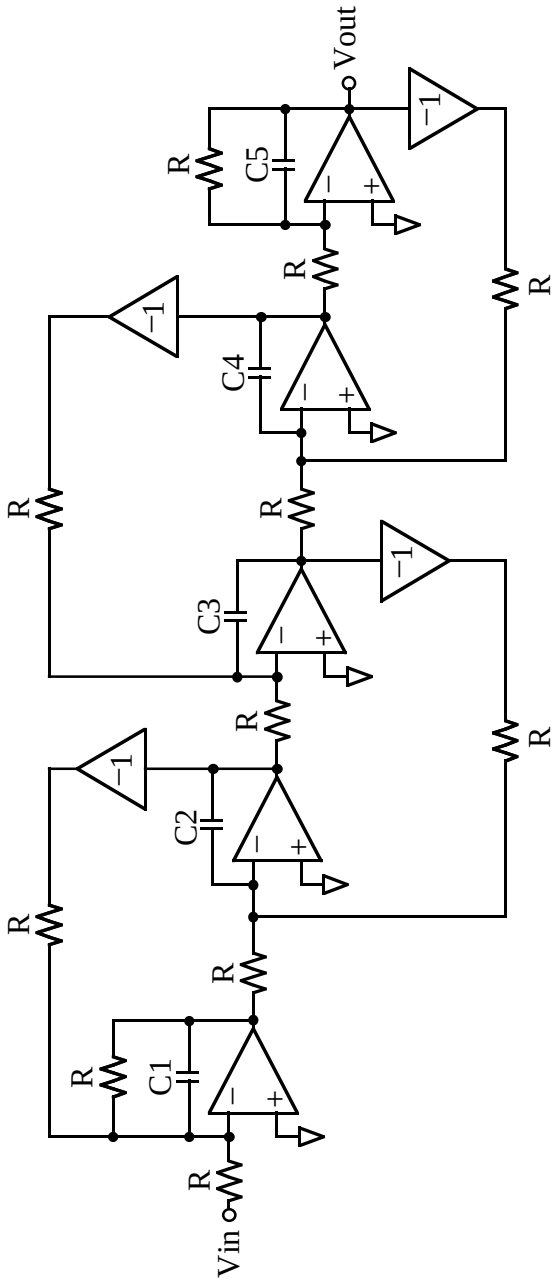


Figure 5.5 Single-ended 5th-order Active RC Filter

Table 5.2 Filter Coefficients Scaled for 22-kHz

	Normalized	Scaled-A	Scaled-B
R	1.0Ω	1.0Ω	81.5kΩ
C1	0.1743F	1.261μF	15.5pF
C2	0.5072F	3.669μF	45.0pF
C3	0.8040F	5.816μF	71.4pF
C4	1.1110F	8.037μF	98.6pF
C5	2.2582F	16.336μF	200pF

sistors and capacitors. Two sets of scaling for the 22-kHz audio-band corner frequency are shown in the Table 5.2. The first set of scaling (Scaled-A) is done in a very straightforward way by increasing all capacitors by the factor, (2π)22k, but the second set of scaling (Scaled-B) uses more reasonably sized capacitors feasible for IC implementation. The fully differential implementation for the fifth-order Bessel filter is shown in Fig. 5.6. The coefficients (resistors and capacitors) reflect the scaled version in the last column of Table 5.2.

5.1.2 Node-voltage scaling

A standard approach to dynamic range improvement that is widely applied in active filter designs is node-voltage scaling. It is mentioned in many references [53]-[57], and a specific example applied directly to this fifth-order Bessel filter design is described in this section.

Analyzing the filter shown in Fig. 5.6, with the corner frequency of the filter normalized to 22-kHz, we find that each output of the five op amps has a frequency-dependent swing

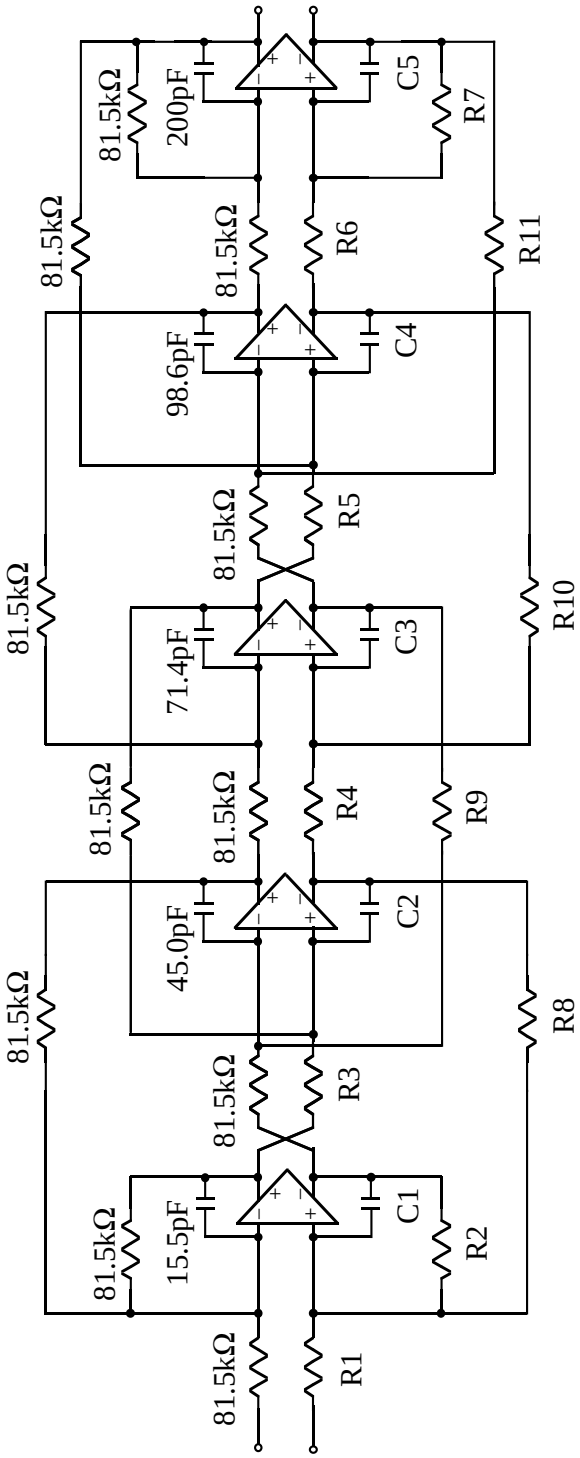


Figure 5.6 Fully Differential 5th-order Bessel Filter

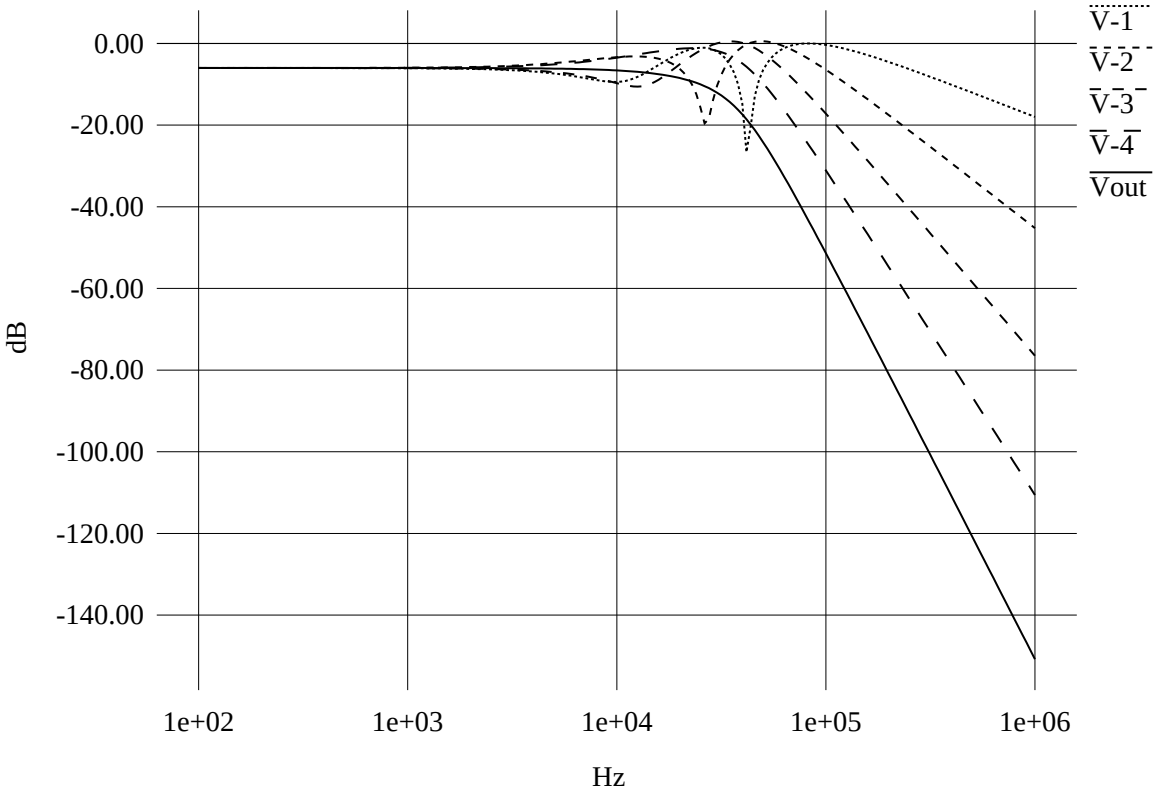


Figure 5.7 Frequency Response of Fifth-order Bessel Filter

that is not quite optimized (i.e., normalized) for maximum dynamic range. Figure 5.7 displays the frequency response of the filter, with each of the five traces representing the output nodes of the five op amps. Because the op amps used in the active filter have a limited amount of voltage swing, it is desirable to utilize their maximum signal swing for the maximum dynamic range (SNR). For example, in the plot shown in Fig. 5.7, the maximum swing (over frequency) at the output node (V_{out}) is approximately 6 dB below 0 dB. Thus the last op amp driving the output only utilizes half of its maximum swing capability. By *raising* this transfer function from the input to the last op amp output (V_{out}) up to 0 dB, the output swing can be approximately doubled (6 dB increase). Similarly, all

outputs of the op amps can be normalized (either by raising or lowering the transfer curve) so that the peak swing over all frequencies of each of the op amp output nodes will line up at 0 dB.

This kind of raising or lowering of the transfer curve (only the constant magnitude change over all frequencies) without affecting the frequency-dependent response, the node-voltage scaling, is done simply by scaling the resistors and capacitor connected at each of the output nodes with the amount of shift (raise or lower) desired. For example, in reference to the schematic in Fig. 5.6, at the output of the last op amp (V_{out}), the capacitor C_5, currently 200 pF, is halved to 100 pF, and the resistors R_7 and R_{11} are doubled. This kind of scaling of the components is repeated for all op amp outputs. For the condition in which the transfer curve is to be lowered (at V_2 for example), the capacitor would be increased and the resistors decreased by the ratio needed for correction.

Once the node-voltage scaling is complete, as the frequency response shows in Fig. 5.8, the peaks of the magnitudes of all transfer curves are normalized to 0 dB, while there is no change in the frequency-dependent response. The schematic of this node-voltage scaled fifth-order Bessel filter has already been shown in Fig. 4.1.

5.2 Added Features in the R-MOSFET-C Filter

Because of the novel implementation of the R-MOSFET-C filter design, using passive resistors and MOSFETs in combination as tunable resistance elements for high linearity, a few additional steps are taken in the design process. One of these additions is simply the active RC to R-MOSFET-C transformation, and the second is a minor THD optimiza-

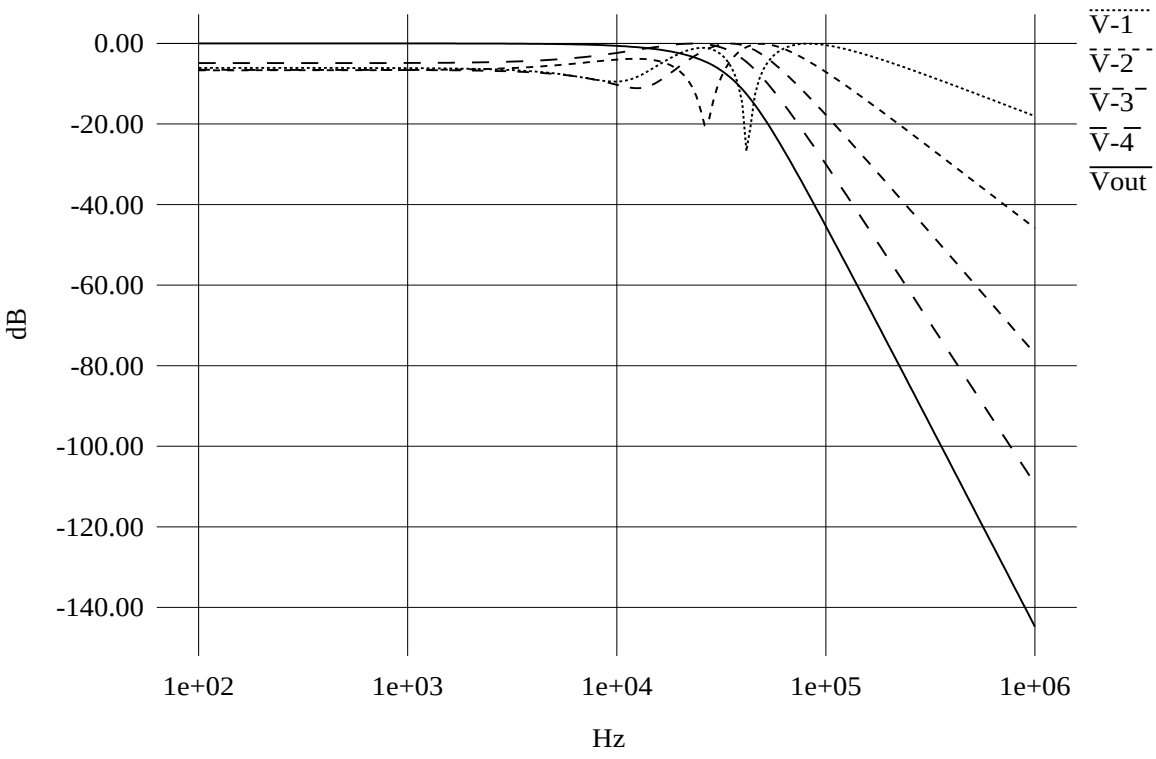
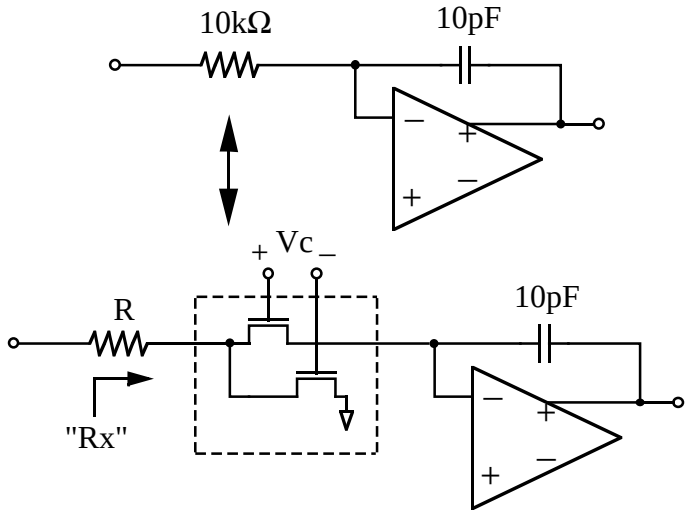


Figure 5.8 Frequency Response of Node-voltage Scaled Filter

tion method named *constant-voltage* R-MOSFET scaling. Both of these enhancements take place after a standard active RC filter has been designed. Thus, in most cases, an experienced filter designer can simply add on these changes to his existing design. Before describing these additional steps in detail, recall that in the design of this prototype filter the dynamic optimization method using the linear programming approach as discussed in Chapter 4 takes place before these additional changes.

5.2.1 Active RC to R-MOSFET-C transformation

As discussed in Chapter 2 with a particular focus on the R-MOSFET portion, each of the resistors in an active RC filter implementation must undergo a transformation resulting in a variable R-MOSFET resistor and a highly linear R-MOSFET-C implementation. In the example shown in Fig. 5.9, the R-MOSFET combination, $R + R_X$, represents a sum that is equal to the original single resistor, 10 kΩ (in the standard RC), and the capacitor value, 10 pF (arbitrary), stays unchanged. Because the parallel combination of the two MOSFETs in triode, R_X, is independent of the frequency tuning differential control voltage, V_C, the voltage scale factor, $F = [R + R_X]/R_X$, is maintained at any V_C, and this differential control voltage tunes the variable resistance by current shunting. Once this active RC to R-MOSFET-C transformation has taken place in either the criss-cross or the current-dumping configuration (discussed in Section 2.2), the multiple-input loading effect is compensated by adjusting the size of the passive resistors as discussed in detail in Section 2.2.3.

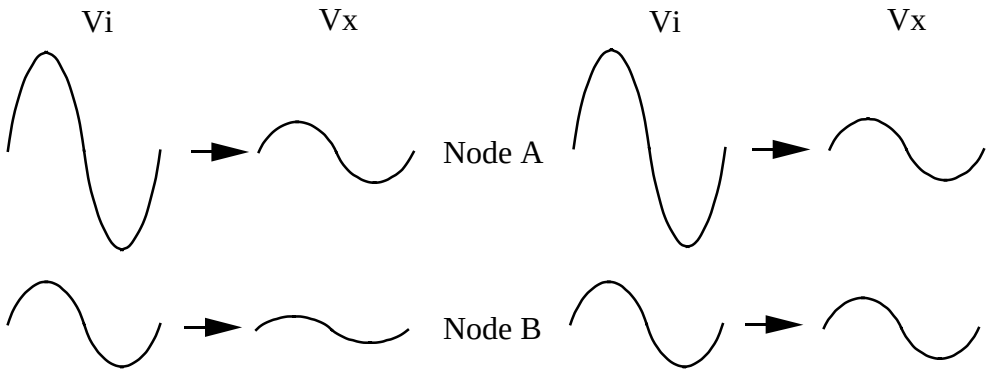


F = (R+Rx)/Rx and R+Rx = 10kΩ

Figure 5.9 Active RC to R-MOSFET-C Transformation

5.2.2 Constant-voltage R-MOSFET scaling

Even though one can choose a constant *ratio* for the R-MOSFET voltage scaling uniformly throughout the filter (recall from the example in the preceding section that $F = [R + R_X]/R_X$), a more optimum choice of voltage scale factor, F, can be used for each of the summing nodes in order to minimize the larger noise due to a larger F. This noise and voltage scale factor trade-off relationship has been discussed in Section 2.2.2. The optimum choice of voltage scale factor, F, can be achieved by applying a constant-*voltage* R-MOSFET scaling. This approach ensures a fixed amount of voltage swing across the MOSFETs (which is approximately proportional to distortion) rather than allowing one tuning element to have the largest signal swing, thereby causing it to be the dominant source of distortion. Shown in Fig. 5.10 is a graphical illustration of this method. The illustration in Fig. 5.10(a) shows that the node B of the constant-ratio scaling results in an



(a) Constant-ratio (b) Constant-voltage

Figure 5.10 Constant-Ratio vs. Constant-Voltage Scaling

unnecessarily small voltage swing across the MOSFETs. On the other hand, for node B in Fig. 5.10(b), the constant-voltage scaling allows the signal swing across the MOSFETs to be comparable to that for node A. The net result is an improvement in the dynamic range due to the reduced F at the particular node B with a negligible sacrifice in the linearity performance.

This constant-voltage scaling method really narrows down to shifting the weight of linearity versus dynamic range optimization towards the lower frequency portion of the filter. Even though each of the op amp output nodes are node-voltage scaled to the 0 dB level as explained in Section 5.1.2, for most of the pass band, the signal level is well below 0 dB for many of these nodes. This was shown earlier in Fig.5.8. In the prototype filter implemented, a set of constant-voltage scaling factors was chosen with approximate measures and the final choice was made based on a wide range of iterative simulation results. The end result of this constant-voltage scaling (F=2.5-5) on dynamic range and

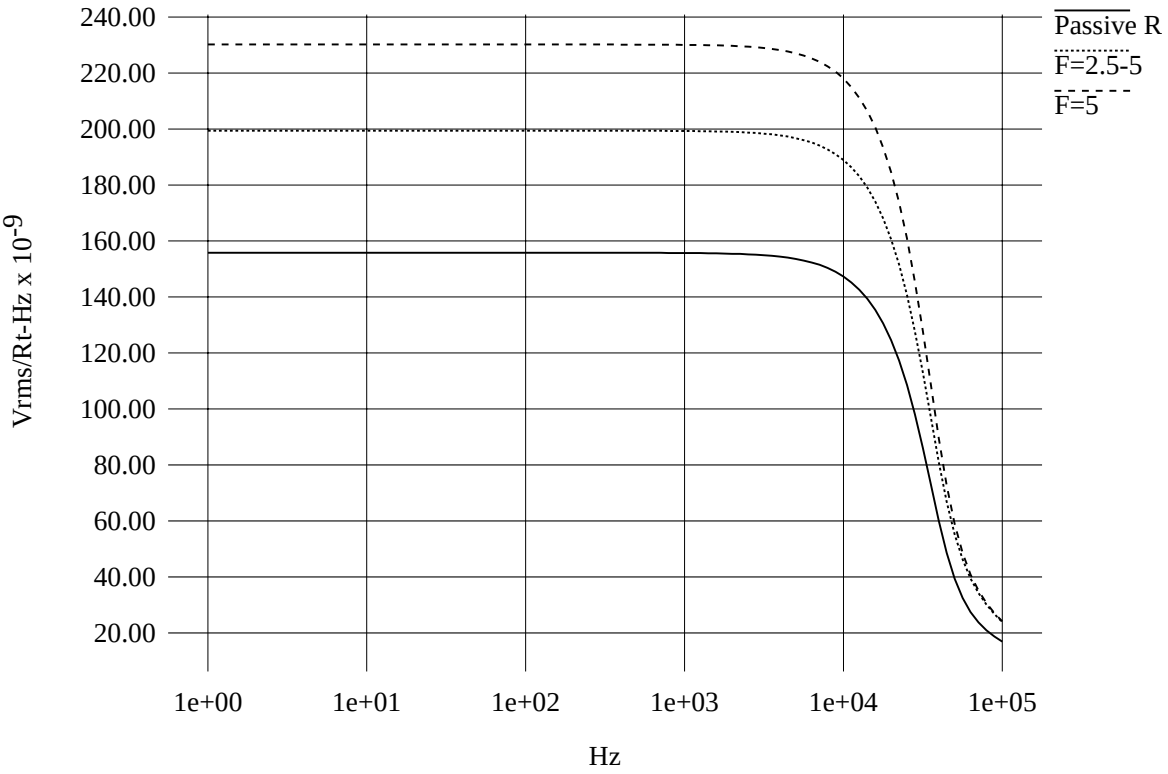


Figure 5.11 Eq Noise (Placement of Constant-Voltage Scaling)

distortion has been presented in Figs. 2.15 and 2.25. These results can now be observed in the context of the constant-ratio scaling (fixed at F=5). Figure 5.11 shows the improvement of equivalent noise at the output of the filter for the case of varied voltage scale factor, F=2.5-5, from a fixed value, F=5. Also, the simulation result shown in Fig. 5.12 is the amount of linearity performance that was "sacrificed" for the varied voltage scale factor, F=2.5-5, in comparison to a fixed voltage scale factor, F=5. The meaning of the term "negligible sacrifice" is less clear here, and the choice becomes more of a specific design issue, but a similar approach to improve the dynamic range using a fixed voltage scaling factor can not achieve the same linearity performance obtained by this constant-voltage

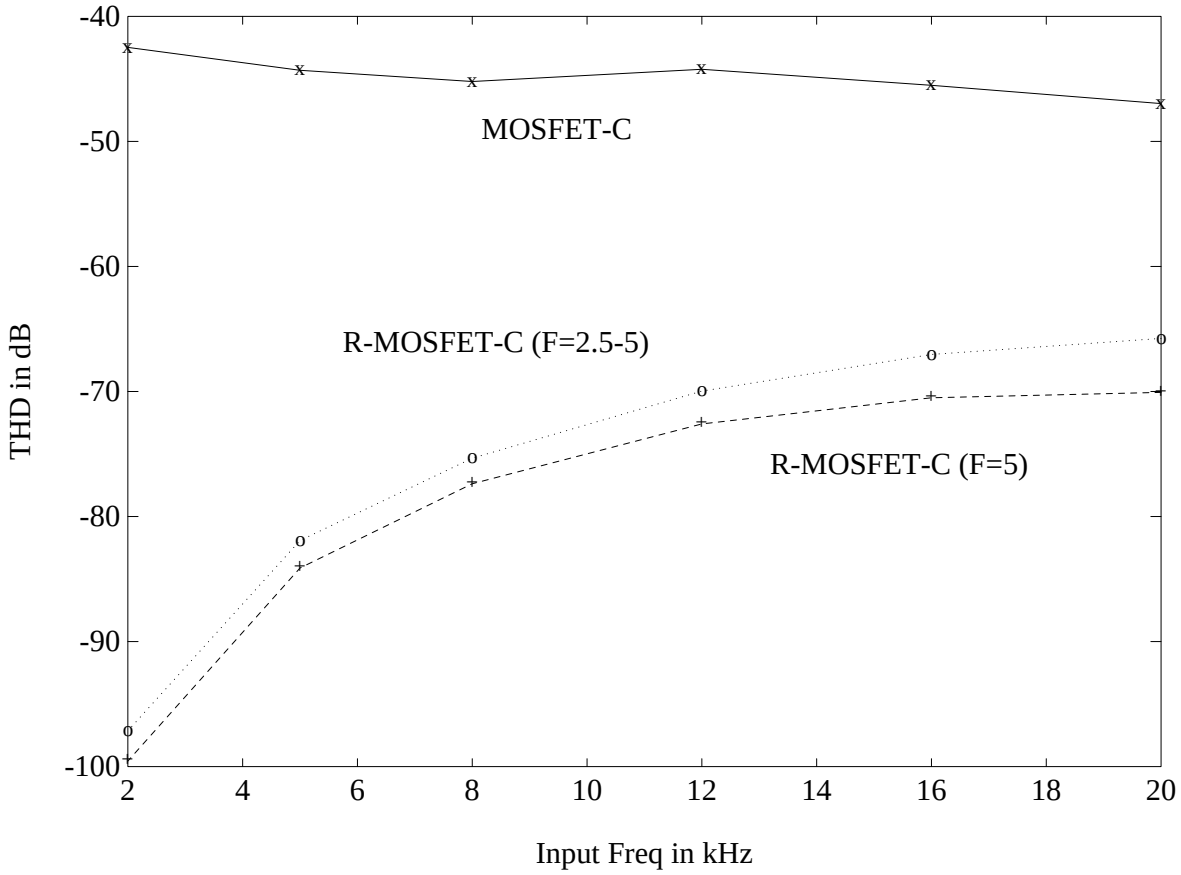


Figure 5.12 Placement of Constant-Voltage Scaling

R-MOSFET scaling.

5.3 Circuit Description

The schematic for the final implementation of the prototype fifth-order Bessel filter using the linearity improvement technique is shown in Fig. 5.13. The box with the crossing arrows indicates the current steering portion of the variable resistance stage with the current-dumping topology (see Section 2.2.1 for details), and the voltage scale factor, F, given at each of the tunable elements, is the value assigned according to the constant-voltage scaling (see Section 5.2.2). As observed in the preceding section, the progression of the filter coefficients reflects a series of transformations, as summarized in Table 5.3. Table 5.3 captures the changes of the coefficients starting from the LC ladder filter. The columns further summarize the LC-ladder-to-active-RC transformation, node-voltage scaling, dynamic range optimization by linear programming (Chapter 4), and, finally, active RC to R-MOSFET-C transformation. The direct schematic representation of the coefficients in the last column is the filter shown in Fig. 5.13.

Other circuit blocks of interest, to be described in the following, include a high-gain operational amplifier, a dc-current bias, and a right-half-plane zero-cancellation bias circuit, and a few miscellaneous blocks such as noncritical single-ended op amps used in the automatic tuning circuit, tunable current-steering MOSFETs in triode, and a nonoverlapping clock generator. The automatic tuning circuitry as a whole has already been discussed in detail in Chapter 3, and a similar discusssion will not be repeated here.

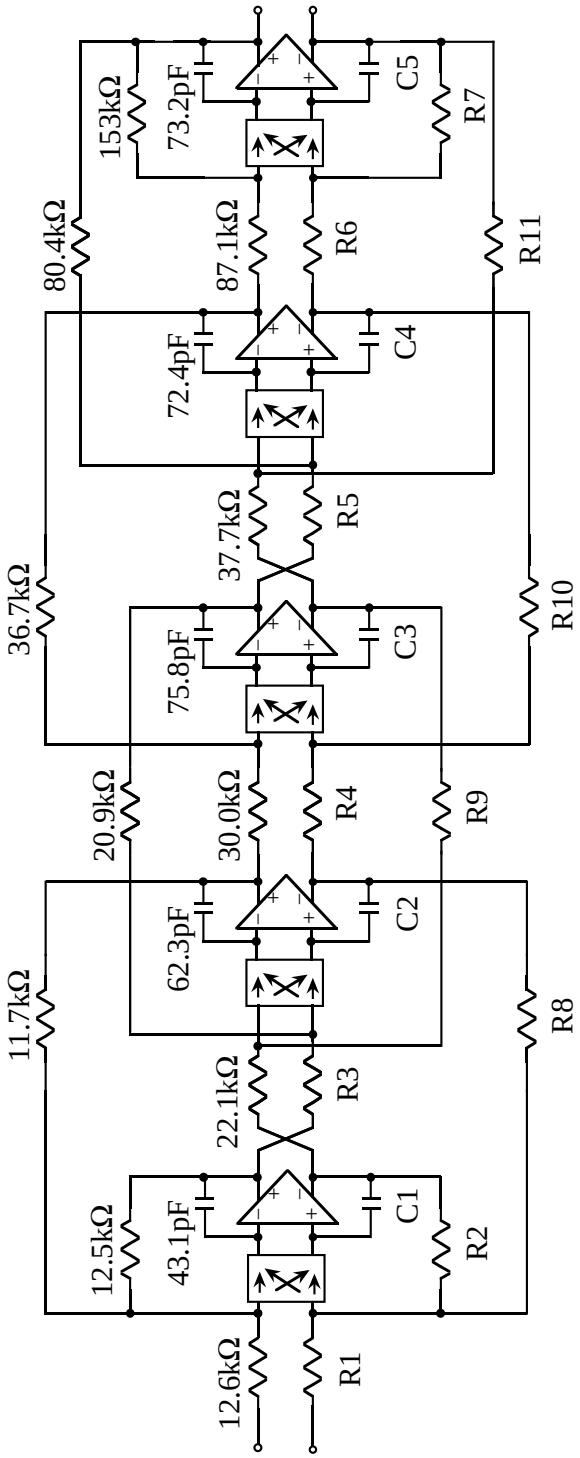


Figure 5.13 Fifth-order Bessel Filter

Table 5.3 Progression of Filter Coefficients

LC	RC	NS	Optimized	R-MOSFET-C
L1=0.1743	C1=15.5pF	15.6pF	43.1pF	43.1pF
C2=0.5072	C2=45.0pF	48.4pF	62.3pF	62.3pF
L3=0.8040	C3=71.4pF	76.0pF	75.8pF	75.8pF
C4=1.1110	C4=98.6pF	86.6pF	72.4pF	72.4pF
L5=2.2582	C5=200pF	100pF	73.2pF	73.2pF
R=1.0000	R=81.5kΩ	R1=81.5kΩ	29.5kΩ	12.6kΩ
		R2=80.9kΩ	29.3kΩ	12.5kΩ
		R3=80.9kΩ	62.9kΩ	22.1kΩ
		R4=75.8kΩ	76.0kΩ	30.0kΩ
		R5=76.5kΩ	91.5kΩ	37.7kΩ
		R6=92.8kΩ	127kΩ	87.1kΩ
		R7=163kΩ	223kΩ	153kΩ
		R8=75.8Ω	27.4kΩ	11.7kΩ
		R9=76.5kΩ	59.5kΩ	20.9kΩ
		R10=92.8kΩ	93.1kΩ	36.7kΩ
		R11=163kΩ	195kΩ	80.4kΩ

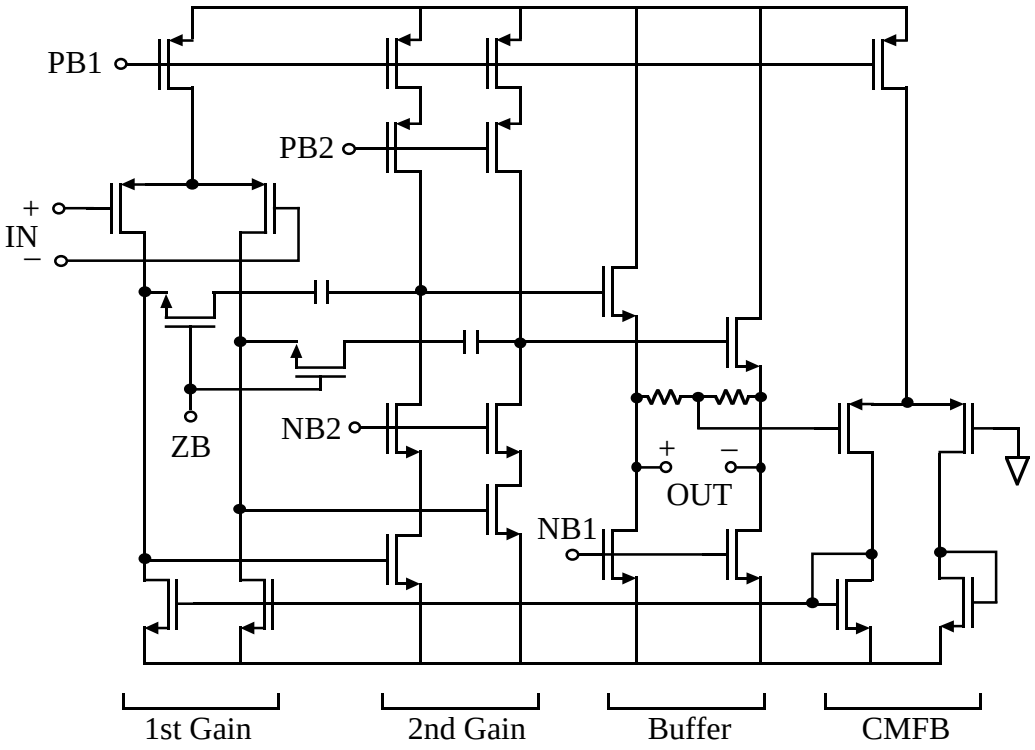


Figure 5.14 Two-stage Operational Amplifier

5.3.1 Operational amplifier

A two-stage, high-gain operational amplifier was chosen in the design to minimize the distortion of the filter that would result from the op amps. The operational amplifier with its frequency compensation network (standard Miller compensation with right-half-plane zero cancellation) is shown in Fig. 5.14. For the right-half-plane zero cancellation, some "tweaking" was necessary using simulation results. As shown in the simulation results in Figs. 5.15 and 5.16, this two-stage $(g_m r_o)^3$ gain op amp displays a dc gain of 98 dB, a 27-MHz unity-gain bandwidth, and a 69^o phase margin. These frequency responses include loading effects at the output of the op amp in an active filter implementation. The simulation results have shown that the open-loop transfer function of the op amp (in the

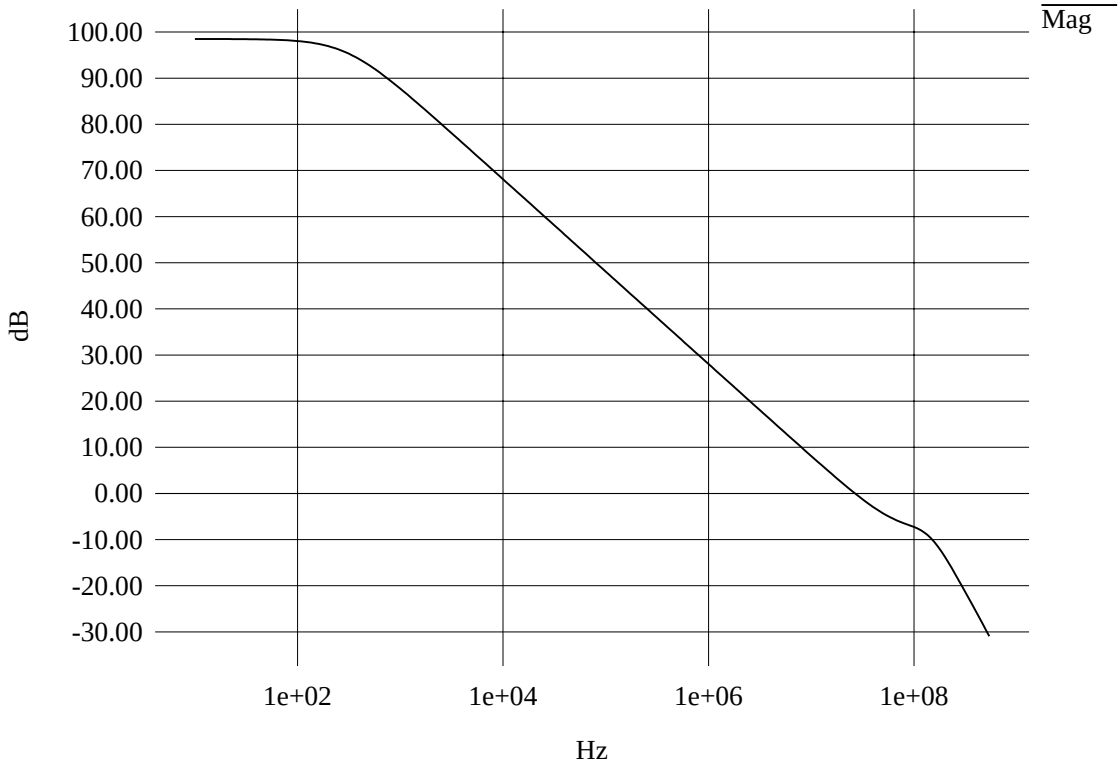


Figure 5.15 Op Amp Magnitude Frequency Response

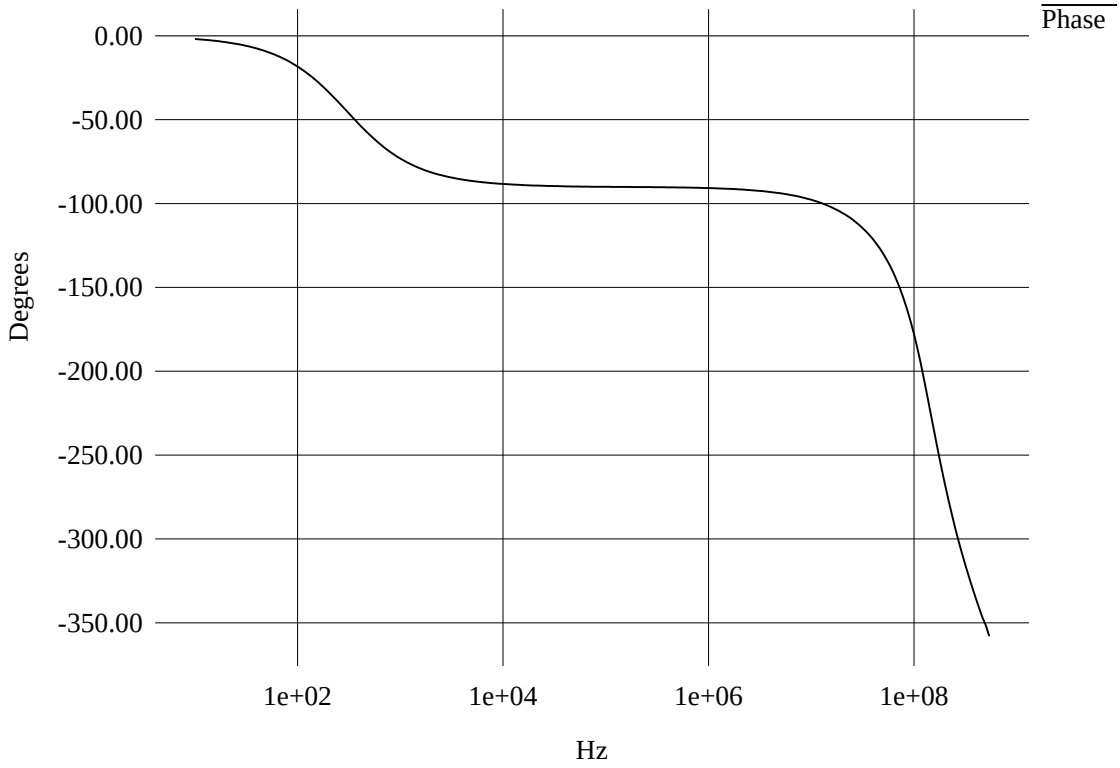


Figure 5.16 Op Amp Phase Frequency Response

"linear" range) has a THD of about -40 dB, but because the op amp operates under a nearly unity-gain closed-loop configuration in the filter setting, the distortion resulting from the op amp is reduced by the amount of the loop gain. For the signals in the audio band (22-kHz), this 27-MHz unity-gain op amp sees a loop gain of at least 60 dB (and even more towards lower frequencies since the dc gain is 98 dB), and the THD resulting from the op amp in the closed-loop configuration is expected to be below -100 dB.

In combination with the resistors (25 kΩ each) used in the common-mode feedback portion, the source-follower output buffer stage of the op amp is able to drive up to 4 kΩ (each output node) for a maximum 2 V_{p-p} swing (4 V_{p-p} differential) by running 400 μA in each branch. The sum of all currents in the op amp is 1.5 mA, resulting in a total power consumption of 7.5 mW per op amp with a 5-V supply.

A single common-mode feedback control is used in this op amp design for simplicity even though one can implement a two-stage design with two sets of common-mode feedbacks controlling the floating output nodes of the first and second stages separately. Another convenient feature of this single common-mode feedback control is that the common-mode loop sees the same frequency compensation network of the signal path. Some resizing of the transistors might be necessary in the common-mode loop in order to insure a comfortable margin of stability of the common-mode feedback loop. The magnitude and phase frequency response simulations of the common-mode loop show a dc gain of 97 dB and the phase margin of 78^o at the unity-gain frequency of 10-MHz.

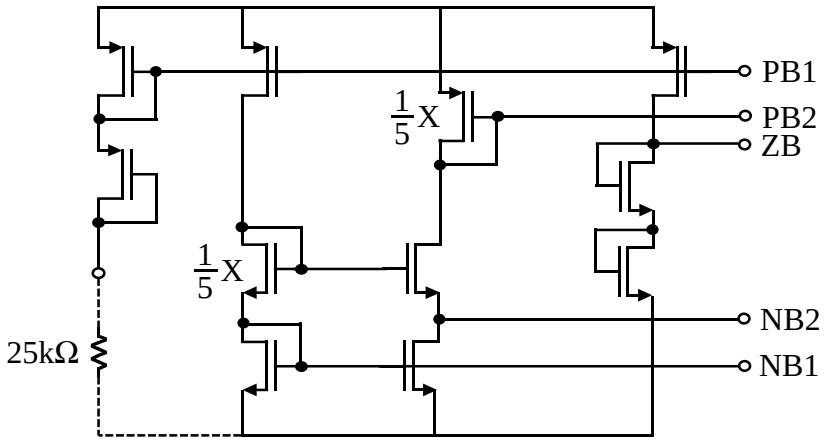


Figure 5.17 Current and Voltage Bias Circuit

5.3.2 Bias circuit

Straightforward cascoded maximum-signal-swing bias circuitry is implemented as shown in Fig. 5.17. This bias circuit feeds all current sources on the chip, and the bias voltage for the zero-cancellation portion of the frequency compensation network is also generated here.

The ultimate reference current is set by an external resistor about the size of 25 kΩ, which should yield approximately a 100 μA reference value. And by simple transistor stacking, using a ratio of 1/5 (ideally 1/4 with an added safety margin), the NB2 node is set at $V_{th} + \sqrt{5}\Delta$, where Δ is the gate access voltage, $V_{GS} - V_{th}$, of the bottom transistors (current sources). As seen in the op amp of Fig. 5.14, when this node NB2 biases the cascode transistor, the V_{DS} of the bottom transistor current source biased by the node NB1 becomes

$$(V_{th} + \sqrt{5}\Delta) - (V_{th} + \Delta) = (\sqrt{5} - 1)\Delta.$$

This would just be Δ if the simple ideal ratio 1/4 is used in the transistor stacking. The

net result is maximum signal swing allowed in the use of the cascode while insuring that the current sources stay out of the triode region of operation. The upper portion of the bias circuit should also be set up by a similar method, but a "lazy" method has been chosen in this case, setting up approximately a $V_{th} + \sqrt{5}\Delta$ voltage drop from the positive supply to the node PB2. Depending upon the size of voltage supplies, the channel length modulation effect (λ) may have to be taken into account.

The other bias voltage to note is the node ZB, where it biases the zero-cancellation part of the op amps that are used in the filter portion of the chip. Transistor stacking attempts to replicate the transconductance, G_{m2}, of the second stage of the op amp. Some "tweaking" was necessary according to simulation results.

5.3.3 Miscellaneous circuit blocks

A part of the remaining circuit implementation includes standard two-stage differential-input single-ended output Miller-compensated op amps (shown in Fig. 5.18) used in various portions of the automatic tuning circuitry and a single-transistor buffer (shown in Fig. 5.19). In reference to the automatic tuning circuitry shown in Fig. 3.4, the op amp with the unity feedback driving V_{C+} refers to the single-transistor buffer. And for the singled-ended op amp of Fig. 5.18, various forms are implemented including an op amp with an N-channel source-follower buffer instead of the P-channel buffer as shown in the figure. A similar op amp without the source follower is also used when driving a purely capacitive load. Given that the performances of these stages are not very critical, these circuit blocks take up only a small proportion of the layout space and consume a negligible amount of power

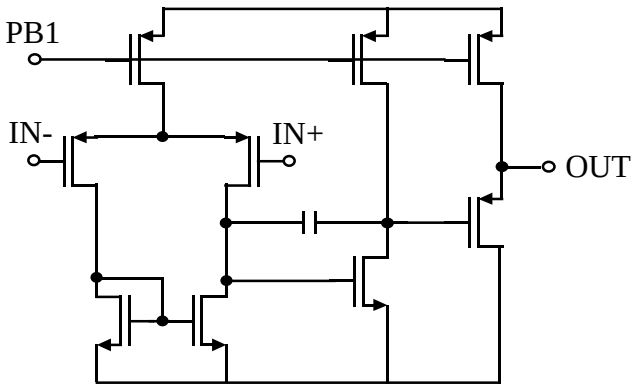


Figure 5.18 Single-ended Operational Amplifier

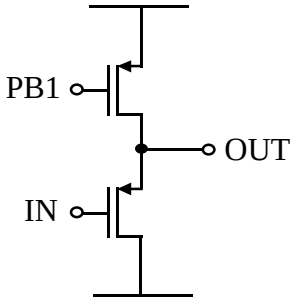


Figure 5.19 Single-transistor Buffer

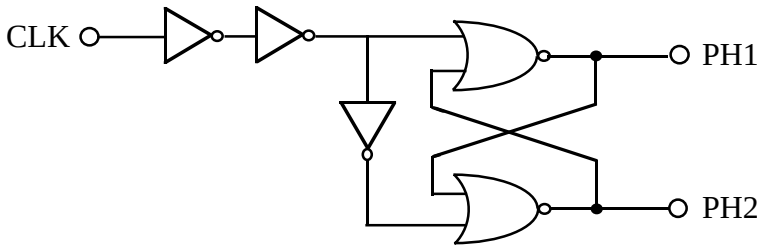


Figure 5.20 Nonoverlapping Clock

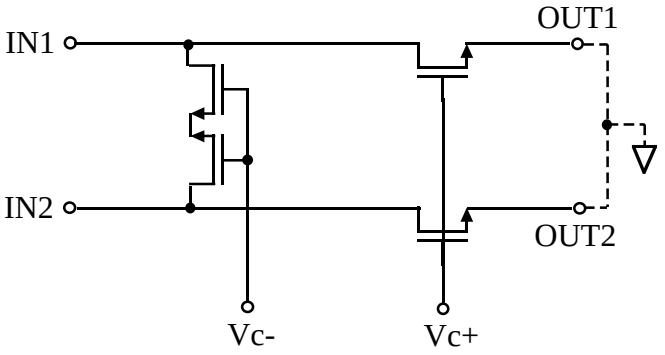


Figure 5.21 Current-steering MOSFETs in Triode

(in comparison to the op amps used in the filter).

The logic-level schematic of the nonoverlapping clock generator driving the switched-capacitor portion (in the automatic tuning circuitry) and the current-steering MOSFETs in triode (the box with crossing arrows in Fig. 5.13) are shown in Figs. 5.20 and 5.21, respectively. The sizes of the current-steering MOSFETs at each of the op amp summing nodes vary between $W/L = 15/30$ and $W/L = 97/30$. The ratios between them are more crucial here as the common-mode control voltage, V_{CM}, takes care of the absolute values by adjusting to the desired voltage scaling factor, F. This is discussed in Section 3.2.1. Also note that the first two MOSFETs on the left which *dump* the currents are not tied to the signal ground. Because of the inherent symmetry of the differential architecture, the

sources of these MOSFETs are allowed to float. The cancellation of differential currents maintains this node very close to the signal ground without any ill effects.

5.4 Simulation Results

Drawing directly upon the circuit description of the preceding section, various simulation results were obtained. In the simulations of this Bessel filter, extended-precision numerical calculations were used with a particular interest in harmonic distortion results. Given the high-gain operational amplifier design, the main source of distortion is expected to be the MOSFET transistors, and the passive resistors are assumed to be linear. The key focus in the simulation results is not so much on the absolute quantities but on the relative change, either an improvement or a degradation, from a meaningful reference.

The resulting frequency response of the filter, in comparison to an all-passive-resistor active RC filter, is shown in Fig. 5.22. The tuning capability from a normalized frequency f_{-3dB} of about 1 to 3 is demonstrated. For the same tuning range, Fig. 5.23 displays its maximally flat group delay characteristic of the Bessel filter. The comparison to an active RC verifies the proper operation of the R-MOSFET-C implementation. The differences in the frequency response are nearly indistinguishable, and the fixed group delay observed in the passband is close to ideal.

Regarding simulation results for the performance measure of linearity, we may recall a few figures from Chapter 2. The differences between Figs. 2.26 and Fig. 2.27 show a considerable improvement in linearity for the R-MOSFET-C implementation from the exemplary comparison, the MOSFET-C filter. These results refer to a 4 V_{p-p} differential

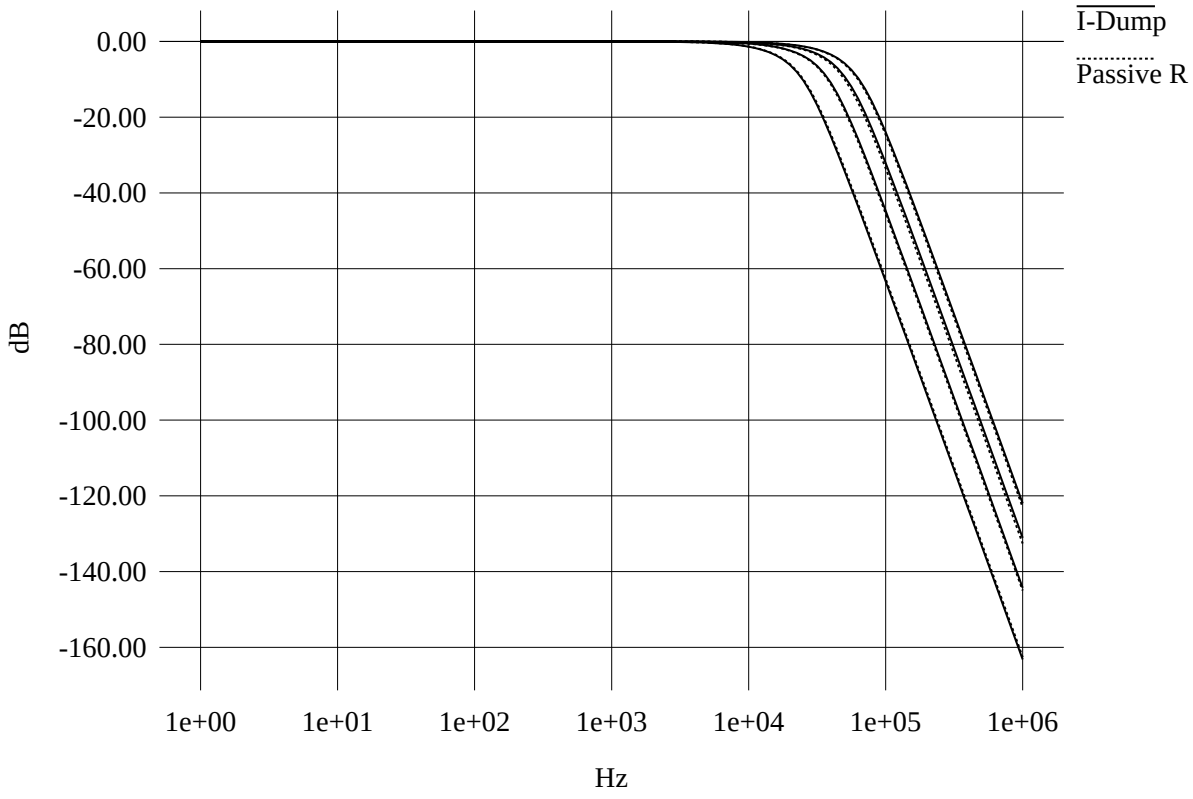


Figure 5.22 Frequency Response (F=2.5-5)

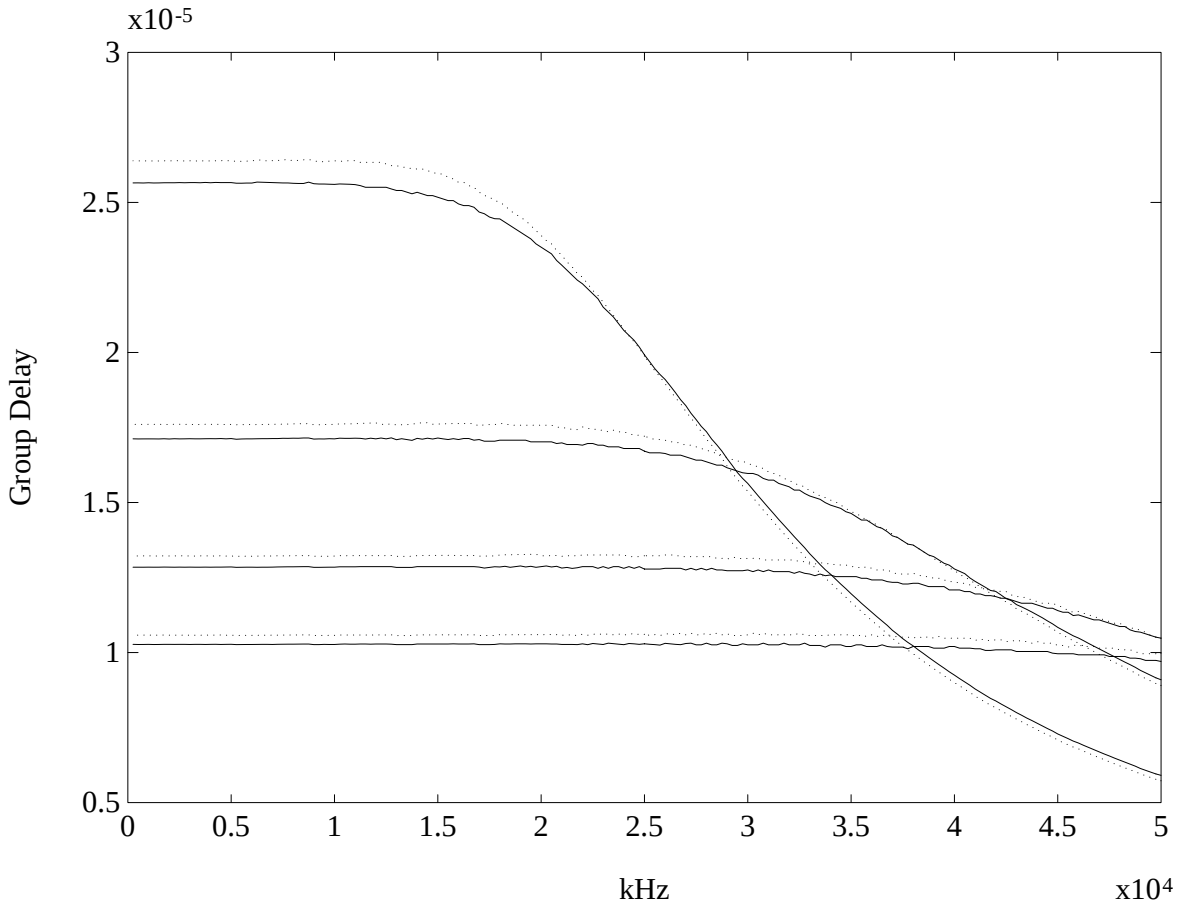


Figure 5.23 Group Delay (F=2.5-5)

input at 2 kHz. In the simulation, a 1% mismatch of W/L, μ, V_{thO} and γ was assumed in the worst-case combination to cover a reasonable range of mismatch. As presented in Chapter 2 in the context of linearity improvement, the THD at different input frequencies is plotted in Fig. 2.25, where the R-MOSFET-C filter achieves about 50 dB improvement over the conventional MOSFET-C filter at 2 kHz 4 V_{p-p} differential input. Note, once again, the effect of the feedback loop gain on distortion. As the input frequency approaches the filter pass-band edge, the loop gain is reduced and the distortion increases.

Other various simulation results relating to total equivalent output noise, automatic tuning circuitry, and dynamic range optimization were presented in Sections 2.2.2, 3.2, and 4.3. Finally, the true measure of performance, the laboratory measurements of the prototype filter, are presented in the following chapter.

CHAPTER 6

EXPERIMENTAL RESULTS

Considering the process and temperature variations of the device parameters and the loading effect of the multiple inputs, an audio-band (22 kHz) fifth-order Bessel filter with a voltage scaling factor, F, varied between 2.5 to 5 (a fixed value for each of the integrators–Section 5.2.2) was designed and fabricated using a double-poly 2-μm CMOS technology. The design steps include an LC ladder to active RC filter transformation, node-voltage scaling, dynamic range optimization with area constraint (Chapter 4), and finally active RC to R-MOSFET-C transformation using constant-voltage scaling (material covered in Chapter 5). In the design verification phase of the Bessel filter, simulations were performed using extended precision in numerical calculations with a particular interest in harmonic distortion results. The measurements presented in this chapter are in good agreement with the predicted results from the simulation (Section 5.4).

Recall that the schematic in Fig. 5.13 is the final prototype R-MOSFET-C fifth-order Bessel filter using the linearity-improvement technique. The box with the crossing arrows is the current-steering portion of the variable resistance stage, and the voltage scale factor, F, given at each of the tunable elements, is the value assigned according to the constant-voltage scaling. Two-stage fully differential operational amplifiers with approximately 98 dB dc gain, 27 MHz unity-gain bandwidth, and 69^o phase margin (from simulation) are used in the filter (see Section 5.3.1 for details). Because of the use of these high-gain

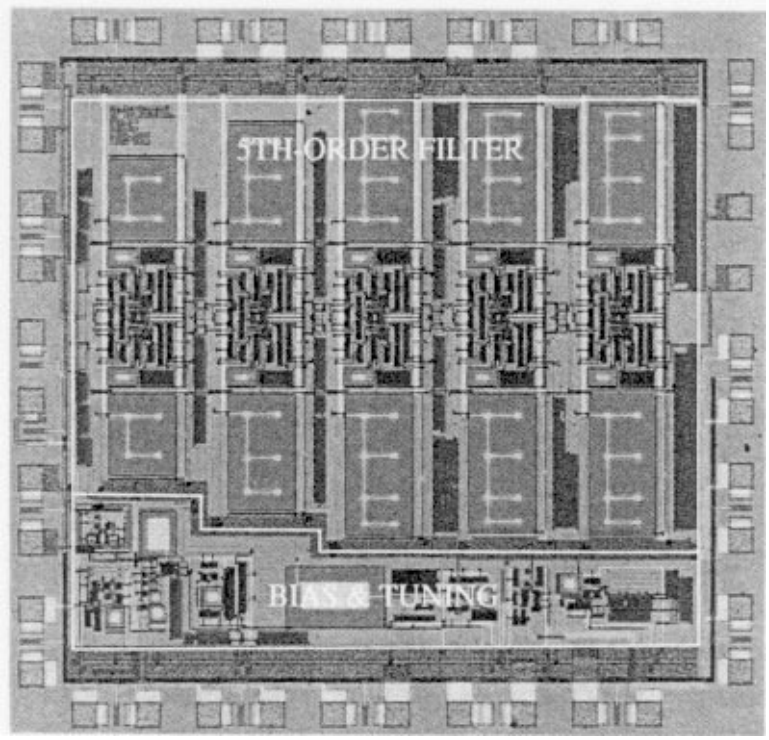


Figure 6.1 Die Photo of the Chip

op amps in the filter, the majority of the distortion is expected to come from the MOS transistors operating in triode, and the passive resistors (undoped poly) are also expected to be sufficiently linear. Shown in Fig. 6.1 is a microphotograph of this fifth-order Bessel filter. The upper portion is composed of the five R-MOSFET-C integrators including the passive components (R's and C's), and the lower portion consists of the filter tuning circuitry and the bias circuit.

The measured frequency responses shown in Fig. 6.2 demonstrate the tunability of the filter. Three different corner frequencies are chosen by using different digital word settings for the set of binary-weighted capacitors which take the place of C_1 in Fig. 3.4 (discussed

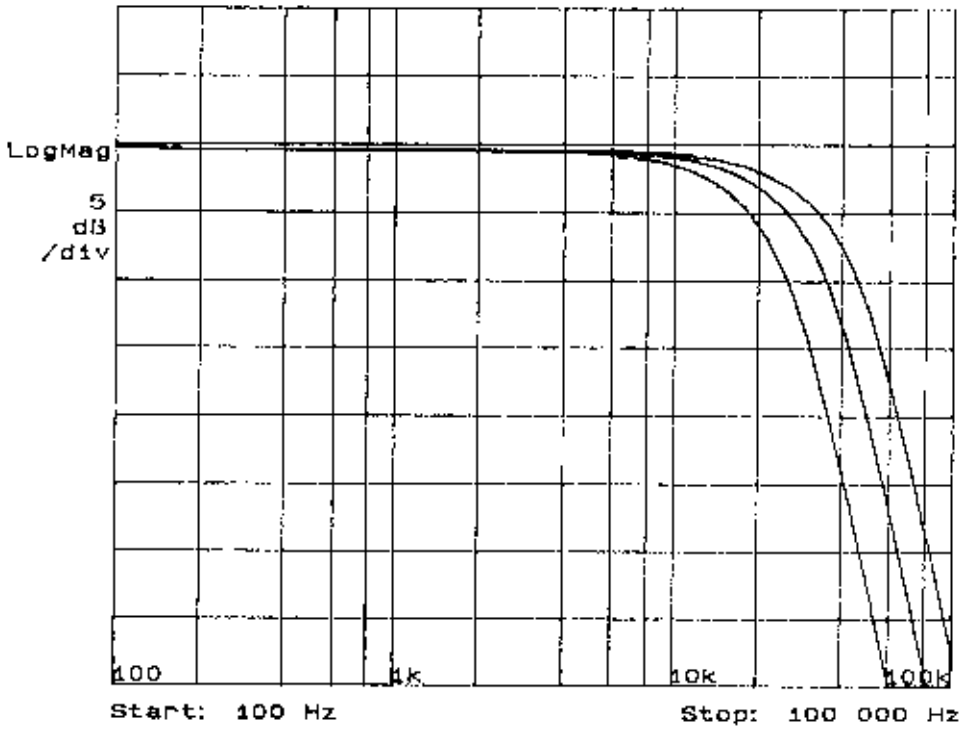


Figure 6.2 Measured Frequency Responses with Tuning

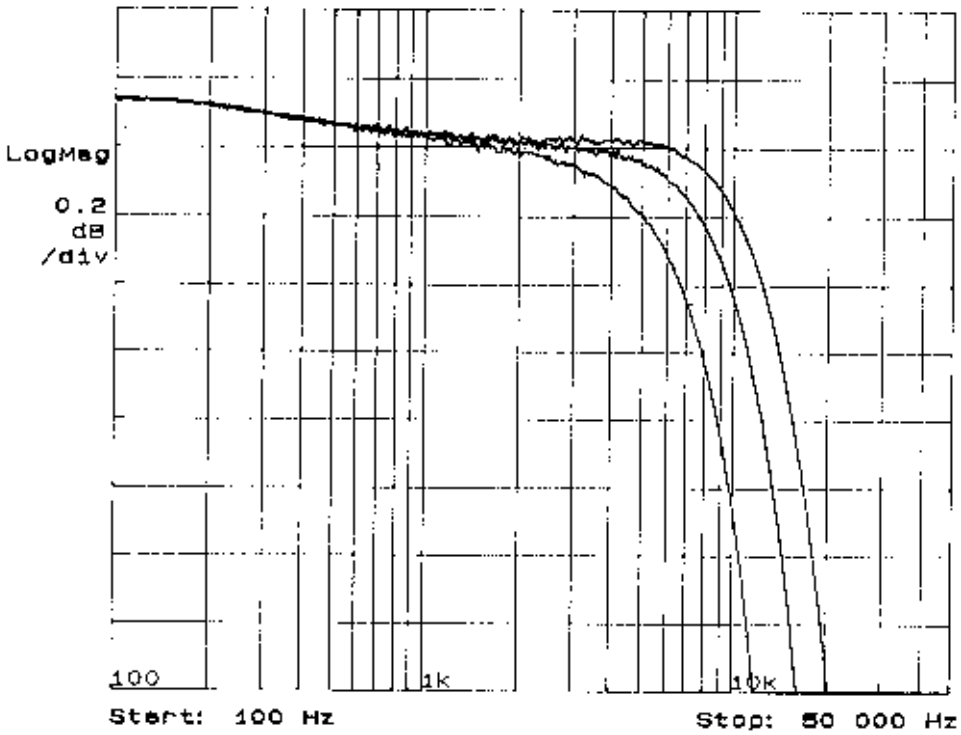


Figure 6.3 Pass-band Flatness

in Chapter 3). The control of the corner frequency can also be accommodated by changing the input reference clock, which is fixed at about 1 MHz in this test setup. Shown in Fig. 6.3 is the expanded pass band for flatness measurement, with the identical setting of the corner frequencies displayed in Fig. 6.2. As observed from the figure, the measured pass-band deviation is about 0.1 dB. The constant group delay of the Bessel filter can also be observed in Fig. 6.4. Again, the corner frequencies are the same but the plot is shown on a linear frequency scale. The group delay is sufficiently flat within the given pass-band for each frequency setting, displaying a variation limited to no more than 1μsec.

Shifting attention to the figures relating to linearity measurements, the output spectrum

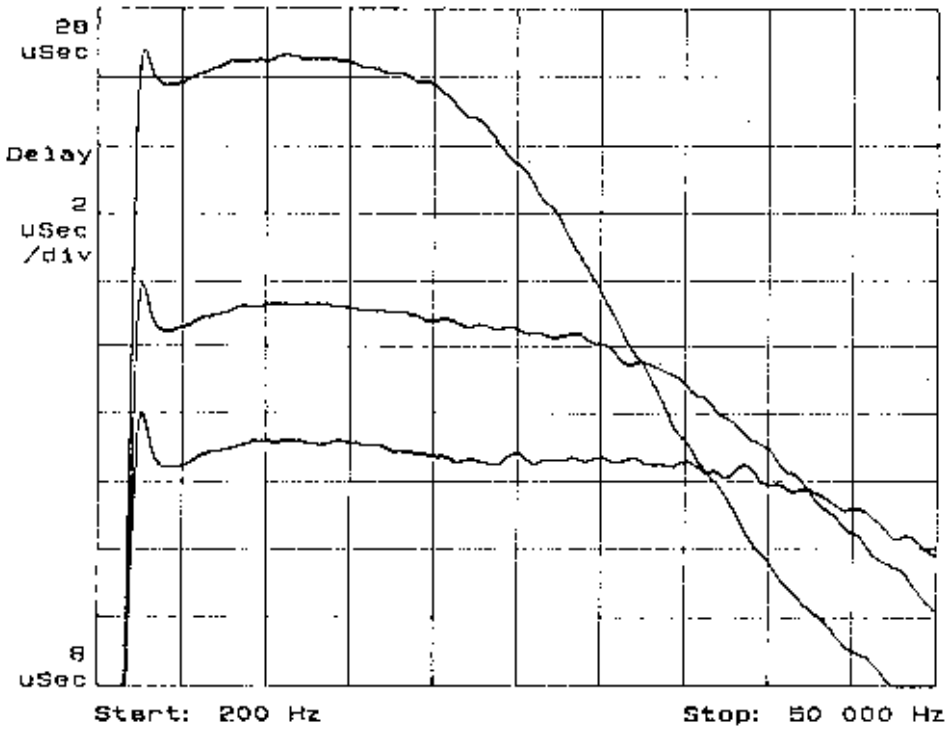


Figure 6.4 Measured Group Delay with Linear Frequency

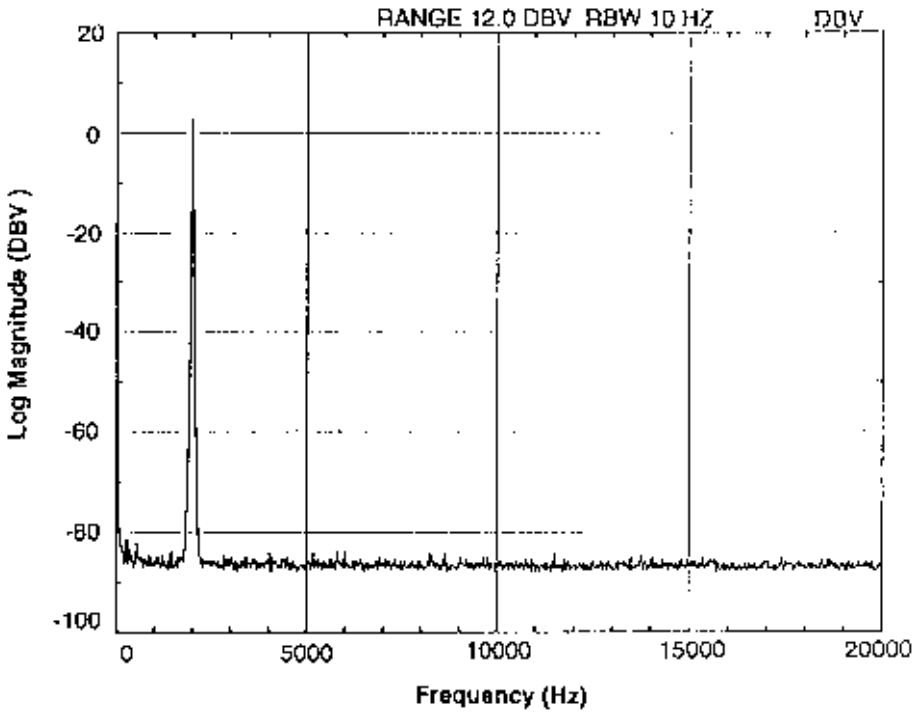


Figure 6.5 Measured Output Spectrum (2-kHz Tone)

in reference to a 2-kHz 4-V_{p-p} input is shown in Fig. 6.5. The output displays a very pure 2-kHz tone showing no distortion above -90 dB in reference to the input signal, bounded by the limited resolution of the spectrum analyzer at that level. Using a separate distortion analyzer, the measured THD versus input frequency is shown in Fig. 6.6. In the measurement taken for f_{-3dB}=22kHz (solid line), the plot verifies a close agreement with the simulation result of Fig. 2.25. The input signal is fixed at 4-V_{p-p} differential. As anticipated, this plot captures the effect of the feedback loop gain on distortion. Consider again the solid line representing the 22 kHz corner frequency setting. As the input frequency approaches the filter pass-band edge, the loop gain is reduced and the distortion increases. Also in this

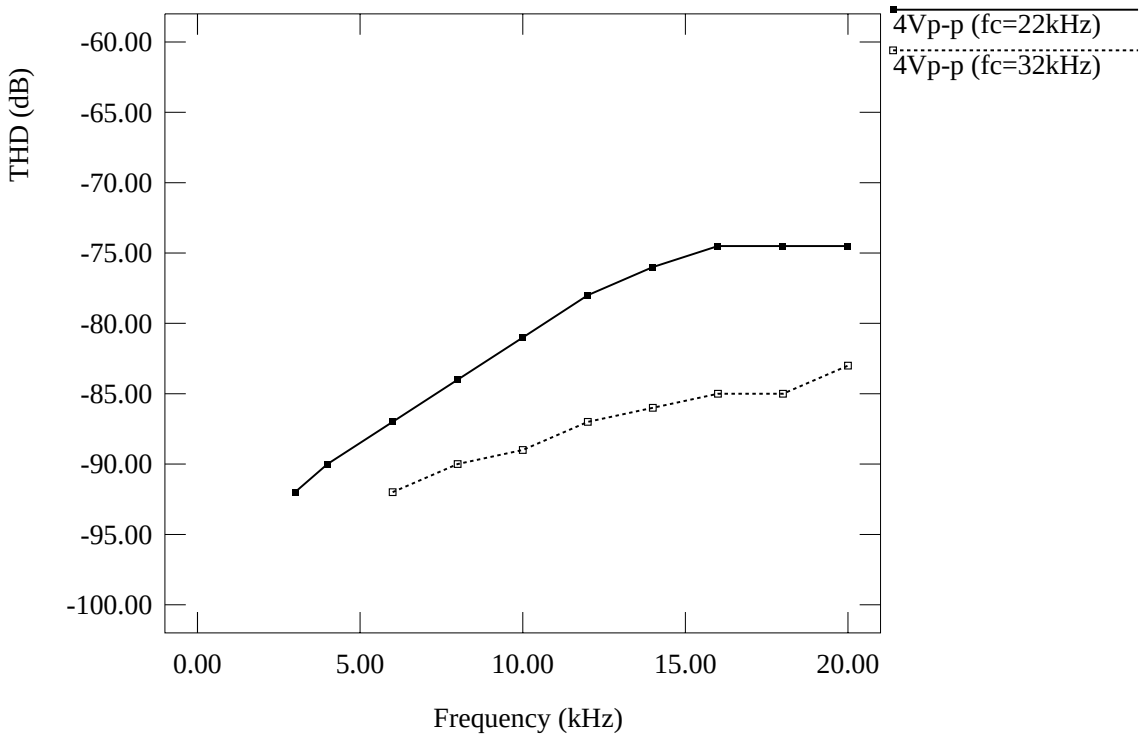


Figure 6.6 Measured THD vs. Frequency

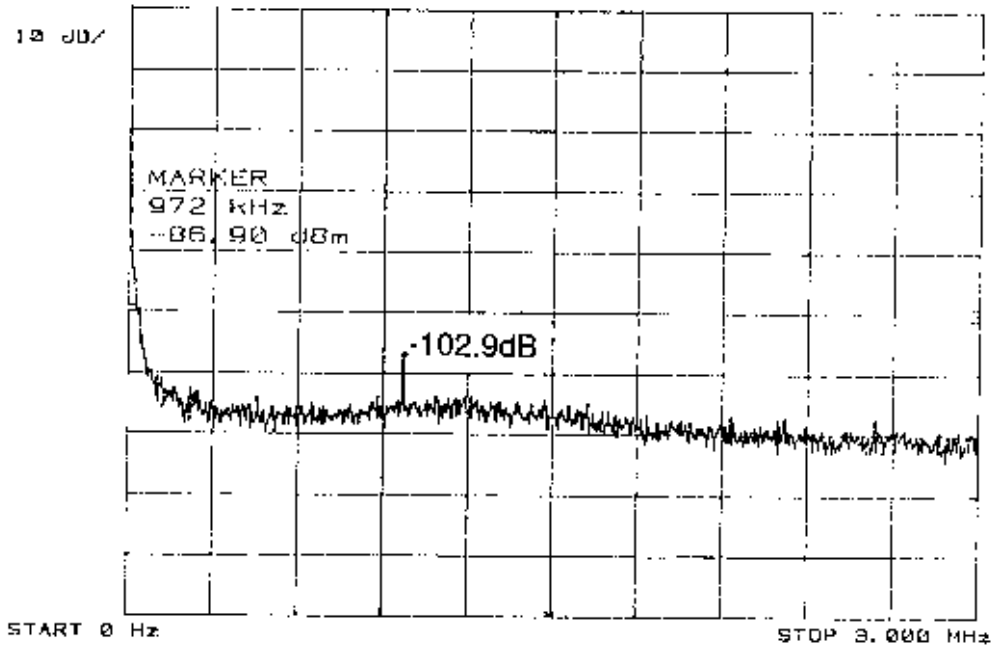


Figure 6.7 Measured Clock Feedthrough

figure, the two separate lines represent the two different control voltages set to place the f_{-3dB} at 22 kHz and 32 kHz. Even though the THD partially depends on the control voltage itself, THD improvement resulting from the widening of the filter bandwidth is also observed in this plot. This implies that for an oversampling digital-audio application, if f_{-3dB} can be allowed to be higher than the audio-band (22 kHz), an even greater linearity in the audio-band (frequencies of interest) is feasible.

Finally, while the clock feedthrough coming from the tuning loop is unseen at the output of the filter at the level of about 90 dB resolution, with an expanded frequency window and without the presence of the input signal, a measurement is made at below -100 dB (10 μV_{rms}) as shown in Fig. 6.7. Table 6.1 summarizes the measured performance of the

Table 6.1 Summary of Measured Performance

Technology	2μ double poly CMOS
Filter type	5th-order Bessel
Cutoff frequency	22kHz
Tunable range	2kHz - 35kHz
Pass band f_{-3dB} (std. dev.)	5%
Pass-band deviation	0.1dB
Group delay	$19 \pm 0.5\mu$sec
Control voltage feedthrough	10 μV_{rms}
THD ($4V_{p-p}$, 2kHz input)	-90dB
SNR	83dB
CMRR (flat across spectrum)	58dB
PSRR+ (worst at 10kHz)	58dB
PSRR- (worst at low freq)	47dB
Power supply	5V
Power consumption	40mW
Active die area	$7mm^2$

prototype filter.

CHAPTER 7

HIGH-FREQUENCY R-MOSFET-C FILTER CONSIDERATIONS

The architectural setting of the R-MOSFET-C filter has been shown to be an extended modification of the MOSFET-C filter [28], which is built on a framework nearly identical to that for the standard RC active filters. It is common knowledge that this kind of filter driving low-impedance loads requires low output impedance and high gain-bandwidth product operational amplifiers for high-frequency applications. For this reason, most high-frequency applications have chosen the Gm-C (or OTA-C) filter approach [22]-[25], [31]-[36]. Just as all modifications of standard RC filter techniques suffer from these drawbacks (the requirement for high-gain and low output impedance op amps), the R-MOSFET-C filters face the same set of obstacles.

7.1 Op Amp Bandwidth Limitation

The extra phase lag and phase lead due to the finite op amp gain bandwidth and dc gain, respectively, cause nonideal behavior in the integrator. These defects in the building blocks of active filters are considered in many references [22], [23], [31]-[33], [47], [48], [61], [62]. The discussions are often in the context of Gm stages, but the principle applies equally to the op amps in the active RC architecture. In summary, the nonideal behaviors are the peaking and drooping effects in the passband towards the -3 dB corner frequency

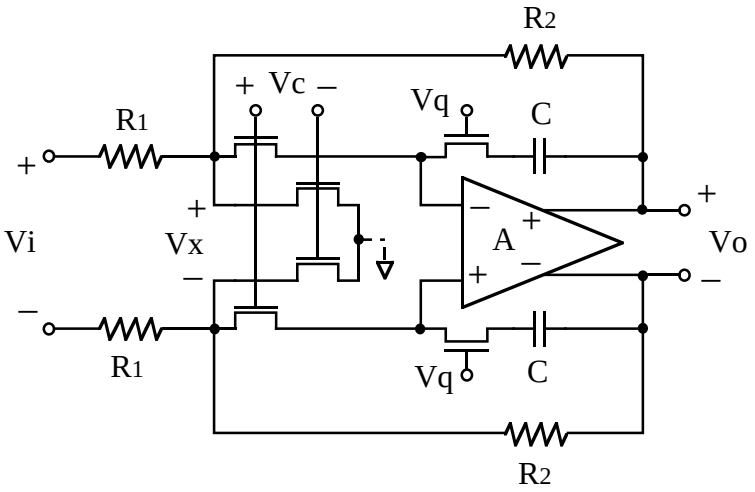


Figure 7.1 R-MOSFET-C with Additional Phase-lead Zero

due to phase lag and phase lead of the integrators, respectively. Also discussed in the same references are various techniques applied in order to compensate for these nonideal effects.

While the phase correction techniques discussed in the references vary in style from choosing optimal device sizes for the cancellation of leading and lagging phases between the dc gain (phase-lead) error and the finite gain-bandwidth (phase-lag) error [22], to introducing extra phase lead and lag Q-control circuitry [33], the common concept used among all is simply the placement of a zero that would cancel the phase-lagging portion. As high-frequency filter design pushes towards the upper limit of a given technology, the common phase-error problem is the phase lag due to the the nondominant poles of the integrator.

Among the techniques available for phase correction, perhaps the simplest and the most natural way to introduce the extra phase lead is to place a tunable resistor in series with the integrating capacitor [31]. This is shown in Fig. 7.1 in the context of an R-MOSFET-C first-order filter. The nonlinear components are inside the feedback loop and on the forward

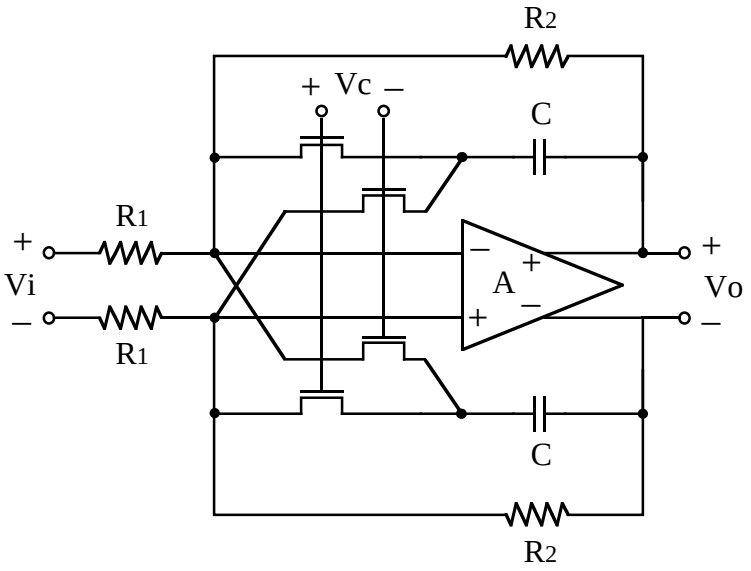


Figure 7.2 First-order R-MC Filter

path; thus, the reduction of distortion by the feedback loop gain is in place. The addition of a zero for phase lead as shown would require some sort of an automatic Q-control circuit similar to [33].

A small variation of the R-MOSFET-C structure can also introduce an additional zero for phase-lead compensation. The schematic shown in Fig. 7.2 has the the current steering element, the four current-steering MOSFETs in triode, lumped with the integrating capacitors instead. This arrangement in the context of digital trimming is described in [1], referred to in this setup as the R-MC integrator/filter. Just as there were design choices for the current-steering portion (criss-cross versus current-dumping) in the prototype R-MOSFET-C filter, this R-MC design may also use the current-dumping block in place of the criss-cross configuration as shown in the figure. This R-MC arrangement does not experience the multiple-input loading effect as in the standard R-MOSFET resistance stage

(discussed in Section 2.2.3), yet the noise increase due to the current-steering MOSFETs (Section 2.2.2) still has to be considered. For the Q-control of the filter, the common-mode portion of the control voltage, V_C, can be adjusted.

7.2 High-Frequency Limitation of MOSFETs in Triode

In addition to the phase lag resulting from the nonideal finite gain bandwidth of the operational amplifiers used in the filter, one must also consider the frequency limitations of the MOSFETs operating in triode. Modeling the MOSFET in triode as a distributed RC element (i.e., RC transmission line), an extensive analysis and application example of the MOSFET in triode have been reported [61], [62]. It was further shown in [61] that the MOSFETs that are arranged in the cross-coupled configuration (Fig. 2.2) experience an inherent cancellation of the high-frequency phase lag. But as the author points out, the theory is valid only within the bounds of modeling assumptions. If these derived results of [61] are applied directly to the R-MOSFET-C filter, the criss-cross configuration (Fig. 2.9) would be free from such high-frequency effects. This benefit does not extend to the current-dumping configuration (Fig. 2.11). The fact remains that MOSFETs in triode will suffer from some kind of extra phase lag.

A similar set of phase correction techniques as discussed in the previous section can be applied to make up for the extra phase lag from the MOSFETs in triode. The aggregate phase-lag effect from the finite gain bandwidth of the op amp and the distributed RC nature of the MOSFETs as a whole can be corrected by the Q-control.

7.3 Driving Low-Impedance Loads

As the requirement of the op amp gain bandwidth increases for the higher frequency filter design (approaching the limit of the technology available), naturally the op amps would require large currents in order to satisfy maximum gain bandwidth [32]. Because of the inherent low-impedance loads due to smaller RC time constants for a fixed dynamic range (i.e., fixed C), the commonly implemented output buffers (source followers) specifically in CMOS technology would have to become wider and run higher currents to make up for the loading. This kind of output buffer would further work against the gain-bandwidth and power consumption concerns. These issues are common to all op amp-based active filters, including the R-MOSFET-C filters. For this reason, the Gm-C (or OTA-C) type filters are preferred in general in the design of high-frequency filters, but the linearity performance is bound by the Gm (or OTA) portion that is made of inherently nonlinear components.

In the recent attempt to achieve high linearity by implementing a fixed-value highly linear Gm stage, in conjunction with a tunable Gilbert cell in the forward path inside a feedback loop, the linearity reported for the 8-MHz low-pass filter is -79dB THD for a 1-MHz 5 V_{p-p} differential input in a 10-V system [35]. The signal swing is limited for the given 10-V system and the technology used was a rather expensive 2.5-GHz BiCMOS process with thin-film resistors, but the topology is quite similar to that for the R-MOSFET-C technique in that current-steering elements (Gilbert cells) are used for tuning and placed inside feedback loops. The linearity limitation is expected to come from the fixed-value Gm stages.

CHAPTER 8

CONCLUSIONS

One of the key driving factors for the study and the invention of the R-MOSFET-C filter was the challenge of implementing a highly linear filter using a basic CMOS technology. Previous work, especially in CMOS, falls far short of the very demanding linearity performance required by some applications such as digital audio. The measured performance of the prototype R-MOSFET-C filter has demonstrated the feasibility of digital-audio filters in CMOS and further extends the low-distortion capabilities of continuous-time CMOS filters.

This thesis describes a method of building a highly linear tunable continuous-time filter, given the name R-MOSFET-C filter. The linearity improvement technique was shown to reduce the signal swing across the nonlinear tunable devices by the voltage scale factor, F, and the feedback loops, in an active filter configuration, which encircles the nonlinear current-steering MOSFETs, further reduces the THD by the amount of loop gain (details in Chapter 2). This R-MOSFET-C linearity improvement technique shows a great improvement in the THD measure at the cost of a slight increase in noise power. For the worst-case simulation, with a 2 kHz, 4 V_{p-p} differential input, the result yields a 50 dB improvement in THD over the conventional MOSFET-C filter with a 2 dB higher noise floor in a fifth-order Bessel filter example. The measured THD is better than -90 dB with a 2 kHz, 4 V_{p-p} differential input for the prototype 22 kHz Bessel filter.

An automatic tuning implementation, utilizing the time constant of a switched capacitor as the accurate reference, was shown to simplify the tuning circuitry greatly (Chapter 3). This automatic tuning implementation can be applied generally for any continuous-time versus discrete-time (switched-capacitor) comparison. The self-tuning block implemented in the prototype filter demonstrates a 5% standard deviation for the passband f_{-3dB} among the fabricated chips. A four-bit digital word for frequency control further accommodates fine tuning down to $\pm 1\%$ accuracy.

An iterative dynamic range optimization method via linear programming, given the fixed total capacitance constraint (approximation for the total silicon area), yields an incremental improvement (Chapter 4), which partly compensates for the minor degradation (details in Section 2.2.2) of the dynamic range resulting from the R-MOSFET-C linearity improvement technique. This dynamic range optimization approach can be applied in general to all active filter designs, and the details of the method may be broadened by building on the cost and constraint conditions.

As mentioned in Chapter 7, there are a few drawbacks to this R-MOSFET-C structure relating to high-frequency filter considerations and limitations, as they are common concerns to all op-amp-based active filters (e.g., active RC and MOSFET-C). As the demand for higher frequency and better linearity performance increases, and efforts continue to produce smaller and lower power ICs, it is desirable to develop new design techniques which produce high-linearity filters that do not have the drawbacks discussed in Chapter 7. The disadvantages are limited op amp gain-bandwidth, frequency limitation of MOSFETs in tri-

ode, and increased power consumption for wide-band op amps and low-impedance loads. One attempt [35] uses highly linear fixed-value Gm stages with the filter tuning controlled by current-steering Gilbert cells. Even though the authors do not point this out explicitly, the Gilbert cells reside in the forward paths inside feedback loops, thus experiencing reduction of distortion by the loop gain (neglecting the nonlinearity of the Gm stages). The achieved linearity is significant, yet the filter is still bound by the imperfect Gm stage and miscellaneous nonlinearities coming from the rest of the circuit.

The R-MOSFET-C linearity-improved filter design technique demonstrates promising linearity performance in the prototype filter, as anticipated in theory. The ambitious performance levels for a given technology (in this case CMOS) are more than feasible given the time for concentrated studies of the related material and experiment. The linearity performance of the CMOS technology is not saturated at -60 dB THD. There are many more ambitious and demanding standards not yet achieved for a given technology (such as low-power, high-linearity, and high-frequency filters); those standards may be reached by new and clever techniques.

REFERENCES

[1] S. Schmalz, "Digitally tunable continuous-time monolithic filters," M.S. thesis, University of Illinois at Urbana-Champaign, April 10, 1991.

[2] R.P. Sallen and E.L. Key, "A practical method of designing RC active filters," *IRE Trans. Circuit Theory*, vol. CT-17, no. 1, pp. 74-85, 1955.

[3] W.J. Kerwin, L.P. Huelsman and R.W. Newcomb, "State-variable synthesis for insensitive integrated circuit transfer functions," *IEEE J. Solid-State Circuits*, vol. SC-2, no. 3, pp. 87-92, 1967.

[4] R. Tarmy and M.S. Ghausi, "Very high-Q factor insensitive active RC networks," *IEEE Trans. Circuit Theory*, vol. 17, no. 3, pp. 358-366, 1970.

[5] G.S. Moschytz, "High-Q factor insensitive active RC network, similar to the Tarmy-Ghausi circuit but using single ended operational amplifiers," *Electron. Lett.*, vol. 8, no. 18, pp. 458-459, 1972.

[6] J.J. Friend C.A. Harris and D. Hilberman, "STAR: an active biquadratic filter section," *IEEE Trans. Circuits Syst.*, vol. CAS-22, no. 2, pp. 115-121, 1975.

[7] G.S. Moschytz, "A universal low-Q active-filter building block suitable for hybrid integrated circuit implementation," *IEEE Trans. Circuit Theory*, vol. CT-20, no. 1, pp. 37-47, 1973.

[8] G.S. Moschytz and W. Thelen, "The design of hybrid integrated filter building blocks," *IEEE J. Solid-State Circuits*, vol. SC-5, pp. 99-107, June 1970.

[9] B.A. Stenoi, "Practical realization of a gyrator circuit and RC–gyrator filters," *IEEE Trans. Circuit Theory*, vol. CT-12, no. 3, pp. 374-380, 1965.

[10] T.N. Rao and R.W. Newcomb, "Direct-coupled gyrator suitable for integrated circuits and time variation" *Electron. Lett.*, vol. 2, no. 7, pp. 250-251, 1966.

[11] A. Antoniou, "Realization of gyrator using operational amplifiers, and their use in RC active-network synthesis," *Proc. IEE*, vol. 116, no. 11, pp. 1838-1850, 1969.

[12] A. Antoniou and K.S. Naida, "Modeling of a gyrator circuit," *IEEE Trans. Circuit Theory*, vol. CT-20, pp. 533-540, Sept. 1973.

[13] H.J. Orchard and A.N. Wilson, Jr., "New active gyrator circuit," *Electron. Lett.*, vol. 10, no. 13, pp. 262-262, 1974.

[14] W.H. Holmes, W.E. Heinlein and S. Gruetzmann, "Sharp-cutoff low-pass filters using floating gyrators," *IEEE J. Solid-State Circuits*, vol. SC-4, pp. 38-50, 1969.

[15] L.T. Bruton, "Network transfer functions using the concept of frequency-dependent negative resistance," *IEEE Trans. Circuit Theory*, vol. CT-16, no. 3, pp. 406-408, 1969.

[16] L.T. Bruton, "Non-ideal performance of two-amplifier positive impedance converter," *IEEE Trans. Circuit Theory*, vol. CT-17, no. 4, pp. 541-549, 1970.

[17] L.T. Bruton and A.B. Haase, "Sensitivity of generalized immitance converter embedded ladder structures," *IEEE Trans. Circuits Syst.*, vol. CAS-21, no. 2, 1974.

[18] A. Antoniou, "Bandpass transformation and realization using frequency-dependent negative-resistance elements," *IEEE Trans. Circuit Theory*, vol. CT-18, no. 2, 1971.

[19] J.G. Linvill, "RC active filters," *Proc. IRE*, vol. 42, pp. 555-564, March 1954.

[20] T. Yangisawa, "RC active filters using current inversion type negative impedance converters," *IRE Trans. Circuit Theory*, vol. CT-4, pp. 140-144, Sept. 1957.

[21] A.I. Larky, "Negative impedance converters," *IRE Trans. Circuit Theory*, vol. CT-4, pp. 124-131, Sept. 1957.

[22] H. Khorramabadi and P.R. Gray, "High-frequency CMOS linear continuous-time filters," *IEEE J. Solid-State Circuits*, vol. SC-19, no. 6, Dec. 1984.

[23] C.S. Park and R. Schaumann, "A high-frequency CMOS linear transconductance element," *IEEE Trans. Circuits Syst.*, vol. CAS-33, pp. 1132-1133, Nov. 1986.

[24] A. Negungadi and T.R. Viswanathan, "Design of linear CMOS transconductance elements," *IEEE Trans. Circuits Syst.*, vol. CAS-31, pp. 891-894, Oct. 1984.

[25] F. Krummenacher and N. Joehl, "A 4-MHz CMOS continuous-time filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. 23, no. 3, pp. 750-758, June 1988.

[26] M. Banu and Y. Tsividis, "An elliptical continuous-time CMOS filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. SC-20, no. 6, pp. 1114-1121, Dec. 1985.

[27] A. Durham, W. Redman-White, and J. Hughes, "High-linearity continuous-time filter in 5-V VLSI CMOS," *IEEE J. Solid-State Circuits*, vol. SC-27, no. 9, pp. 1270-1276, Sept. 1992.

[28] Y. Tsividis, M. Banu, and J. Khoury, "Continuous-time MOSFET-C filters in VLSI," *IEEE J. Solid-State Circuits*, vol. SC-21, no. 1, pp. 15-29, Feb. 1986.

[29] J. van der Plas, "MOSFET-C filter with low excess noise and accurate automatic tuning," *IEEE J. Solid-State Circuits*, vol. 26, pp. 922-929, Jul. 1991.

[30] K. Lou, D. Hiser, W. Adams, and R. Geiger, "A versatile digitally controlled continuous-time filter structure with wide-range and fine resolution capability," *IEEE Trans. Circuits Syst.*, vol. 39, no. 5, pp. 265-276, May 1992.

[31] C. Laber and P. Gray, "A 20 MHz 6th order BiCMOS programmable filter using parasitic-insensitive integrators," *Dig. of Symp. VLSI Circuits*, pp. 104-105, 1992.

[32] John Khoury, "Design of a 15-MHz CMOS continuous-time filter with on-chip tuning," *IEEE J. Solid-State Circuits*, vol. 26, no. 12 pp. 1988-1997, Dec. 1991.

[33] V. Gopinathan, Y. Tsividis, K. Tan, and R. Hester, "Design consideration for high-frequency continuous-time filter and implementation of an antialiasing filter for digital video," *IEEE J. Solid-State Circuits*, vol. 25, no. 6 pp. 1368-1378, Dec. 1990.

[34] G. De Veirman and R. Yamasaki, "A 27MHz programmable bipolar 0.05^o equiripple linear phase filter," *ISSCC Dig. of Tech. Papers*, pp. 64-65, Feb. 1992.

[35] S. Willingham and K. Martin, "A BiCMOS low-distortion 8MHz lowpass filter," *ISSCC Dig. of Tech. Papers*, pp. 114-115, Feb. 1993.

[36] K. S. Tan and P. R. Gray, "Fully integrated analog filters using bipolar-JFET technology," *IEEE J. Solid-State Circuits*, vol. SC-13, no. 6, Dec. 1978.

[37] K. Bult and Hans Wallinger, "A class of analog CMOS circuits based on the square law characteristic of an MOS transistor in saturation," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 3, pp. 357-365, June 1987.

[38] E. Seevinck and R. F. Wassenman, "A versatile MOS linear transconductor/ square-law function circuit," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 3, pp. 366-377, June 1987.

[39] M. Banu and Y. Tsividis, "Fully integrated active RC filters in MOS technology," *IEEE J. Solid-State Circuits*, vol. SC-18, no. 6, pp. 644-651, Dec. 1983.

[40] M. Ismail, S. V. Smith, and R. G. Beale, "A new MOSFET-C universal filter structure for VLSI," *IEEE J. Solid-State Circuits*, vol. 23, no. 1, pp. 183-194, Feb. 1988.

[41] B.-S. Song, "CMOS RF circuits for QAM transceivers," *AT&T Bell Labs Tech. Memo*, #52214-84703-01 TM, July 3, 1984.

[42] Y. Tsividis, Z. Czarnul, and S.C. Fang, "MOS transconductors and integrators with high linearity," *Electron. Lett.*, vol. 22, no. 5, pp. 245-246, Feb. 1986.

[43] B.-S. Song, "CMOS RF circuits for data communications applications," *IEEE J. Solid-State Circuits*, vol. SC-21, no. 2, pp. 310-317, April 1986.

[44] Z. Czarnul, "Modification of Banu-Tsividis continuous-time integrator structure," *IEEE Trans. Circuits Syst.*, vol. CAS-33, no. 7, pp. 714-716, Jul. 1986.

[45] R. Castello and P.R. Gray, "A high-performance micropower switched-capacitor filter," *IEEE J. Solid-State Circuits*, vol. SC-20, no. 6, pp. 1122-1132, Dec. 1985.

[46] K. -L. Lee and R. Meyer, "Low-distortion switched-capacitor filter design techniques," *IEEE J. Solid-State Circuits*, vol. SC-20, no. 6, pp. 1103-1113, Dec. 1985.

[47] L.C. Thomas, "The biquad: Part I — Some practical design considerations," *IEEE Trans. Circuit Theory*, vol. CT-18, pp. 350-357, May 1971.

[48] A. Budak and D.M. Petrela, "Frequency limitations of active filters using operational amplifiers," *IEEE Trans. Circuits Syst.*, vol. 19, pp. 322-328, Jul. 1972.

[49] B.-S. Song, ECE497 Advanced Topics in Analog IC Design class notes, University of Illinois at Urbana-Champaign, Spring 1991.

[50] Y. Tsividis and Bingxue Shi, "Cancellation of distortion of any order in integrated active RC filters," *Electron. Lett.*, vol. 21, no. 4, pp. 132-134, 14 Feb. 1985.

[51] T.R. Viswanathan, S. Murtuza, V.H. Syed, J. Berry, and M. Staszel, "Switched-capacitor frequency control loop," *IEEE J. Solid-State Circuits*, vol. SC-17, no. 4, pp. 775-778, Aug. 1982.

[52] G. Groenewold, "A high-dynamic-range integrated continuous-time bandpass filter," *IEEE J. Solid-State Circuits*, vol. 27, no. 11, pp. 1614-1622, Nov. 1992.

[53] A.B. Williams and F.J. Taylor, *Electronic Filter Design Handbook*, 2nd ed. New York: McGraw Hill, 1988.

[54] A.I. Zverev, *Handbook of Filter Synthesis*. New York: Wiley, 1967.

[55] R.S. Schaumann, M.S. Ghausi, and K.R. Laker, *Design of Analog Filters*. New Jersey: Prentice Hall, 1990.

[56] R. Gregorian and G. Temes, *Analog MOS Integrated Circuits for Signal Processing*. New York: John Wiley & Sons, 1986.

[57] D.J. Perry, "Scaling transformation of multiple feedback filters," *Proc. IEE*, vol. 128, pt. G, pp. 176-179, 1981.

[58] Gilbert Strang, *Linear Algebra and Its Applications*, 3rd ed. San Diego: HBJ, 1988.

[59] F. E. J. Girling and E. F. Good, "The leapfrog or active-ladder synthesis," *Wireless World*, vol. 76, pp. 341-345, 1970.

[60] H.J. Orchard, "Inductorless filters," *Electron. Lett.*, vol. 2, pp. 224-225, June 1966.

[61] J. Khoury and Y. Tsividis, "Analysis and compensation of high-frequency effects in integrated MOSFET-C continuous-time filters," *IEEE Trans. Circuits Syst.*, vol. CAS-34, no. 8, pp. 862-875, Aug. 1987.

[62] B.-X. Shi, J. Khoury, and Y. Tsividis, “High frequency effects in MOSFET-C Tow-Thomas biquads,” *IEEE Trans. Circuits Syst.*, vol. CAS-33, no. 7, pp. 648-651, June 1986.

VITA

Un-Ku Moon is a naturalized U.S. citizen, born in Seoul, Korea, on July 4, 1964. He received the B.S. degree from University of Washington, Seattle, in December 1987, and the M.E. degree from Cornell University, Ithaca, New York, in May 1989. From February 1988 to August 1989, he was a Member of Technical Staff at AT&T Bell Laboratories in Reading, Pennsylvania, and from August 1989 to January 1991, he was a graduate student at Cornell University. While pursuing the Ph.D. degree at the University of Illinois, Urbana-Champaign, he has taught a junior-level microelectronics course from August 1992 to December 1993. His research has been in the area of analog and mixed analog-digital intergrated circuits, focusing on highly linear and tunable continous-time filters.