Low Voltage High-SNR Pipeline Data Converters

Charles Myers, Jipeng Li, Dong-Young Chang, and Un-Ku Moon
School of EECS, Oregon State University, Corvallis, OR 97331
Email: myersch@eecs.oregonstate.edu

***Abstract*— A design strategy is presented for obtaining high-SNR (14 bits or higher) in a low voltage pipeline data converter. This is accomplished with the removal of the S/H input stage and the use of a rail-to-rail input stage. The rail-to-rail input requires a reference calibration scheme to maintain converter linearity, and is implemented as a radix calibration.**

I. Introduction

Improving the signal-to-noise ratio (SNR) of any data converter design must be accomplished through two basic means, either by decreasing the noise power generated within the data converter (generally the first few stages) or by increasing the signal power. In many cases the only available option is the former due to circuit-level signal swing limitations.

In pipeline data converters, noise reduction options such as oversampling and noise shaping are not available and focus must instead be placed on deciding how much power and area can be spent to achieve low noise. For most pipeline applications, this makes higher SNR levels unattainable, especially at low supply voltages.

Any further improvement in SNR must come from an increase in signal power. The signal swing in pipeline stages is traditionally limited to the voltage reference level, but for the input stage this need not be the case. The signal swing is, however, fundamentally limited by the power supply voltage, which many modern processes require to be quite small. The high-SNR design techniques discussed in this paper will allow low-voltage designs to compete with SNR values of todays higher-voltage data converter designs.

In this paper, *rail-to-rail input* will be discussed as a viable option for improving SNR in high-resolution pipeline data converter designs. Implementation of rail-to-rail input on the circuit level will also be covered as well as a calibration method for correcting reference mismatches. The organization will be as follows: First, two methods for improving SNR efficiently will be discussed, then the simultaneous circuit implementation of these ideas will be explored, and finally a calibration method will be presented to correct errors generated by the system implementation.

II. Achieving High-SNR

Current pipeline data converter designs are almost exclusively implemented as switched-capacitor circuits, and as such are subject to kT/C noise resulting from RC-filtered and sampled thermal noise. It can be shown that a one-bit (6dB) improvement in kT/C noise level requires an increase in input sampling capacitance of four times. This fundamental relationship between noise and capacitance severely limits noise levels that can be achieved economically.

In a pipeline data converter, the residue amplification between stages reduces the proportional noise contributions of following stages to the overall data converter noise. As a result, the first stages in the pipeline are the most crucial for determining the overall noise level of the converter. This paper will therefore focus on the first pipeline stage, as it will largely determine the overall accuracy, speed, power consumption and die area of the data converter.

A. Removal of S/H

The function of the sample-and-hold (S/H) circuit is to provide a clean and settled analog value for the input of the first stage. This allows the comparator to finish sampling the input signal and latch regenerate the comparison result before the MDAC requires the value for the amplification phase. The S/H does not provide any gain, and therefore does not suppress the noise generated by the first stage of the pipeline. The S/H and first stage will therefore generate the same proportional amount of input-referred noise. This is very undesirable for high-SNR designs.

If the S/H is removed the noise power generated before the second stage will be cut in half, or alternatively, the first stage capacitance can be halved to maintain the same noise level. Remaining stage capacitance requirements need not change.

The removal of the S/H will create some problems. These are discussed in a paper by Mehr and Singer [1] and include sampling mismatch between the MDAC and comparator paths and reduced speed due to extra time required for the comparator latch to regenerate. Further discussion about these issues will follow in section 3: Circuit Implementation.

B. Rail-to-Rail Input

Further improvement in the converter's SNR can be realized if the signal power is increased. It is initially assumed that the signal swing is set to the reference voltage level; therefore, the input swing must be extended beyond the reference to increase the input signal power. The furthest that the signal can be extended without creating reliability issues within devices is to the power rails. While this input can be accommodated with a switched-capacitor circuit, the MDAC opamp would not be able to drive this signal without large nonlinearities.

The solution to this problem is to reduce the output voltage swing of the first stage by a factor of two compared to the input voltage swing. This can be accomplished by simply doubling the feedback capacitance of the MDAC during the

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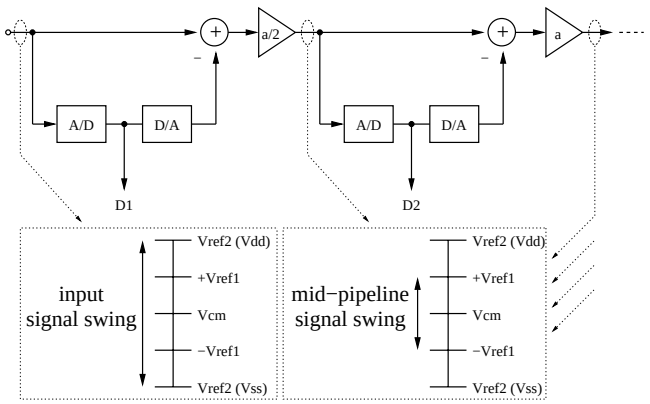

Fig. 1. Rail-to-Rail Input.

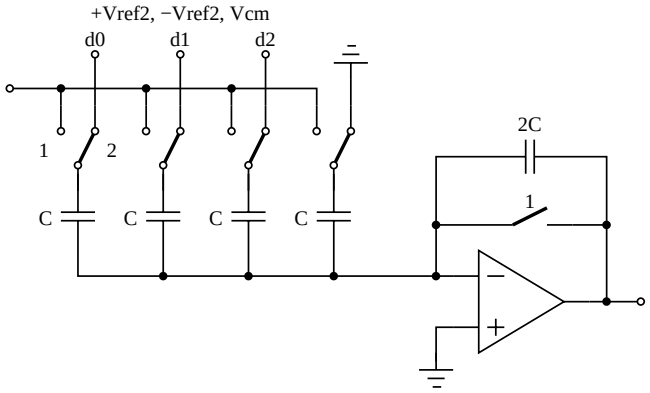

Fig. 2. Standard MDAC (with extra feedback cap).

amplification phase. The MDAC opamp should be able to easily drive this signal swing. It then follows that the rest of the pipeline should have input and output signal swings equal to 1/2 the power supply (Fig. 1). While this increases the input-referred noise power contributions of following stages by 4 times, the amount of capacitance area saved in the first stage is much larger than the required additional capacitance on remaining stages that make up for the lost noise attenuation.

III. Circuit Implementation

There are several ways in which the rail-to-rail input MDAC can be implemented. The most obvious solution is to use a standard MDAC structure, with twice as large feedback capacitors, and change the reference voltages applied to the subtraction capacitors from Vref1 to Vref2 (Fig. 2). While this solution is simple to implement, it does require that some calibration scheme be developed to correct inaccuracies in the charge subtraction due to Vref1 to Vref2 mismatch.

Another solution would be to create separate charge subtraction capacitors (as opposed to the shared input and subtraction capacitors of the standard MDAC structure) with a value twice as large as the input sampling capacitors (Fig. 3). This would allow the signal Vref1 to be used as the subtraction reference voltage and no calibration would be required. While the removal of a calibration requirement is desirable, the extra

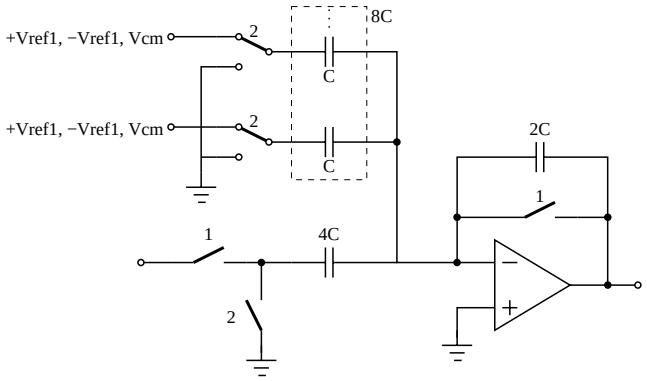

Fig. 3. Separate Reference Capacitor MDAC.

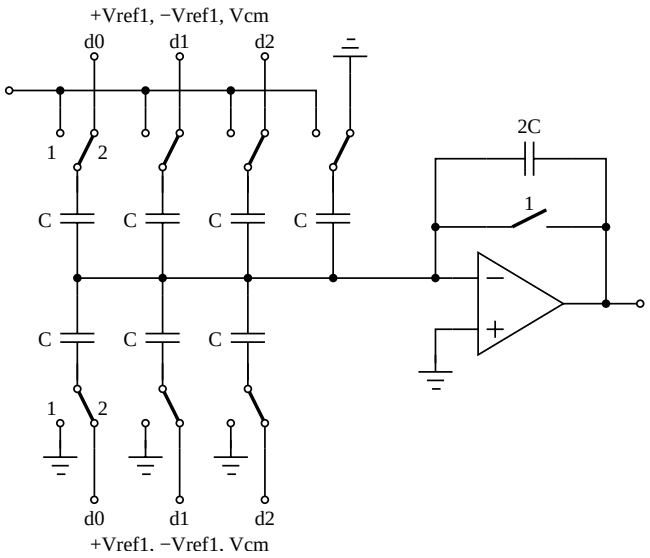

Fig. 4. 1/2 Separate Reference Capacitor MDAC.

charge noise injected by these subtraction capacitors is three times worse than the previous twice-reference solution. The feedback factor is also degrated by roughly the same amount.

One more solution, a compromise between the previous two solutions, is to keep the standard MDAC structure intact and to add one extra set of subtraction capacitors during the amplification phase (Fig. 4). This MDAC structure would also alleviate the calibration requirement, but would still have twice the amount of noise and nearly twice as worse a feedback factor as in the standard MDAC with a Vref2 reference voltage. Given the high-SNR goal discussed, required calibration is a small price to pay for the total savings in power, speed and area.

Not only must the MDAC be adjusted to operate correctly with a rail-to-rail input, but the structure of the entire 1st stage must be redesigned because of the removal of the sample-and-hold circuit. A good redesign would incorporate time-constant matching of input paths to ensure matched sampling between the comparator input and the MDAC input at high input frequencies, and a phase timing that schedules regeneration time for the comparator and latch. This was done in [2] and is

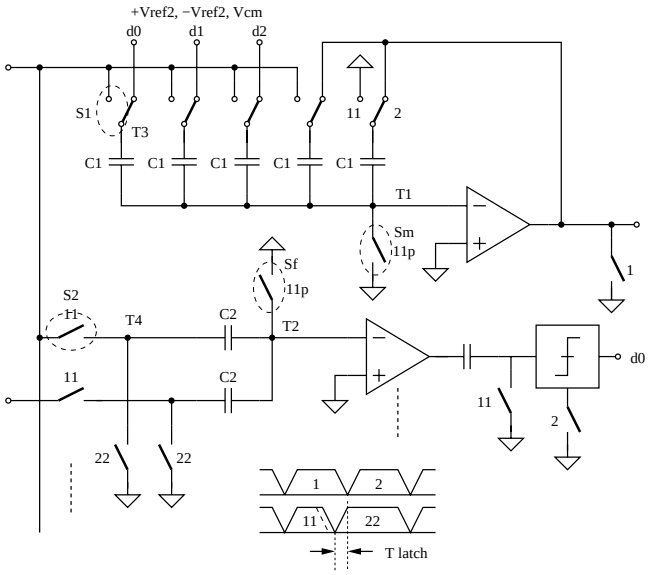

Fig. 5. NO S/H Circuit Implementation.

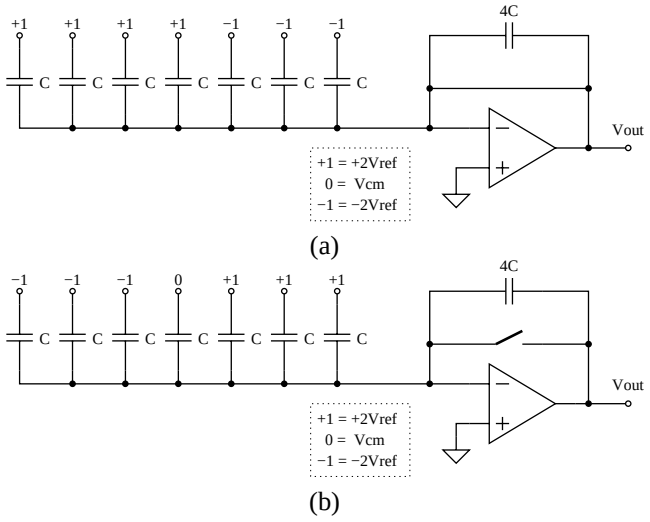

Fig. 6. Reference error extraction.

adapted for the special condition of the rail-to-rail input stage.

There are three operations that need to occur one after the other in the redesign of the first stage: sample, compare/latch, amplify. A straightforward solution would be to make three clock phases to schedule these operations, but would imply a 33% performance loss. Instead of evenly splitting the time between the three functions, phase 1 is divided between sampling and compare/latch functions leaving the amplification time untouched. The proposed 1st stage circuit structure and timing is presented in Fig. 5. The circled switches, S1, S2, Sf, and Sm must be carefully designed to match time-constants between the two input paths.

If additional tolerance to comparator offset is needed for a design in question, it can be generated by extending the allowable input range of the second stage by 1 LSB (LSB of that stage) with a simple structural change to the second stage [2]. By adding two additional comparators and a simple subtract-by-one logic, the offset tolerance can be extended – even resolving non-monotonic stage comparator levels without non-monotonic codes in the final output.

IV. Reference Calibration

In order to match the reference voltage used in first stage to the reference used in remaining stages, a calibration method must be adopted. The most applicable method would be a radix-based calibration [3]. While reference mismatch is not a classic gain error like that caused by feedback capacitor mismatch, it can still be modeled as such. The ideal radix value is given by 2^{m-1}, where m is the bits resolved in the current stage.

The measurement of the gain error created by the reference mismatch can be done either directly from the reference values with an on-chip delta-sigma converter [4], or indirectly through the 1st stage MDAC and measured with the remaining bits in the pipeline. While the second method is limited by the resolution of the remaining bits, it requires a minimum of additional circuitry and the error value can be readily extracted using similar means as is done for code-error calibration [5]. Averaging of multiple measurements (using all possible capacitor combinations) can increase the accuracy of the reference error measurement – reducing the the effects of noise and capacitor mismatch on the measurement.

A circuit method for extracting these mismatches from the MDAC is shown in Fig. 6. It can be proven that any one-bit increase from (a) to (b) will produce a resulting voltage on the output equal to (1/4)*Vref2 (assuming an input range between +Vref2 and -Vref2). This is equivalent to β*(1/2)*Vref1, where β is the reference mismatch error. The reference mismatch can be extracted from the measurement as follows,

$$\beta = \frac{V_{REF2}}{2V_{REF1}} = \frac{1/4V_{REF2}}{1/2V_{REF1}} = \frac{D_{HR} * V_{REF1}}{1/2V_{REF1}} = 2 * D_{HR}$$

where D_{HR} is the digitally measured *half-reference*. It can be seen by this equation that a bit-shift is the only digital operation that needs to be performed to extract β.

The radix calibration itself must be performed by a fixed-point multiplier so that slight variations in radix value can be accommodated [3]. A system that incorporates a microprocessor with this function can process a correction code for each first stage code that will be stored in a small on-chip memory. This correction code will then be referenced by the first stage code and added to the overall pipeline output to generate a calibrated output code. Implemented as such, the data converter can operate in normal mode without tying up microprocessor resources.

Since the error measurement is is done with a code-error type measurement, it is also possible to extract offset errors generated by the capacitor mismatch. These errors can then be added to the reference calibration code generated for each first

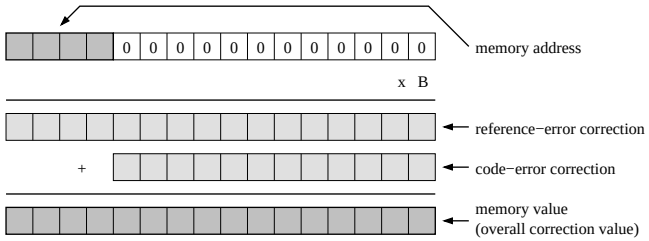

Fig. 7. Error code generation.

stage digital code. As such, both errors can be corrected at the same time by adding the calculated code-error and reference-error correction value (Fig. 7).

V. Conclusion

A design methodology for achieving high-SNR in pipeline data converters has been presented. This includes the use of a rail-to-rail input stage without input sample-and-hold circuitry and the development of a reference calibration scheme. The calibration scheme requires a foreground calibration phase, but can then run in the background once the calibration process is complete. This calibration can also simultaneously remove capacitor mismatch errors by incorporating code-error correction into the final correction value.

The removal of the sample-and-hold stage will create potential sampling mismatches between the first stage MDAC and comparator and will decrease the amount of time allowed for input sampling and comparator and latch regeneration. However, by incorporating the S/H removal and a rail-to-rail input, low voltage, high-SNR designs are economically attainable.

Acknowledgement

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