A 0.9V 9mW 1MSPS DIGITALLY CALIBRATED ADC WITH 75dB SFDR

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Abstract

A low-voltage two-stage algorithmic ADC incorporating the Opamp-Reset Switching Technique (ORST) is presented. The low-voltage digital CMOS process compatible operation is achieved without the clock boosting/bootstrapping or switched-opamp. The ADC employs a highly linear input sampling circuit at the front-end, and the digital output is calibrated using a radix-based scheme. The prototype was fabricated in a 0.18-μm CMOS technology and the active die area is 1.2mm $\times$ 1.2mm. The calibrated ADC demonstrates 75dB SFDR at 0.9V and 80dB SFDR at 1.2V. The total power consumption of the ADC is 9mW at the clock frequency of 7MHz (1MSPS).

Keywords: Low-voltage, opamp-reset switching technique, pipeline ADC, input sampling circuit, radix-based digital calibration.

INTRODUCTION

The state-of-the-art digital CMOS process is making the power supply transition to 1-V and below. This directly brings our attention to the emerging analog IC design challenges. Specifically, the shrinking/thinning gate oxide is prone to voltage stress and breakdown. While it is highly desirable that all analog circuits would adapt to the downscaling supply voltage, the switched-capacitor circuits, used in many practical signal processing applications, face a fundamental limitation in the operation of the floating switch under very low supply voltage. There are a several well-known techniques that seek to bypass this problem. However, the clock boosting/bootstrapping methods have the added loading and reliability issues, and the switched-opamp (SO) technique has the clock speed limitation. This paper summarizes an ADC implementation that incorporates the Opamp-Reset Switching Technique (ORST), where higher speed operation is achieved while maintaining all voltage levels within the power supply rails [1].

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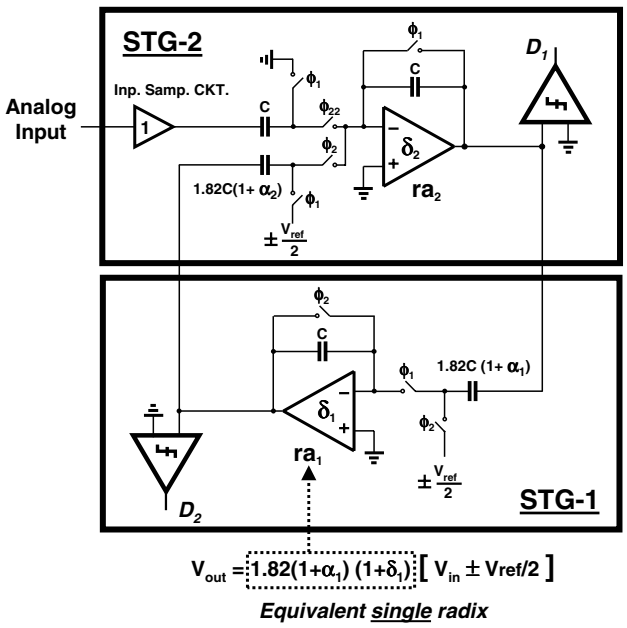

Figure 1: Block diagram of the low-voltage two-stage algorithmic ADC.

LOW-VOLTAGE ADC ARCHITECTURE

In the ADC design, the overall linearity is routinely limited by the matching characteristics of the analog building blocks. The digital calibration has been recognized as one of the effective solutions to correct for this unavoidable component mismatch. In this work, a radix-based digital calibration technique is applied to a two-stage algorithmic ADC (1-bit-per-stage). The block diagram of the ADC is shown in Figure 1. The ADC is composed of a front-end input sampling circuit and two cascaded stages that perform cyclic conversion. The nominal residue gain of the two multiplying DAC (MDAC) stages (STG-1 and STG-2) is 1.82 in order to allow for digital redundancy that relaxes the offset requirements [2]. The opamp and the comparator in each stage also employ offset cancellation technique to minimize

the overall offset. Any remaining offset can be suppressed by the digital redundancy. The interstage gain of 1.82 also implies that the ADC output can only be reconstructed by radix-1.82 calculation. Primarily due to the capacitor mismatch (α) and the opamp finite dc gain (δ), the ADC output is not linear. For a special case, as in the single-stage algorithmic ADC, there are no V_{ref} mismatches between stages and all error terms can be interpreted as a single interstage gain error [3]. As long as we measure that error, the ADC output can be digitally calibrated with a simple radix calculation. However, in the case of the multi-stage ADC, the error terms are unique for the interstage gains and the V_{ref} mismatches between stages. The ADC output is no longer easily calibrated with a simple radix calculation [4].

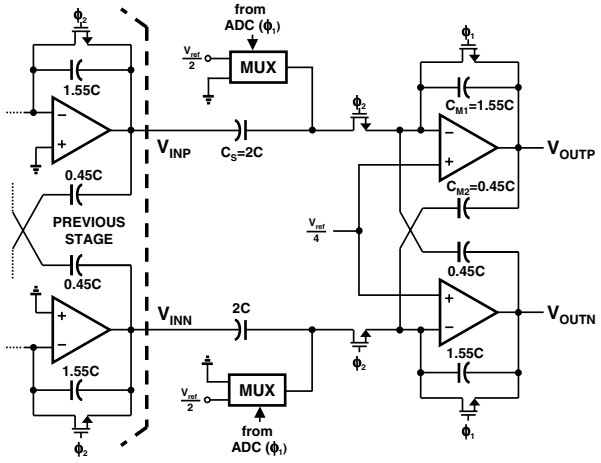

Figure 2: Simplified schematic of the low-voltage MDAC.

RADIX-BASED MULTI-STAGE ADC CALIBRATION

As shown in Figure 1, the sampling capacitors sample both input and $V_{ref}/2$ (instead of V_{ref}) in the same clock phase. A look-ahead scheme is used to pre-determine the polarity. In this way, the two signal paths (for input and reference) see the same set of error terms (α and δ) at the same time. Consequently, the residue voltage contains only one equivalent error term that represents the radix number for each stage (ra_1 and ra_2). The ADC output can now be digitally calibrated:

$$\begin{aligned} D_{out} &= \underbrace{D_{12}}_{LSB} + D_{11}\cdot(ra_1) + D_{10}\cdot(ra_1)(ra_2) \\ &\quad + D_9\cdot(ra_1)^2(ra_2) + D_8\cdot(ra_1)^2(ra_2)^2 \\ &\quad \cdots + \underbrace{D_1}_{MSB}\cdot(ra_1)^6(ra_2)^5 \end{aligned} \quad (1)$$

One important thing to be considered in this ADC structure is the operation timing. In conventional pipelined ADCs, the comparator's bit-decision is made a half clock period later than the input signal sampling. This implies that the input and $\pm V_{ref}/2$ cannot be sampled during the same clock phase. Therefore, the low-voltage structure requires a bit-lookahead configuration to move the comparator decision a half clock ahead. Instead of comparators deciding polarity of the present stage input, they look ahead to the next stage's signal polarity by shifting the reference point of the comparator by + and - $V_{ref}/2$ [5]. This will result in two digital output in each stage. The valid data between the two is selected by the previous stage's digital output. This scheme is omitted in Figure 1 for simplicity.

In this radix-based calibration, the overall linearity is determined by the measurement accuracy of the radix numbers ra_1 and ra_2. The primary difficulty is that the exact radix for each stage cannot be known in advance. The measurement procedure starts by forcing digital bits of "1" and "0" in turn at the MSB stage with fixed zero analog input. Since the digital outputs are inherently corrected by the digital redundancy (by making interstage gain of less than two), the two different MSBs will only change the residue signal path. Therefore, the nominal difference between the two outputs has to be zero when they are quantized by (1). With this desired value of zero, the estimated radix numbers can now be corrected by an incremental update algorithm:

$$ra_i[n+1] = ra_i[n] - \Delta\cdot\varepsilon_i[n] \quad (2)$$

A mathematical iteration index n and an update weighting factor Δ are used. Here ε_i is the mismatch between the two quantized output. During one radix update calculation, the other one is fixed to the previous estimate and vice versa until they converge to the two final values.

MDAC

The simplified schematic of the low-voltage MDAC is depicted in Figure 2. It employs the ORST in the pseudo-differential configuration. Because the circuit must operate within the given low supply voltage, all switches need to be driven to either maximum (V_{DD}) or minimum (GND) voltage potential. With a differential signal range of 0.9V peak-to-peak differential, $V_{ref}/2$ equals 0.225V, which is low enough to turn on the NMOS transistors at 0.9V clock swing. All floating switches are eliminated and the output of the opamps are connected directly to the sampling capacitor of the following MDAC stage. The fundamental operation of the ORST relies on fast and accurate resetting of the opamp in the unity-gain feedback configuration. Unlike the SO technique, opamps are always in the active mode of high-speed operation. To avoid the common-mode error accumulation problem that would result in a cascade of

pseudo-differential gain stages, a set of cross-coupled feedback capacitors are added. The small amount of differential positive feedback created from the cross coupling allows the differential gain of $C_S/(C_{M1} - C_{M2}) = 1.82$ while the common-mode gain of $C_S/(C_{M1} + C_{M2}) = 1$ is maintained. The common-mode level from the input is retained throughout the pipelining stages without requiring additional common-mode feedback circuitry. The opamp offset cancellation circuitry is excluded in Figure 2 for brevity, as well as the feedback factor modification (during unity-gain reset) which aids in keeping a steady opamp stability during both clock phases.

INPUT SAMPLING CIRCUIT

In order for the overall low-voltage ADC to be linear, a fast and sufficiently accurate input sampling circuit that is able to sample and transfer the external signal source into the IC is required. The circuit shown in Figure 3 provides the linear input signal tracking as well as the accurate reset signal to the first stage MDAC [6]. The inverting unity gain of the tracking signal is obtained from a one-to-one resistor ratio. All floating switches have been eliminated. During the tracking phase (ϕ_1), the intermediate virtual ground V_{xp} (V_{xn}) becomes $V_{DD}/2$. Assuming that the input common-mode voltage is $V_{DD}/2$, the output common-mode voltage also becomes $V_{DD}/2$. However, the voltage division between linear R and the on-resistance of MPP (MPN) during the reset phase (ϕ_2) introduces signal-dependent voltage fluctuation at V_{xp} (V_{xn}), which results in harmonic distortion during the tracking phase (ϕ_1). The precharged capacitors C_C connected between V_{xp} (V_{xn}) and the gate of MPP (MPN) cancel this distortion. This makes the resistance of MPP (MPN) constant. In addition, the nodes V_{xp} and X_1 (V_{xn} and Y_1) are sampled to the top plates of reference capacitors (C_1 and C_2) during the reset phase (ϕ_2) to cancel the remaining errors. Finally, a differential switch MPC is connected between the two pseudo-differential signal path further improves linearity and suppresses even order harmonics.

MEASURED RESULTS

The prototype ADC was fabricated in a 0.18-μm CMOS technology and occupies 1.2mm $\times$ 1.2mm of active die area. The micrograph of the prototype IC is shown in Figure 4. All measurement results were obtained at 0.9V single power supply. During the calibration mode, once two ε_i measurements are obtained, the mathematical iteration starts from the nominal radix value of 1.82 and converges to the correct numbers as shown in Figure 5. The FFT plots of Figure 6 illustrate the linearity improvement after the calibration for a 50kHz full-scale sinusoidal input sampled at 1MSPS (7MHz clock). After calibration, SNDR and SFDR improve from 40dB to 55dB and from 47dB to 75dB, respectively. Figure 7 shows the dynamic measurement results with different V_{DD} levels at the same dc bias current, demonstrating up to 80dB SFDR. In the measurement setup for Figure 7, the peak-to-peak differential input range was set equal to V_{DD}. The total power consumption of the prototype at 0.9V supply is 9mW. Performance of the ADC is summarized in Table 1.

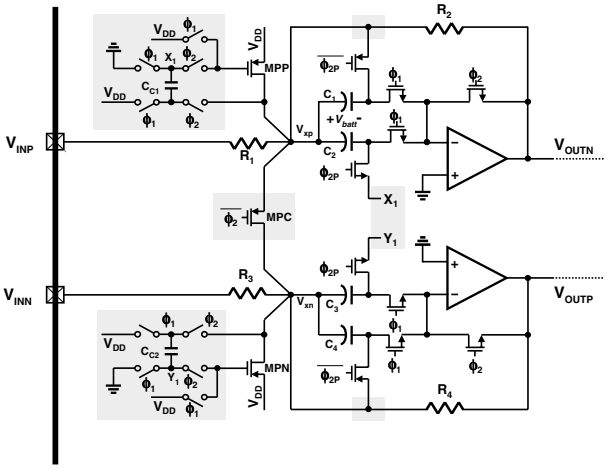

Figure 3: Input sampling circuit.

CONCLUSIONS

The design of a 0.9V 1MSPS (with internal clock of 7MHz) two-stage algorithmic ADC is described. For low-voltage operation, the ORST and pseudo-differential architecture are used. A highly linear input sampling circuit is also designed at the front-end. To overcome nonlinear effects, a radix-based digital calibration technique is proposed. Fabricated in a 0.18-μm CMOS process, an experimental IC dissipates 9mW at 0.9V supply. It has a differential input range of 0.9V peak-to-peak.

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Technology	0.18-μm CMOS
Resolution	10.4 binary bits (12 bits of 1.82 radix)
Chip size	1.2mm $\times$ 1.2mm
Supply voltage	0.9 V
Conversion rate	1 MSPS (clock=7 MHz)
Power consumption	9 mW (at 0.9V)
DNL	1.4 LSB / 0.8 LSB (cal.)
INL	6.3 LSB / 1.05 (cal.) LSB
SNDR	40 dB / 55 dB (cal.)
SFDR	47 dB / 75 dB (cal.)

Table 1: Measurement summary.

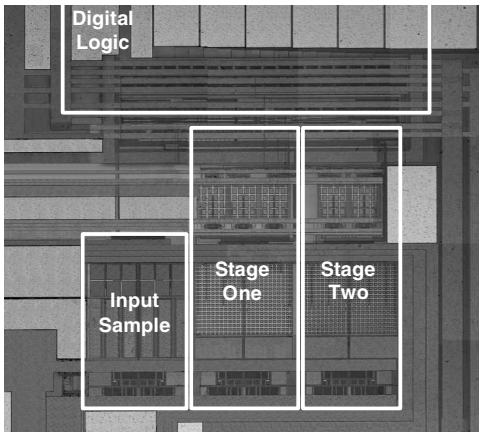

Figure 4: Die photograph.

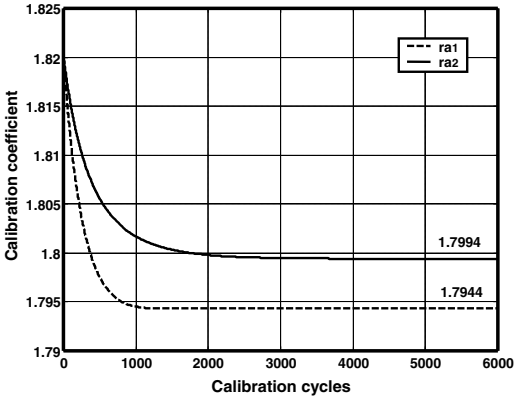

Figure 5: Measured radix convergence.

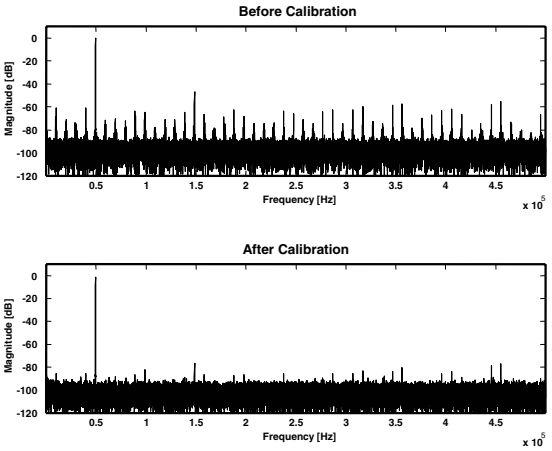

Figure 6: Measured output spectrum at V_{DD}=0.9V.

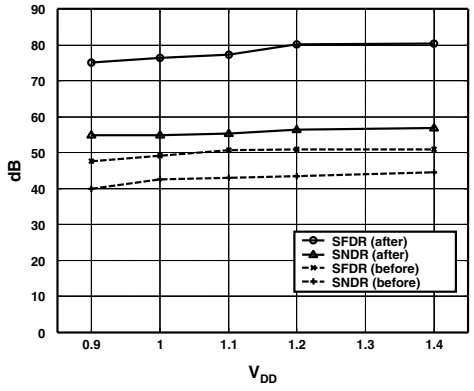

Figure 7: SNDR and SFDR vs. supply voltage.