A Sub-picosecond Resolution 0.5-1.5GHz Digital-to-Phase Converter

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Abstract

A digital-to-phase converter operating from 0.5-1.5GHz employs oversampling, noise shaping and DLL phase filtering to achieve sub-ps resolution independent of the operating frequency. Test chip fabricated in a 0.13μm CMOS process achieves a DNL below $\pm$100fs and $\pm$12ps INL and consumes 15mW while operating at 1GHz.

Introduction

The digital-to-phase converter (DPC) is an important building block in serial communication systems, instrumentation and in digital phase modulators. The two conventional ways to implement a DPC are depicted in Fig. 1. In the first method in Fig. 1(a) [1], the digital input word simply selects one of the many phases generated by a multi-phase generator such as a phase-locked loop (PLL). The resolution of this technique is severely limited by the minimum achievable delay in a given technology. The second method in Fig. 1(b) [2][3] overcomes this limitation by interpolating between two closely-spaced phases. However, this method also suffers from two major drawbacks. First, the interpolation linearity depends on phase-spacing, rise and fall times of the input phases and bandwidth of the interpolation buffers. Second, this technique requires rise and fall times to scale with frequency in order to maintain the accuracy, but that degrades jitter performance at lower frequencies. In this paper, we present an alternate technique that employs noise shaping and filtering to circumvent these drawbacks.

Proposed Architecture

A simplified block diagram of the proposed DPC architecture is shown in Fig. 2. As opposed to conventional phase interpolators, high resolution is achieved by dithering phases and filtering the quantization error with a low-pass phase filter. The three most significant bits of the 14-bit input digital word D_{IN} are used to select three out of the eight equally spaced phases $(\Phi_1 - \Phi_8)$ generated by the PLL. The remaining 11-bits are quantized to 3-levels $(\pm 1, 0)$ by a second-order delta-sigma modulator (DSM) and are then used to dither the $8:3$ multiplexor (mux) output phases. For example, if the required phase is between 67.5° and 112.5°, phases Φ_2, Φ_3, Φ_4 are dithered as indicated in Fig. 2. The shaped quantization error appears as high-frequency phase noise at the output of the $3:1$ mux. By filtering this phase noise with a low-pass filter, precise phase adjustment is achieved. Theoretically, with a 14-bit input word, a minimum phase step of 62fs is achievable at 1GHz. However, in practice, the resolution is limited by jitter on the dithered phases. In the following section, the implementation of the phase filter and the circuit details of various building blocks are described.

Circuit Design

An obvious choice for a low-pass phase filter is a PLL. However, a PLL poses conflicting requirements for bandwidth optimization to minimize jitter. While a large bandwidth suppresses VCO noise, input noise reduction mandates low-bandwidth operation. In order to overcome this bandwidth tradeoff, the modified delay-locked loop (DLL), shown in Fig. 3, is used. This DLL offers the benefits of low jitter and small area with little power overhead. A DLL is a simple first-order system with an all-pass transfer function. Two modifications were made to the conventional DLL to achieve the required low-pass transfer function and efficient filtering of the input phase noise. First, a *clean phase* of the PLL output is used as the reference input (Φ_{REF}) to the voltage-controlled delay line (VCDL), while the dithered *noisy phase* Φ_{IN} is used as the DLL input. As a result, it can be shown that Φ_{REF} and Φ_{IN} experience all-pass and low-pass transfer functions, respectively. Second, an active loop-filter is employed, and the higher-order poles arising from the opamp are optimized to suppress the quantization error of the DSM. The active loop-filter also biases the charge-pump to a fixed reference voltage (V_{REF}) irrespective of the VCDL delay, thus, minimizing noise folding of high-frequency phase noise due to the charge-pump nonlinearity. V_{REF} is nominally equal to half of the power supply voltage. False locking of the DLL is avoided by choosing Φ_{REF} to nominally have the same phase as Φ_{IN}, and resetting the VCDL to the minimum delay point at start-up. The remaining building blocks in the PLL and DLL design employ well-known conventional circuits. Glitch-free phase switching is achieved by synchronizing the selection signal with the mux output.

Experimental Results

The test chip fabricated in a 0.13μm CMOS process also contains built-in self test capability. As shown in Fig. 4, a digital accumulator is used to sweep the input word and a XOR phase detector is used to measure the output phase change. The measured DNL/INL plots are shown in Fig. 5. Several codes at the beginning and at the end were discarded to remove the nonlinearity due to XOR saturation. The repeating pattern, which is independent of operating frequency, shows that the INL is limited by inaccuracies in the phase-spacing of the multi-phase generator. This can be attributed to path mismatches in the layout. The DPC output jitter, when the DLL and DSM are reset is 3.8ps rms (Fig. 6). Jitter increases to 4.1ps rms (Fig. 7) under normal operating conditions, which implies the jitter contributed by the DLL and DSM is only 1.5ps rms. The measured phase-span is greater than π radians over the entire operating frequency range. The chip micrograph is shown in Fig. 8 and overall performance is summarized in Table. 1.

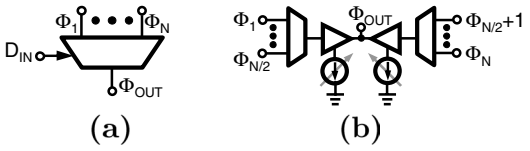

Figure 1: Conventional phase interpolators.

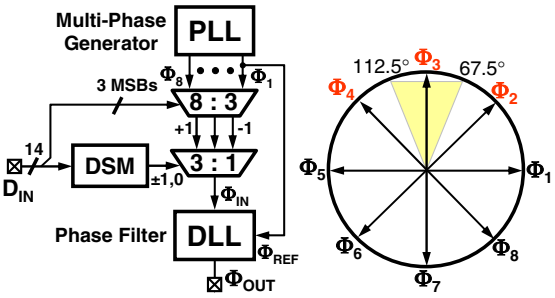

Figure 2: Proposed digital to phase converter architecture.

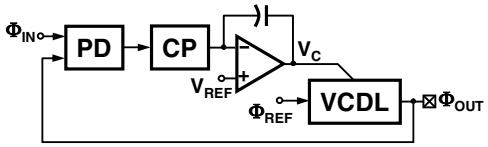

Figure 3: Filtering DLL with active loop filter.

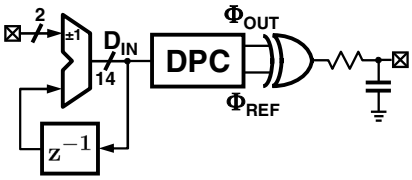

Figure 4: Simplified DPC built-in self test setup.

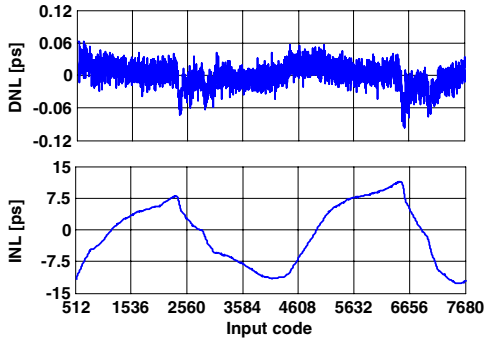

Figure 5: Measured DNL/INL at 1GHz.

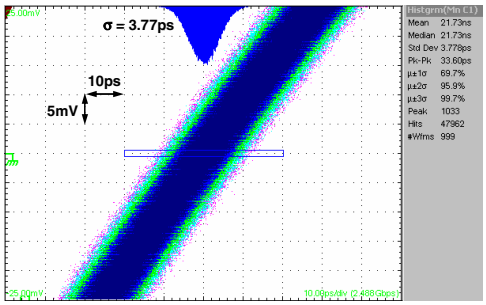

Figure 6: DPC jitter when DLL and DSM are reset.

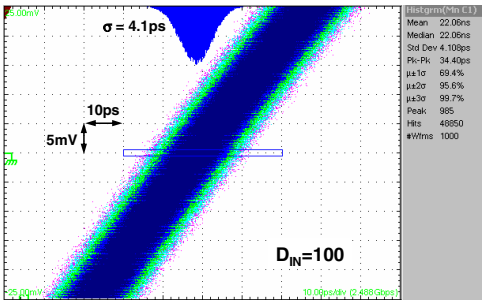

Figure 7: DPC jitter when input word is set to 100.

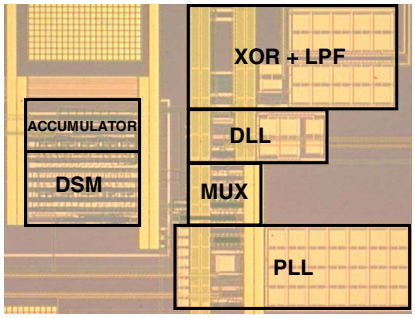

Figure 8: Chip micrograph.

Acknowledgments

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References

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Table 1: Performance Summary

Technology	0.13μm CMOS
Supply Voltage	1.2V
Operating Frequency	0.5-1.5GHz
DNL/INL	$\pm$150fs/$\pm$12ps @ 0.5GHz $\pm$100fs/$\pm$12ps @ 1GHz
Jitter @ 1GHz	PLL : 3.8ps rms DSM + DLL : 1.5ps rms Total: 4.1ps rms
Phase Span	$> \pi$ radians
Power Consumption @ 1GHz	PLL : 10mW DLL : 3.5mW Digital : 1.5mW Total : 15mW
Active Die Area	0.48mm^2