# Reconfigurable X-Band 4×4 Butler Array in 32nm CMOS SOI for Angle-Reject Arrays

***Abstract*—Introducing reconfigurable spatial filtering prior to ADC in digital beamforming (DBF) receiver (RX) arrays can improve the RX tolerance for in-band out-of-beam jammers. Such spatial filtering can be achieved using a Butler matrix that provides multibeam outputs. In this paper, an integrated 4×4 reconfigurable X-Band Butler matrix is designed in SOI CMOS to provide multibeam output with frequency tunability. The hybrid couplers that constitute the Butler matrix can also be configured to have <-15dB coupling ratio to create a thru-mode for the matrix. A prototype 4×4 Butler matrix using compact couplers is implemented in 32nm SOI with measured 9GHz to 13GHz frequency tuning range and ∼-2.5dB loss per coupler (die occupies 0.64 mm$^2$). Measurements also demonstrate desired multibeam formation and spatial filtering.**

***Index Terms*—Phased arrays, Butler matrix, CMOS, X-band**

## I. Introduction

Multi-element array receivers target spatial filtering (beamforming) and frequency filtering to capture desired signals from targeted directions while rejecting blockers that are separated from desired signals by frequency or spatial angle of incidence. Falling ADC costs and improving ADC performance has motivated interest in digital beamforming (DBF) for flexible array signal-processing [1]. In such arrays, signals from $N$ elements are sampled by $N$ ADCs, with subsequent digital signal processing (DSP) and spatial filtering (Fig. 1). DBF arrays can be equivalent to MIMO since each array element's output is available for DSP as opposed to traditional beamforming phased arrays that provide only one output. Interestingly, for several multi-functional array applications [1], [2], it is preferable to have DBF arrays with *spatial angle rejection/nulling* capabilities rather than phased arrays that perform *spatial angle selection*. However, deferring signal phase shifting and combining to the digital domain implies that in-band but out-of-beam jammers are present in the analog signal chain and are digitized by the ADC (Fig. 1), requiring high ADC dynamic range.

## II. Reconfigurable Multibeamforming Array

As shown in Fig. 2, an alternate architecture can be considered where a multi-beamformer is inserted prior to the ADCs. In this case, the $N$ ADCs digitize the $N$ outputs of a multi-beamformer. If the multibeam outputs provide a complete basis set, subsequent DBF can be used to recover the original signals at each antenna (Fig. 2). A significant advantage with this approach is that the *the jammer affects only a subset of the ADCs unlike in Fig. 1 where the jammer affects quantization in all ADCs*. In the example highlighted in Fig. 2, $ADC_N$ is affected by jammer which is spatially-filtered at other ADCs.

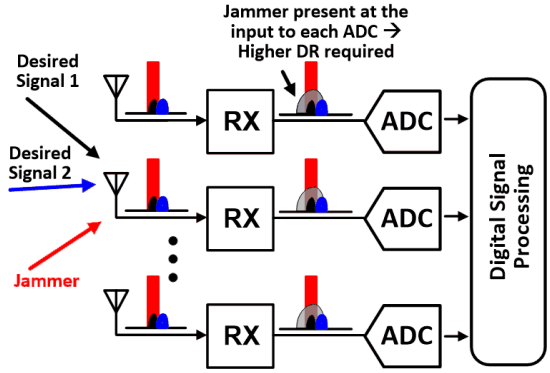


Fig. 1. Conventional DBF arrays do not suppress in-band, out-of-beam interferers → ADC dynamic range(DR) can limit jammer tolerance.

Since the desired signals are at different angles of incidence compared to the jammer - if $Q_N$ in Fig. 2 is ignored or assigned a small weight in the DSP, a spatial notch is created in the output, $T$, that can reject out-of-beam interferers. It is also desirable to have a mode in Fig. 2 which supports conventional DBF operation in the absence of interferers.

A Butler matrix [3] provides multibeam outputs and an integrated X-band Butler matrix is targeted as shown in Fig. 3(a) to achieve spatial filtering. Narrowband applications across the X-band are of interest. Since prior CMOS Butler arrays do not operate across the full X-band [4], frequency tunability and reconfigurable coupling must be incorporated to enable the spatial filtering block targeted in Fig. 2.

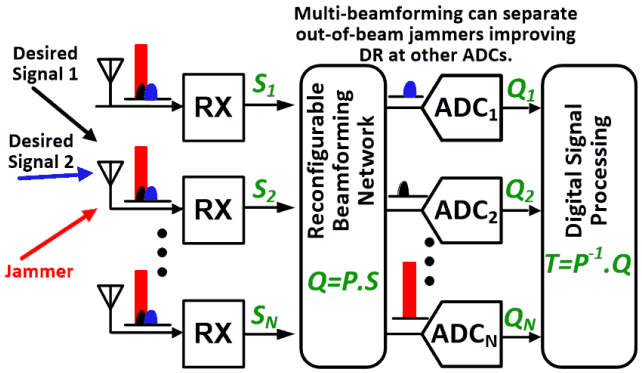


Fig. 2. Multi-beamformer prior to ADC can reject out-of-beam jammers (which appears only at $ADC_N$ in this case). Signals at all elements can be recovered in DSP since multibeam outputs form complete basis set.

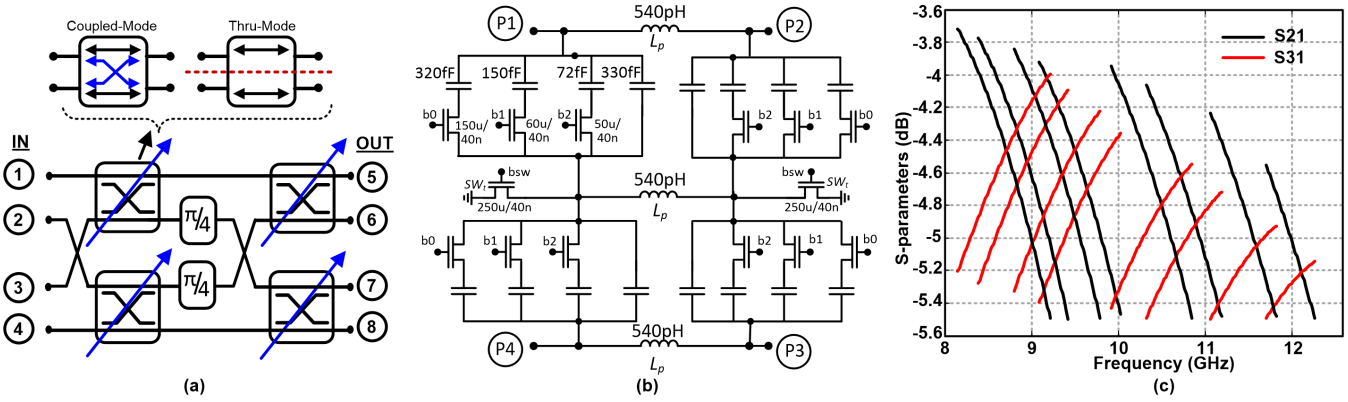


Fig. 3. (a) Multi-beamforming implemented using reconfigurable 4×4 Butler matrix, (b) Schematic of coupler with switched capacitor bank and thru mode, (c) Simulated performance based on insertion-loss and overall tuning range constrained optimization of switches and capacitances in Fig. 3(b).

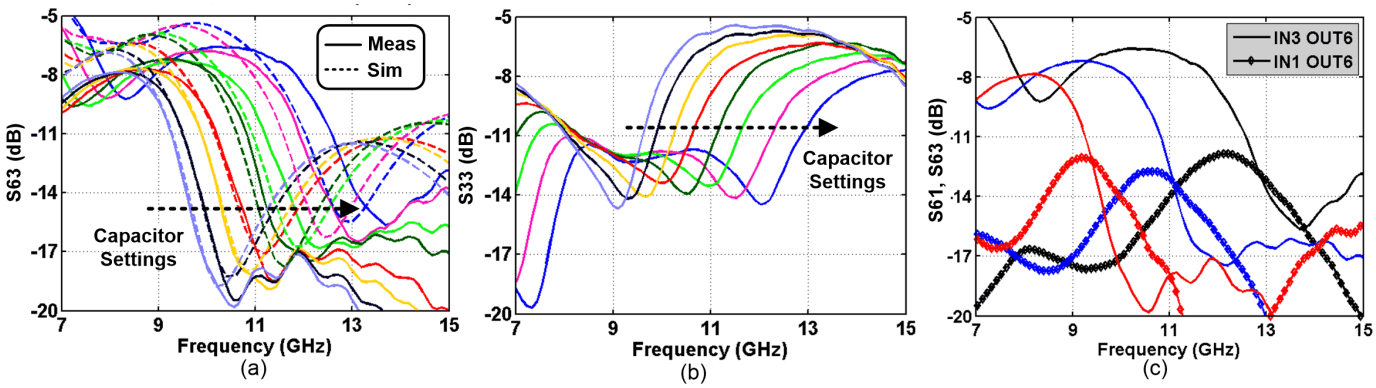


Fig. 4. (a) Measured and simulated performance across capacitor bank settings, (b) Measured input-match at Input 3 across capacitor bank settings, (c) Measured s-parameters (S63 and S61 in Fig. 3(a)) across capacitor bank settings.

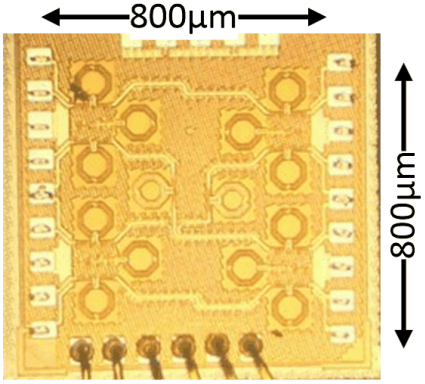


Fig. 5. Die photo of 4×4 Butler matrix in 32nm CMOS SOI.

## III. Design of CMOS Reconfigurable Butler Array

A reconfigurable hybrid coupler and a variable phase shifter are the key building block in the architecture in Fig. 3. An integrated implementation is targeted therefore compact area is necessary for practical feasibility. While wideband lumped couplers suited to CMOS integration have been proposed [5], adding reconfigurability and inductor losses showed high loss and large area for X-band Butler matrix implementation. Therefore, a hybrid coupler approach with high-pass and low-pass lumped element introduced in [6] is adopted in this work, as shown in Fig. 3(b). In this case, for 3-dB quadrature coupling at frequency, $\omega_0$ with impedance $Z_0$,

$$L_p = \frac{Z_0}{\omega_0};\ \ C_p = \frac{1}{Z_0\omega_0} \tag{1}$$

In this work, as shown in Fig. 3(b), a switched capacitor bank is used to provide capacitance, $C_p$, while $SW_t$, enables the thru path from $P1$ to $P2$ and from $P4$ to $P3$ in each coupler. On-state switch resistance and off-state capacitance limit coupler insertion loss and tuning range. Therefore, switch design is critical to optimize performance.

### A. Switch Design:

The switched capacitor-bank based architecture is well-suited to CMOS integration, particularly as technology scaling leads to improved switch performance. The switch Figure-of-Merit, ($FOM_{SW}$) captures the trade-off between on-resistance, $R_{ON}$ and off-state capacitance, $C_{OFF}$, where,

$$FOM_{SW} = R_{ON}C_{OFF} \tag{2}$$

While SOI technologies reduce parasitic capacitances improving $FOM_{SW}$, wiring parasitics contribute significantly to

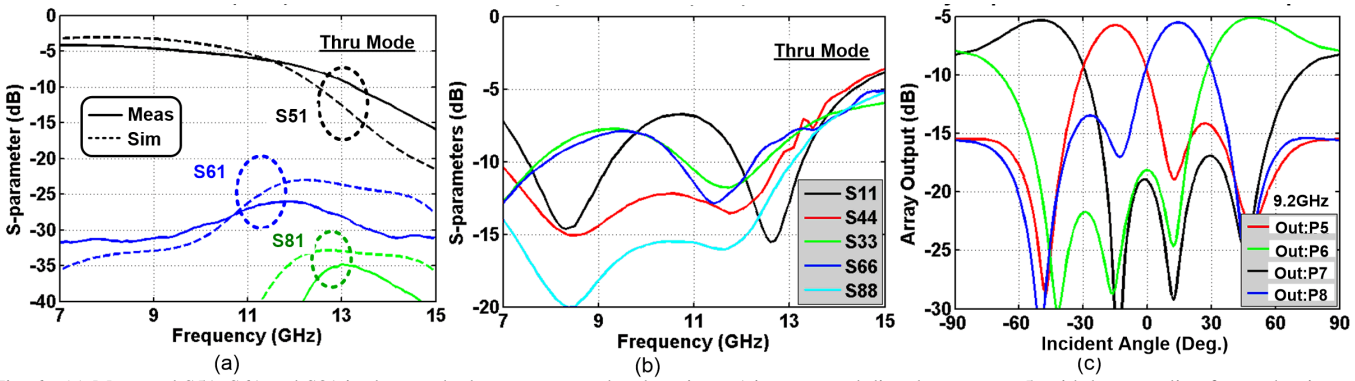


Fig. 6. (a) Measured S51, S61 and S81 in thru-mode demonstrate mode where input 1 is connected directly to output 5, with low coupling from other inputs, (b) Measured input match in thru-mode, (c) Array factor calculated from measured s-parameters at 9.2GHz with appropriate capacitor settings.

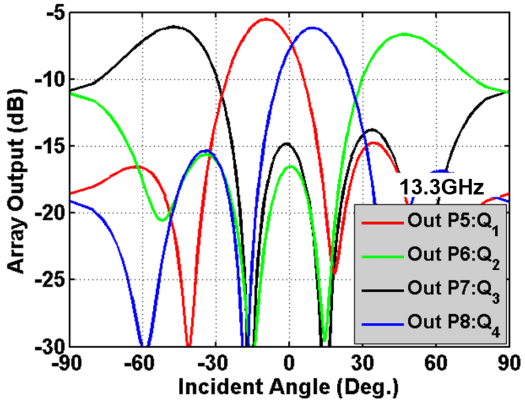


Fig. 7. Array factor calculated from measured s-parameters at 13.3GHz with appropriate capacitor bank settings

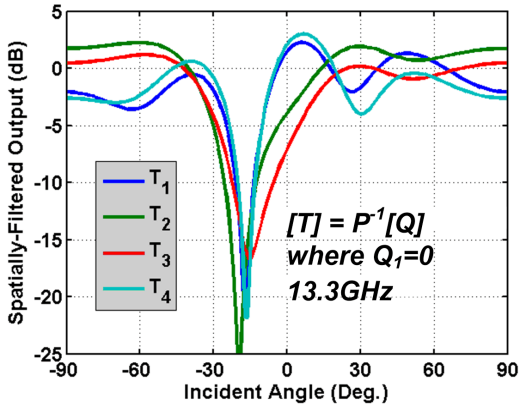


Fig. 8. Input signals recovered by applying inverse of Butler matrix, (Fig. 2) while zeroing *Out:P5* creating a spatial notch providing interferer suppression.

the capacitances in advanced nodes. Therefore, we increase the spacing between gate fingers to 0.25$\mu$m reducing wiring parasitics between the drain and source. Based on extracted simulations, increasing the gate pitch lowers parasitic by $>$20% improving the extracted $FOM_{SW}$ to 170fs.

An optimization procedure was developed for sizing inductors, capacitors and switch size in Fig. 3(b) to achieve operation across the X-band while constraining insertion loss and targeted tuning range. Simulated coupler performance is shown in Fig. 3(c). Comparisons of simulated and measured performance at the Butler matrix level are shown in Fig. 4.

## IV. Measured Performance

The design was implemented in a 32nm SOI process with a top-metal layer thickness of 1.2$\mu$m and occupies 0.8mm $\times$ 0.8mm (Fig. 5) with each coupler occupying $\sim$0.1 $mm^2$. Measured $s$-parameter in multi-beamforming mode and thru-modes are summarized in Fig. 4 and Fig. 6. As shown in Fig. 4(a,b), the coupler is frequency tunable from $\sim$9GHz to $\sim$13.5GHz - the higher frequency of operation compared to pre-tapeout simulations can by replicated by updating passive models (Fig. 4(a)). Thru-mode measurements in Fig. 6(a,b) demonstrate coupler operation with direct path between $P1$ and $P5$. The lower measured $S61$ and $S81$ provides isolation with respect to other inputs.

Multi-beamforming is demonstrated using the measured $s$-parameter data in Fig. 6(c) (at 9.2GHz) and Fig. 7 (at 13.3GHz). The inputs to the Butler matrix can be fully recovered from the 4$\times$4 matrix outputs following digitization, by applying the inverse of the Butler matrix ($P^{-1}$ in Fig. 2). This can provide spatial filtering - for example, Fig. 8 plots the recovered signals when *OUT:P5* in Fig. 7 is zeroed in the inverse operation. In this case, the recovered signals corresponding to the input ports (P1, P2, P3, and P4 in Fig. 3) with a spatial notch providing interferer suppression.

## References


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