2.2 A Scalable 28GHz Coupled-PLL in 65nm CMOS with Single-Wire Synchronization for Large-Scale 5G mm-Wave Arrays

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Demonstrations of mm-Wave arrays with >50 elements in silicon has led to an interest in large-scale mm-Wave MIMO arrays for 5G networks, which promise substantial improvements in network capacity [1,2]. Practical considerations result in such arrays being developed with a tiled approach, where *N* unit cells with *M* elements each are tiled to achieve large MIMO/phased arrays with *NM* elements [2]. Achieving stringent phase-noise specifications and scalable LO distribution to maintain phase coherence across different unit cell ICs/PCBs are a critical challenge. In this paper, we demonstrate a scalable, single-wire-synchronization architecture and circuits for mm-Wave arrays that preserve the simplicity of daisy-chained LO distribution, compensate for phase offset due to interconnects, and provide phase-noise improvement with increasing number of PLLs [3]. Measurements on a scalable 28GHz prototype demonstrate a 21% improvement in rms jitter and a 3.4dB improvement in phase noise at 10MHz offset when coupling 28GHz PLLs across three different ICs.

LO or reference distribution to PLLs on unit-cell ICs using a symmetric H-tree distribution network presents scalability challenges. While daisy-chained LO/reference distribution networks can provide a scalable approach, the reference-signal phase noise is degraded as it is transferred along the daisy-chain [2]. Additionally, the phase offset between elements must be calibrated due to unidirectional reference signaling. Importantly, both *H*-tree and daisy-chain schemes do not provide any performance benefits as the number of ICs (PLLs) operating in the array increase. Bidirectional coupling between PLLs as shown in Fig. 2.2.1 can eliminate phase offset variations and provide phase-noise improvement within the coupling bandwidth but this approach doubles the number of IO pins and increases the layout complexity. In this paper, we demonstrate a single-wire coupled-PLL approach (Fig. 2.2.1) that can couple two PLLs with only one interconnect between them. This approach is extended to a scalable synchronization scheme with dual-input PLLs, where the PLL on $Tile_K$ is coupled with the PLLs on $Tile_{K-1}$ and $Tile_{K+1}$ without adding any board-level overhead when compared to daisy-chained reference distribution. It can be shown that for dual-input type-II PLLs, a steady-state solution exists when a reference signal is present (shown for three PLLs in Fig. 2.2.1), albeit with a phase offset between the LO signals on multiple ICs. However, this static offset can be undesirable for a PLL and must be minimized. In comparison with coupled injection-locked oscillator-based arrays [4], the proposed architecture operates with a reference, and the type-II approach does not require static phase offsets for phase locking.

Figure 2.2.2 shows the schematic of the dual-input 28GHz PLL that targets the single-wire bidirectional PLL-coupling concept outlined in Fig. 2.2.1. The LO chain consists of a 25.3-to-30.4GHz LC-VCO that drives a low-power frequency-tunable injection-locked divide-by-two. Following this, a CML divide-by-four generates ~3.5GHz signal and drives PD1 and PD2 as well as the output buffers, *BUF1* and *BUF2*, that are matched to 50Ω. A type-II PLL with dual differential ~3.5GHz mixer-PD drives the differential VCO varactors. Critical challenges include: (a) achieving bidirectional coupling while distinguishing between the VCO signal and the reference signal at each common IO port and (b) accommodating interconnect phase shifts to achieve low static phase offset between the inputs to the phase detectors. The latter challenge is addressed by incorporating >2π variable phase shift in the path between the output driver ($BUF1_K$ *or* $BUF2_K$) on $Tile_K$ and the input to the phase detector ($PD2_{K-1}$ or $PD1_{K+1}$), respectively, on the adjacent PLL. First, output buffers, *BUF1* and *BUF2,* can select any one of quadrature phases from the CML dividers providing 90° coarse phase shift. Second, as detailed in the following, the IO-coupling block also provides variable-phase-shift capability to compensate for interconnect phase shifts. A low loop-bandwidth varies phase shift in the IO-coupling block to ensure a quadrature phase difference between the mixer-PD input signals at 3.5GHz, which is equivalent to $2m\pi$ phase offset at 28GHz.

Figure 2.2.3 shows the schematic of the ~3.5GHz IO-coupling block that (a) senses the input signal incident on *P1* and (b) provides a variable phase shift for signals travelling from *P2* to *P1*. The block is based on a 3dB quadrature coupler, where the coupled and through ports are terminated with high impedances. As shown in Fig. 2.2.3, the signals at *Thru* and *Cpl* are in quadrature with *Cpl* leading *Thru* for the input at *P1* and *Thru* leading *Cpl* for the input at *P2*. Therefore, a polyphase filter that combines the outputs at *Thru* and *Cpl* can reject signals from *P2* while only selecting signals from *P1* as shown in Fig. 2.2.3. In this work, a lumped 3.5GHz hybrid coupler is implemented using a transformer and MIM capacitors. The voltages at *Thru* and *Cpl* are sensed using transconductances ($G_{M1,2}$). Baluns at the output of $G_{M,1,2}$ create differential signals that drive a programmable *RC* polyphase filter. A variable capacitance, C_P, is included in the resonator of the G_{M12} to provide a variable phase shift. Figure 2.2.3 shows the simulated gain performance as well as the measured phase shift across quadrature polyphase outputs and capacitor, C_P, settings. The IO-coupling topology can further be viewed as a reflection-type phase shifter between P2 (buffer output) and P1 (chip input/output). A variable capacitance, C_{RTPS}, consisting of a digital coarse step and analog varactor, is included at *Thru* and *Cpl*, creating a variable phase shift between *P2* to *P1* without affecting the incident signal at *P1* that is sensed by G_{M1} and G_{M2}. The varactor is controlled by the DLL, which minimizes phase offset between PD inputs. Simulated insertion losses with and without the variable C_{RTPS} between *P1* and *P2* are 2.7-to-4.8dB and 1.6dB, respectively. The output buffer is matched to 50Ω and consumes ~3.5mA to generate a 0dBm output.

The dual-input 28GHz PLL is implemented in a 65nm CMOS process with 3.4mm-thick top-metal layer and occupies 1.5mm×1.6mm (including test circuits that occupy ~25% of the area). The IC is packaged using a Rogers 4350 board with chip-on-board packaging. The VCO and the PLL phase noise performance is characterized using an R&S FSUP26 signal analyzer. The measured VCO tuning range and the open-loop phase noise of the VCO with the injection locked divider and the CML dividers are shown in Fig. 2.2.4. The VCO achieves 18% tuning range at 27.5GHz, with an optimum FOM of ~181dB while consuming 3.9mW. The single PLL and the cascaded/coupled PLL performance are characterized at the divided 3.5GHz output. The stand-alone VCO and the divider chain achieve a phase noise of -135dBc/Hz at 10MHz offset for 3.5GHz output. Figure 2.2.5 shows the 28GHz PLL phase noise for the stand-alone PLL with the reference loop bandwidth of ~2MHz and a low-noise reference provided by an Anritsu MG3694C. In subsequent measurements, two and three PLLs are coupled with the setup shown in Fig. 2.2.5 and Fig. 2.2.6. Following a coarse phase calibration and DLL activation, the three PLLs are able to stay in lock throughout the varactor tuning range (~100MHz in each band). Transfer functions with respect to the reference input are measured to characterize loop bandwidths. Measured phase noise for a constant loop bandwidth (~2MHz) with two and three PLLs coupled are shown in Fig. 2.2.5 demonstrating ~3dB-to-5dB phase noise improvement. Measured phase noise with three PLLs in a cascaded and coupled mode is shown in Fig. 2.2.6 while the loop settings were calibrated to match the transfer function from the reference input to the output. When coupling is enabled, a phase noise improvement is observed within the coupling bandwidth (~40MHz) with lower PLL rms jitter of 104fs. Notably, PLL FOM [5] (including all buffer and G_M-cell power consumption) improves with increasing number of elements. The die micrograph is shown in Fig. 2.2.7.

Acknowledgements:
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References:
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[2] X. Gu et al., "A Compact 4-chip Package with 64 Embedded Dual-Polarization Antennas for W-band Phased-Array transceivers," *IEEE Electronic Components and Technology Conf.,* pp. 1272-1277, May 2014.
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[5] X. Gao et al., "Jitter Analysis and a Benchmarking Figure-of-Merit for Phase-Locked Loops," *IEEE Trans. Circuits and Systems-II*, vol. 56, no. 2, pp. 117-121, Feb. 2009.

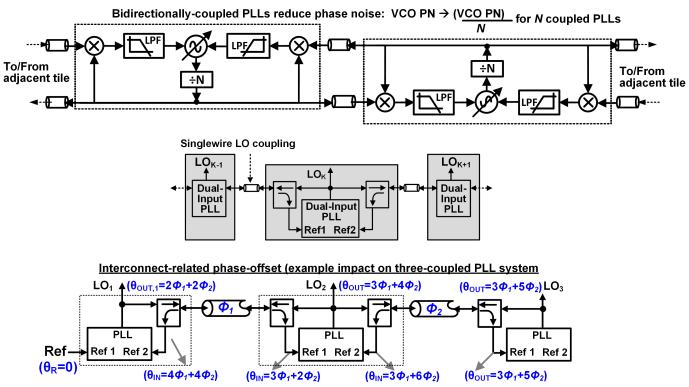


Figure 2.2.1: Proposed scalable, single-wire approach for coupling-PLLs across multiple ICs in a large-scale mm-Wave array, leading to reduction in phase noise and jitter.

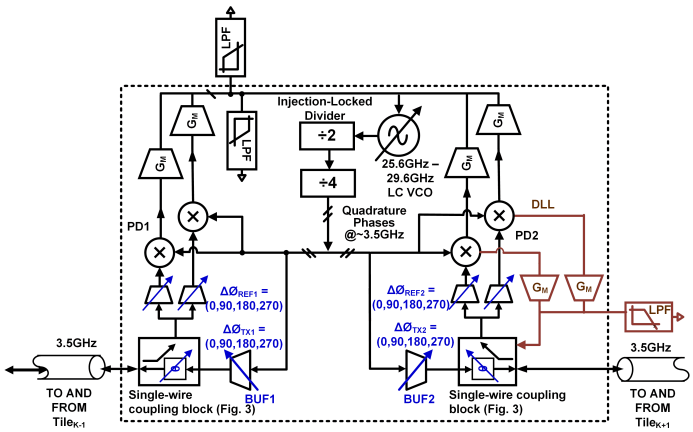


Figure 2.2.2: Schematic of a 28GHz dual-input PLL targeting scalable synchronization. A DLL with low loop bandwidth senses the phase offset and ensures quadrature input to mixer-PD.

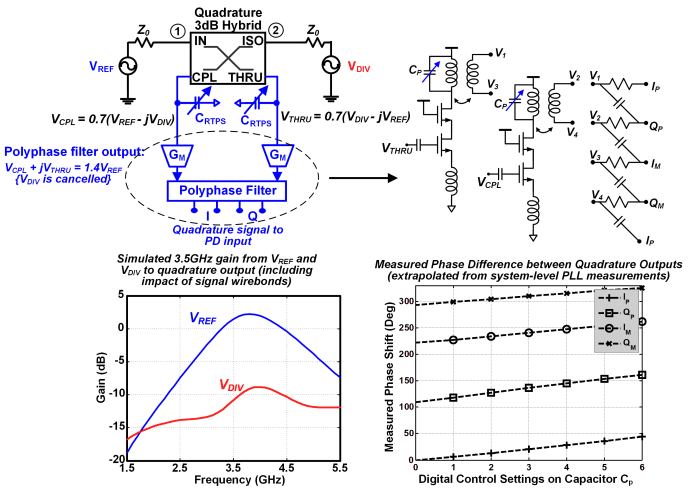


Figure 2.2.3: Schematic and simulated/measured performance of the 3.5GHz bidirectional IO coupling block.

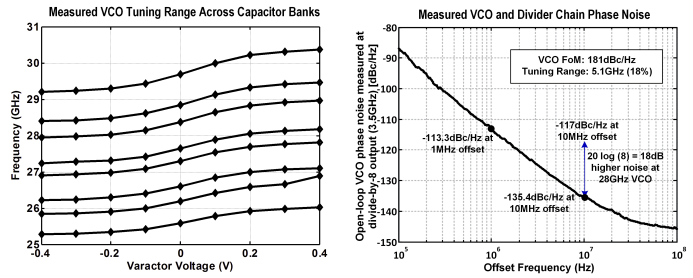


Figure 2.2.4: Measured 28GHz-VCO tuning range across switched capacitor banks and measured open-loop VCO phase noise.

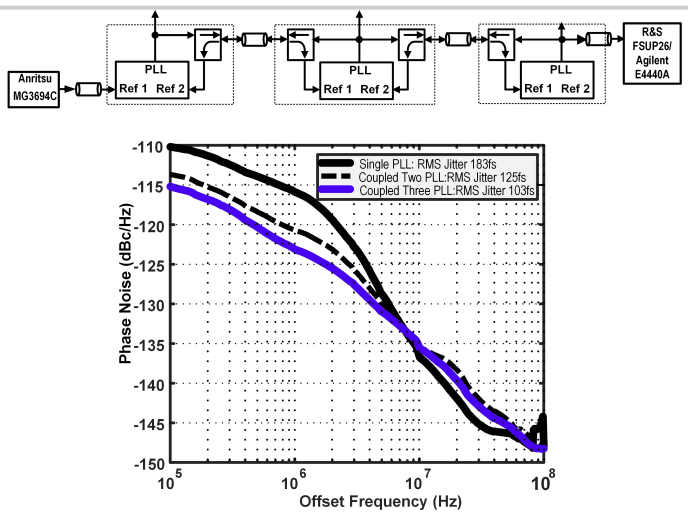
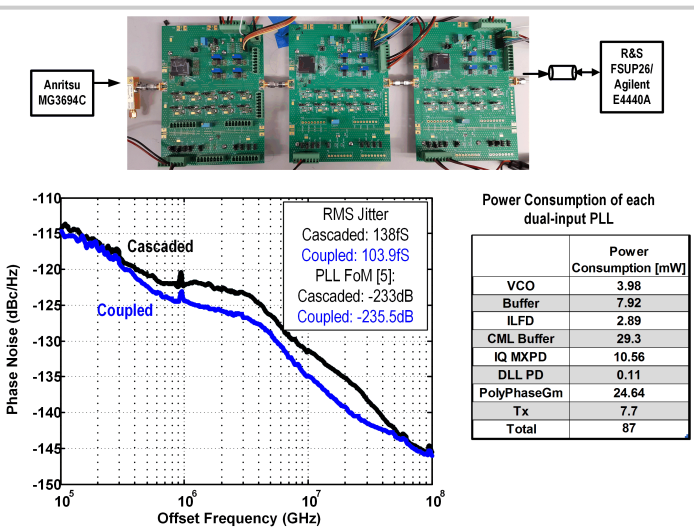


Figure 2.2.5: Measured 28GHz-PLL phase noise for a single PLL and with two and three PLLs coupled with a constant reference loop bandwidth (measurements at 3.5GHz divided output).



	Power Consumption [mW]
VCO	3.98
Buffer	7.92
ILFD	2.89
CML Buffer	29.3
IQ MXPD	10.56
DLL PD	0.11
PolyPhaseGm	24.64
Tx	7.7
Total	87

Figure 2.2.6: Measured performance of three PLLs. The PLLs are placed in cascaded or coupled mode based on the PD and output buffer settings.

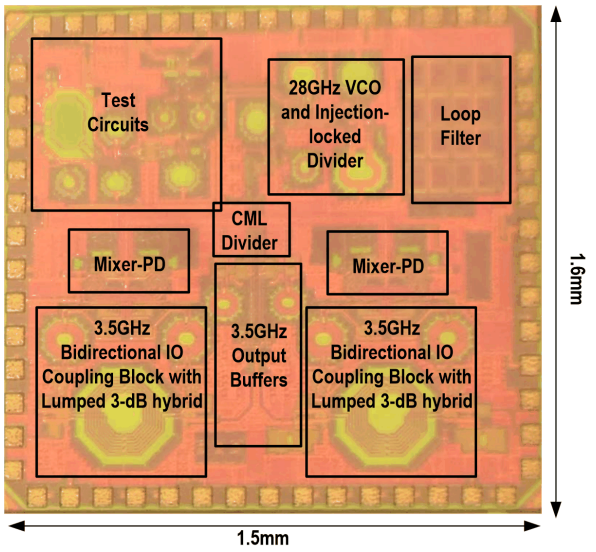


Figure 2.2.7: Die micrograph of the single-wire scalable 28GHz coupled PLL.

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