A 74.6GHz - 83.6GHz Digitally Controlled Oscillator with 370kHz Frequency Resolution in 65nm CMOS

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***Abstract*— All-digital PLLs promise flexible and precise FMCW radar signal generation for 77GHz radar applications. Such PLLs require digitally-controlled oscillators (DCO) with wide frequency tuning range (FTR) and high resolution to address a range of applications and low phase noise requirements. In this work, novel resonator structures with fine capacitance/inductance switching are embedded in a wide FTR common-source Colpitts DCO to achieve <1MHz DCO frequency resolution at 78GHz. The proposed structures also reduce dependence on switch-position for frequency step size, simplifying calibration. The DCO implemented in 65nm CMOS occupies 0.1mm^2 and consumes 15.6mW to achieve 74.6GHz - 83.6GHz FTR (11.4%) with 370kHz resolution, phase noise of -115dBc/Hz at 10MHz offset at 80GHz and state-of-the-art mm-wave DCO FoM-T of -182dBc/Hz.**

I. Introduction

Silicon integration of 77GHz collision-avoidance radar enables higher system complexity/performance. Such FMCW radar systems are being developed in advanced CMOS technologies [1] that are well-suited for all-digital PLL[2]. mm-Wave digitally-controlled oscillators (DCO) targeting such applications must simultaneously achieve wide frequency tuning range (FTR) to accommodate process variations/wideband applications and fine frequency resolution ($\sim$1MHz) to ensure low quantization-related phase noise. Since mm-wave DCO with $\sim$1MHz resolution require $<$ 10aF capacitance steps, high resolution is achieved in [2] by placing switchable distributed metal strips underneath inductors, leading to 160kHz frequency resolution but non-uniform step size, leading to a non-linear frequency tuning curve. An implementation with switchable metal strips underneath a transformer achieves uniform step size but only 2.5MHz frequency resolution [2]. In this work, we demonstrate a new switchable metal strip topology to achieve the highest frequency DCO (78GHz) with 370kHz resolution, uniform step size, and extensive overlap between frequency bands. A switched-capacitor ladder network is recently introduced in [3] to achieve <1kHz extrapolated resolution in a 60GHz DCO. The proposed passive resonator approach can also be applied in such networks to achieve high DCO resolution.

II. 78GHz DCO Design

A. Common-Source(CS)-Colpitts DCO:

Fig. 1(a) shows the schematic of the proposed DCO. It can be shown that the product of resonator quality factor, Q, and FTR is inversely proportional to frequency and to the technology-dependent switch time constant ($R_{ON}C_{OFF}$)[4]. Therefore, irrespective of frequency resolution, achieving wide FTR at 78GHz leads to low resonator Q (dominated by capacitor Q) ($\sim$5-8) in 65nm CMOS. At mm-wave, this challenge is further exacerbated since fixed transistor and layout parasitics dominate tank capacitance and limit FTR. A design study that included device parasitics was carried out across cross-coupled, common-drain (CD) Colpitts and CS-Colpitts topologies for the targeted 75 GHz to 82 GHz FTR (resonator model for the CS Colpitts is shown in Fig. 1(b)). Since C_{GS} is incorporated into a variable C_2 and there is no Miller multiplication of C_{GD} (Fig. 1(b)), the CS-Colpitts topology with variable C_1 and C_2 showed the largest tuning range for the same fractional variation in C_1 and hence was adopted in this work. From Fig. 1(b), the oscillation frequency is provided by,

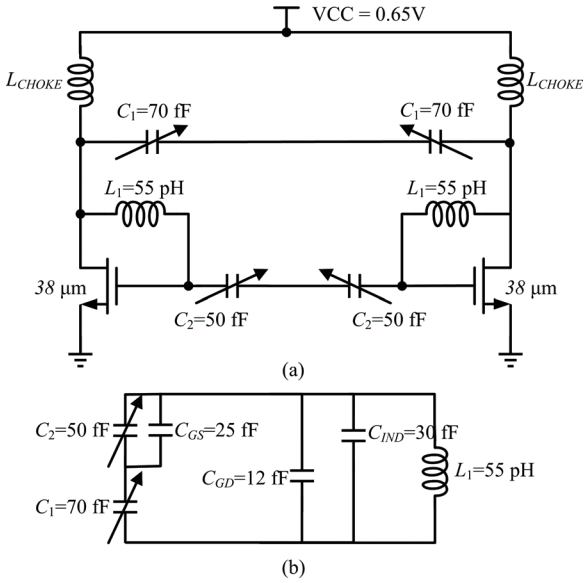

Fig. 1. (a) Schematic of 78GHz Common-Source Colpitts DCO (b) Equivalent circuit for resonator including device and inductor parasitics

$$f_0 = \frac{1}{2\pi\sqrt{L_1\left(\frac{C_1(C_2+C_{GS})}{C_1+C_2+C_{GS}} + C_{GD} + C_{IND}\right)}} \quad (1)$$

The variation in C_2 also provides an extra degree-of-

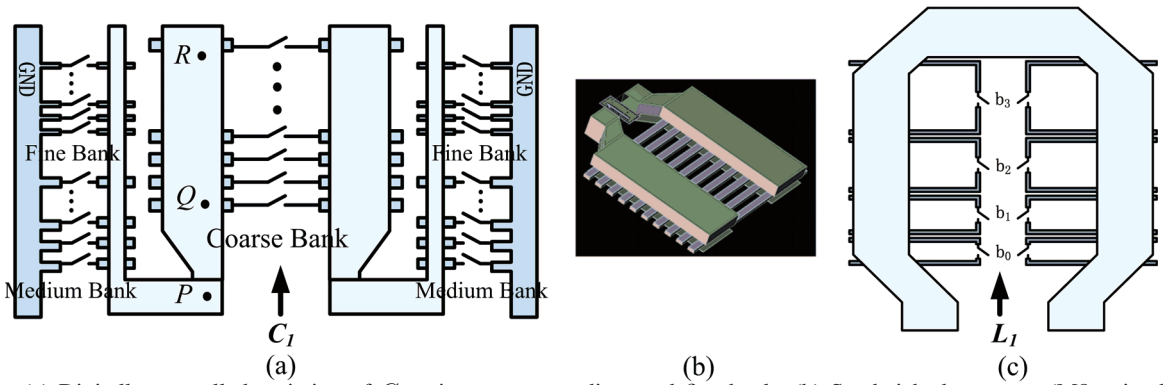

Fig. 2. (a) Digitally-controlled variation of C_1 using coarse, medium and fine banks (b) Sandwiched structure (M8 strips between M9 & M7 t-lines) to minimize parasitic inductances, (c) Switchable loop structures under inductor (L_1) for fine inductance variation

freedom to control the ratio between C_1 and $(C_2 + C_{GS})$ for higher FTR without degrading phase noise.

B. Digitally-controlled Resonator Design:

Assuming a 200MHz reference, frequency resolution of 500kHz leads to quantization related phase noise of $\sim -100dBc/Hz$ at 1MHz offset [2]. From (1), the frequency step due to change in capacitance, ΔC or a change in inductance, ΔL, can be shown to be,

$$\frac{\Delta f}{f_0} = \frac{-\Delta C_1}{2\left(C_1 + (1+m)\,C_P\right)} \frac{1}{1+m} \text{ and } \frac{\Delta f}{f_0} = \frac{-\Delta L}{2L_1}$$

where, $C_P = C_{GD} + C_{IND}$ and $m = C_1/\left(C_2 + C_{GS}\right)$. Therefore, achieving 1MHz resolution with L =56.12pH requires ΔL=1.38fH. Similarly, $\Delta C_1 \sim 7.3$aF is required to achieve a frequency step size of 1MHz. In this work, variation in each of C_1, C_2 and L_1 is implemented using switchable metal strips underneath resonator structures. In particular, C_1 is implemented using the structure in Fig. 2(a) where the capacitor is divided into coarse, medium and fine banks to achieve wide FTR with fine resolution.

A switch position-dependent ΔC_1 is observed in such resonator topologies (that are similar to [2]) due to differences in parasitic inductance. For e.g., in Fig. 2(a), $L_{PQ} \neq L_{PR} \rightarrow \Delta C_Q \neq \Delta C_R$. In this work, metal strips in $M8$ are sandwiched between the t-line implemented across $M9$ and $M7$ (Fig. 2(b)). This reduces difference between L_{PQ} and L_{PR}, minimizing position dependence. The location of coarse bank close to the $-G_M$ cell, followed by medium bank and fine bank also reduces position dependence by placing larger capacitors closer to the $-G_M$ cells.

Frequency resolution beyond fine capacitor bank is achieved using the inductor approach shown in Fig. 2(c). The switchable loop approach in this work resolves position dependence challenges that lead to non-uniform step size in [2]. It can be shown that with this approach, to the first order, ΔL depends upon the area of the loop being switched and is relatively independent of location relative to the inductor. This enables a binary switching approach targeting step size from ΔL to $15\Delta L$ (Fig. 3).

III. Measured Performance

The DCO was implemented in a 65nm CMOS process with 3.6um thick top-metal layer. The DCO occupies 0.32mm × 0.31mm (Fig. 4) and drives 3-stage buffer/CMOS PA with 0dBm output power (Fig. 4). The IC occupies 0.85mm × 0.75mm. The DCO was characterized by down-converting the mm-wave signal using a Spacek mixer and phase noise was measured using a Rohde & Schwarz FSUP 26 signal analyzer.

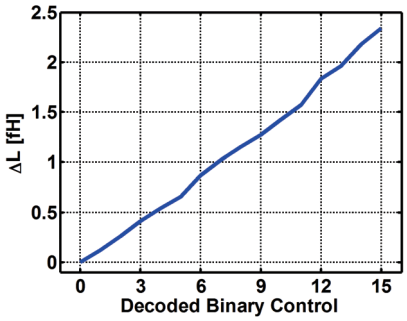

Fig. 3. Simulated inductance step across inductor switch settings (binary-coded based on area of loop)

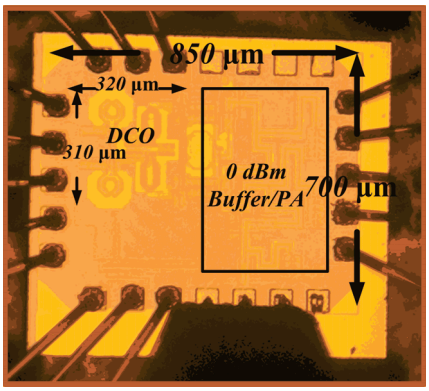

Fig. 4. Die photo of 78GHz DCO in 65nm CMOS (includes buffer and 0dBm PA)

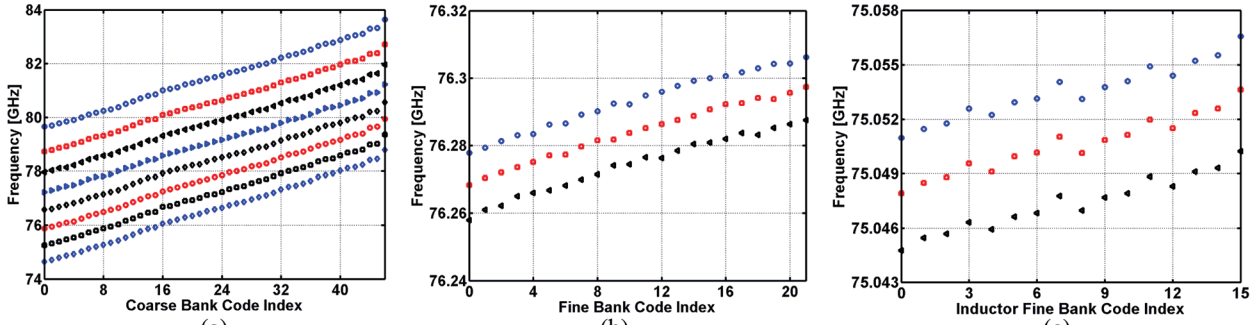

Fig. 5. (a) Measured DCO tuning range across coarse C_1 settings (b) Measured DCO tuning across fine C_1 demonstrating 1.35MHz resolution (c) Measured DCO tuning range across L_1 settings demonstrating 370kHz resolution with overlap across all bands.

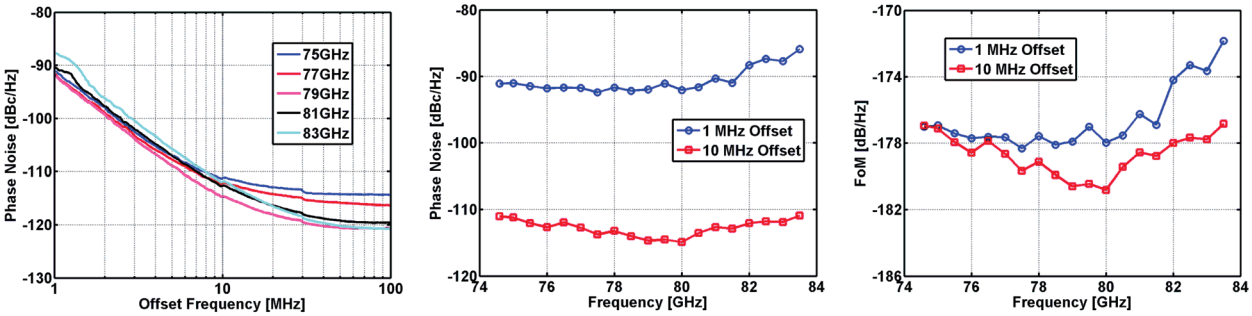

Fig. 6. (a) Measured DCO phase noise across FTR (b,c) Measured DCO PN and FoM at 1MHz and 10MHz offset across FTR

Measured DCO tuning range across coarse codes is shown in Fig. 5(a) demonstrating a tuning range of 74.6GHz to 83.6GHz (11.4% FTR), with overlap between codes. Medium bank shows similar overlap. Measured frequency across fine capacitance bank codes is shown in Fig. 5(b) demonstrating 1.35MHz resolution. The frequency range and step-size are (4.14GHz, 88MHz), (132MHz, 8.8MHz) and (29.6MHz, 1.35MHz) in coarse, medium and fine-banks respectively. This corresponds to capacitance step sizes of 0.7fF, 81aF and 8aF.

Measured frequency across inductor settings is shown in Fig. 5(c) demonstrating 370kHz resolution and 5.5MHz range at 75GHz, with relatively uniform step size. This translates to dithering-less raw quantization-noise related phase noise of -102.5dBc/Hz at 1MHz offset assuming 200MHz reference (∼12dB lower than the DCO phase noise of -90dBc/Hz at 1MHz offset).

Measured phase noise at different offset at five different frequencies is shown in Fig. 6(a). Measured DCO phase noise and VCO Figure-of-Merit (FoM) at 1MHz and 10MHz offset are plotted across frequency in Fig. 6(b) and Fig. 6(c). Measured DCO performance is summarized in Table 1, demonstrating competitive performance at the highest frequency of operation.

ACKNOWLEDGEMENT

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TABLE I
COMPARISON WITH THE STATE-OF-THE-ART

	This work	[5]	[3]	[2] L-DCO	[2] T-DCO
f_0 (GHz)	74.6-83.6	51.3-53.3	54.8-63.2	56.2-62.2	55.9-61.6
PN (dBc/Hz) Offset (MHz)	-114.9 (10)	-116.5 (10)	-94.1 (1)	-93 (1)	-94 (1)
P_{DC} (mW)	15.6	2.3	18	12	14
FoM (dBc/Hz)	-180.9	-187.2	-176.9	177.9	-177.9
FoMT (dBc/Hz)	-182.1	-179.2	-180	-177.9	-177.9
FoM-DT (dBc/Hz)	-185.3	-179.2	-184.2* -190.4**	-181.3	-179.3
CMOS	65nm	90nm	65nm	90nm	90nm

*:measured; **:extrapolated

$$FoM = PN - 20 \cdot log_{10}(f_0/\Delta f) + 10 \cdot log_{10}(P_{DC}/1mW)$$
$$FoM_T = FoM - 20 \cdot log_{10}(FTR/10)$$
$$FoM_{DT} = FoM_T - 20 \cdot log_{10}(N_{eff}/10)$$

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