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Millimeter-wave IC-Antenna Cointegration for Integrated Transmitters and Receivers

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***Abstract*—Advances in CMOS and SiGe technologies have made mm-wave multi-element arrays with complex architectures, high yields and good inter-element matching feasible. However, Antenna-in-Package approach is challenging with larger number of array elements due to the increase in mm-wave I/O, the need for impedance-controlled via/routing symmetry. In this work, we describe an antenna-IC co-integration approach that relies on aperture coupling between on-chip feed/ground-plane slot and an antenna-on-substrate to simultaneously achieve wide bandwidth and high efficiency. The proposed approach is validated through a 60-GHz packaged prototype in which a 60-GHz quadrupler and aperture-coupled antenna feed fabricated in a 0.18-μm SiGe technology is co-integrated with a 60-GHz patch antenna on a 100-μm LCP substrate. Measured E-plane and H-plane antenna patterns show 0 dB gain at 61 GHz (corresponding to 40% efficiency) and cross-polarization ratio of $\sim$10 dB demonstrating the feasibility of the proposed approach.**

***Index Terms*—On-chip antenna, Aperture-coupled, antenna, co-integration, mm-wave, CMOS, BiCMOS, transceivers, LCP**

I. Introduction

Integrated mm-wave transmit and receive arrays have been demonstrated in SiGe BiCMOS and CMOS, demonstrating the feasibility of low-cost multi-functional arrays for communication/imaging applications [1]–[3]. Silicon integration results in excellent yields and gain/phase matching for complex arrays. This has led to increasing interest in scalable, large-scale arrays with hundreds of elements built using multi-element unit-cells tiled in X and Y dimensions [1], [2]. While silicon ICs can achieve high yields, the mm-wave interface between the IC and the package is challenging for large number of mm-wave IO. Antenna-in-package (AiP) approaches have been investigated for multi-element mm-wave ICs using low-temperature co-fired ceramics (LTCC) and multi-layer organic laminates (MLO) [4]. However, large number of impedance-controlled lines being routed in a compact area on a package leads to element-to-element mismatches, need for impedance-controlled vias, and significant routing losses. For example, >1.5-dB interconnect loss in [4] reduces overall efficiency to 63% even if 90% antennas efficiency is assumed.

On-chip antennas are attractive for such mm-wave arrays if comparable system performance can be achieved. However, silicon substrate has high dielectric constant ($\sim$ 11.7) and often low resistivity ($\sim$ 10Ω-cm), leading to low efficiency if EM energy is confined inside the substrate by the antenna.

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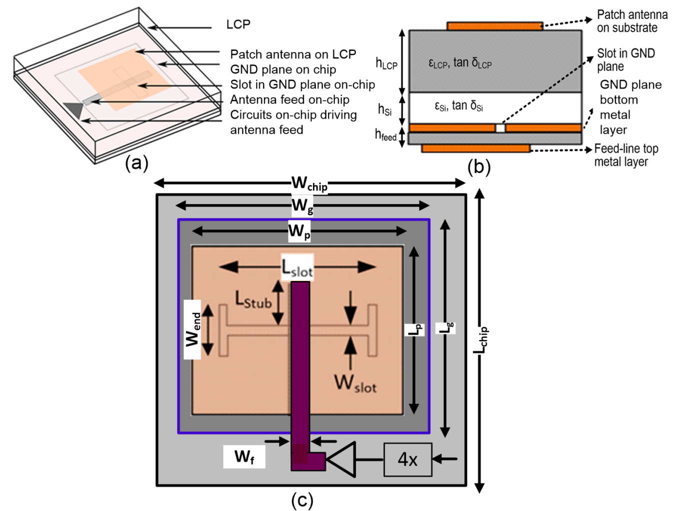

Fig. 1. Proposed antenna-cointegration scheme with on-chip feed and slot aperture-coupled to antenna on LCP substrate bonded to backside of die (a) Top-view (b) Side-view.

While an on-chip ground plane can isolate the substrate, antenna to ground plane distance is limited to 9-15 μm leading to poor radiation efficiency and narrow bandwidths. On-chip antenna performance can be improved by adding a superstrate on top of the antenna [5] or by proximity coupling to an antenna on a superstrate [6]. However, this presents large-scale packaging challenges since all other IO must also be accessed through wirebond and flip-chip pads on the frontside of the IC. While a wafer-scale approach has been proposed with custom lithography in [7], performance is affected if IO and supply/ground routing is restricted to the periphery as opposed to internal supply and IO pads, similar to [4].

In this work, we propose a wafer-scale compatible antenna-IC co-integration approach that significantly simplifies mm-wave packaging and test by eliminating mm-wave I/O to/from the IC while potentially achieving $\sim$50% efficiency and $\sim$15% bandwidth simultaneously (Fig. 1). This performance is competitive with overall efficiencies achieved with state-of-the-art MLO and LTCC packaging. Section II details the proposed antenna concept while design methodology and simulated performance are discussed in Section III. Measured performance of a 60-GHz prototype is described in Section IV. Finally, Section V discusses conclusions and future directions.

II. Proposed Approach

Fig. 1 shows the proposed wafer-scale compatible antenna-cointegration scheme that relies on aperture-coupling between the on-chip feed and the patch antenna on a substrate that

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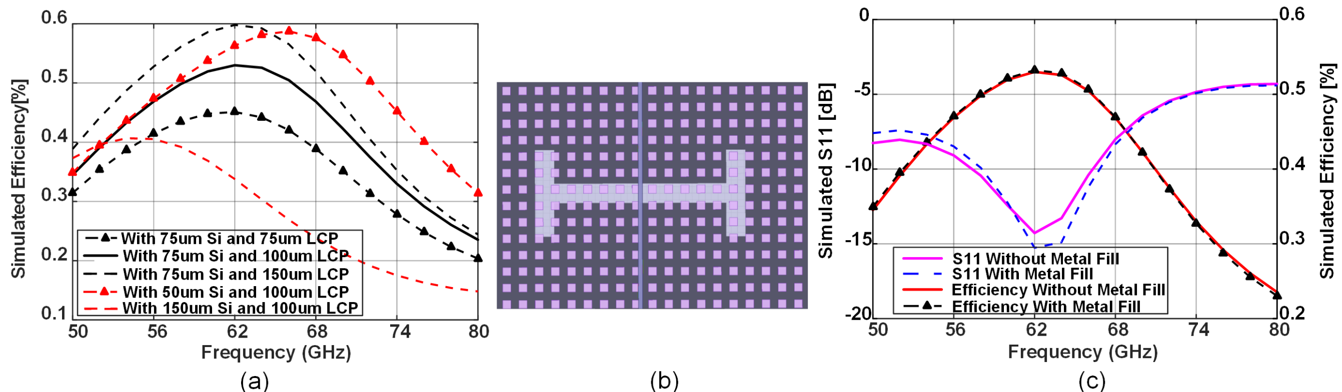

Fig. 2. (a) Efficiency variation with different LCP and silicon thickness, (b) Feedline and slot with metal fill, (c) Impact of metal fill on S11 and efficiency.

is bonded to a thinned silicon IC. The thick top-metal layer on the IC is used for antenna feed and accompanying ground plane is created using the lower metal layers. CMOS lithography allows the creation of a precise slot in the ground-plane that aperture-couples the feed to a patch antenna on the substrate without the need for any off-chip vias that conduct mm-wave signal. The silicon die (or wafer) with circuits is thinned to reduce loss. The patch antenna metalization is created on the substrate, and the die (or wafer) and substrate can be bonded together using well-established adhesive techniques. From an antenna performance perspective, this technique preserves all the benefits of aperture coupling - wide bandwidth as well as isolation between the antenna layer and feed line layer, which allows for transmision line (t-line) structures to be created without interfering with antenna performance. Bandwidth enhancement techniques such as stacked aperture-coupled patches [8] are also potentially feasible.

As will be shown in simulation (Section III) and measurement, efficiencies of over 50% are feasible, with overall performance comparable to complex AiP approaches. While the slot and ground-plane occupy IC area, this is common to other antenna-on-chip approaches [5], [6]. The proposed backside-radiation scheme is relatively insensitive to metal-fill rules, compatible with wirebonding/flip-chip packaging, and is well-suited for CMOS or SiGe wafer-scale post-processing since only wafer-thinning is required.

III. Antenna Design

As shown in Fig. 1, design variables include patch and slot dimensions ($L_p, W_p, W_{slot}, L_{slot}$, and W_{end}), on-chip ground plane size (W_g and L_g), feed structure parameters (L_{stub}) and substrate parameters (ϵ_{LCP}, h_{LCP} and h_{si}).

A. Substrate material parameters and dimensions:

Since wafer-scale compatibility is targeted, the patch substrate material must have low dielectric constant, low loss at mm-wave and silicon-compatible coefficient of thermal expansion. Liquid Crystal Polymer (LCP) has been identified as a potential low-cost, high performance, mm-wave substrate [9] and is selected in this work. Notably, similar performance is also achieved in simulation with quartz as the substrate. LCP has a low dielectric constant ($\epsilon_{LCP} \sim 3.1$) and low loss at mm-wave ($\tan\delta_{LCP} \sim 0.003$) which is comparable to LTCC. While increasing LCP substrate thickness can initially lead to higher radiation efficiency and bandwidth, a very thick substrate leads to lower efficiency due to surface-wave loss.

The impact of silicon and LCP thickness are shown in Fig. 2 - reducing silicon thickness improves efficiency, for e.g. changing thickness from 150 μm to 50 μm improves efficiency from 38% to >50%. While thinning silicon dies can lead to reliability challenges, 3D IC integration has motivated research into die thinning and bonding techniques for robust packaging. In the prototype, silicon thickness of $\sim$75 μm is selected to balance efficiency with ease of chip handling for packaging. Similarly, increasing LCP thickness from 75 μm to 150 μm can increase efficiency as well. Readily-available LCP material with 100 um thickness (Rogers 3850) is used, leading to 52% efficiency and 9-GHz bandwidth in simulation (Fig. 2(a)).

B. Aperture-coupled patch and slot design:

The patch antenna length, L_p, is determined using,

$$f_0 = \frac{c}{2\left(L + 2\Delta L\right)\sqrt{\epsilon_{eff}}} \tag{1}$$

where ϵ_{eff} is the effective dielectric constant that includes impact of silicon and LCP substrate, f_0 is the resonant frequency, and ΔL is additional length due to fringing fields. A ratio of W_p/L_p between 1 and 2 is targeted to get good bandwidth and efficiency without degrading cross-polarization and generating undesired modes [10]. The coupling between the feed-line and patch and the front-to-back ratio is primarily determined by the slot/aperture dimensions (L_{slot} and W_{end}).A large L_{slot} is desirable to increase coupling. However, this also degrades front-to-back and cross-polarization ratios. Hence, a dogbone-shaped slot is used to boost coupling between feed-line and patch without degrading front-to-back ratio [11].

While the ground plane dimensions (W_g and L_g) affect pattern and efficiency, size is limited by die area. Simulations show that when ground plane size is increased from 1.2 mm$\times$1.2 mm to 2 mm $\times$ 2 mm, f_0 varies from 60.6 GHz to 63.1 GHz, and efficiency increases from 44% to 51%. Ground plane impact can also be viewed in the context of typical micro-strip antennas as predicted in [12] - in this work, size is limited to 2 mm $\times$ 2 mm to limit die size.

C. Impact of metal density and metal fill:

Floating metal-fill structures are placed in each metalization layer to satisfy metal density rules to ensure performance/yield of interconnect in silicon. Such rules can require density

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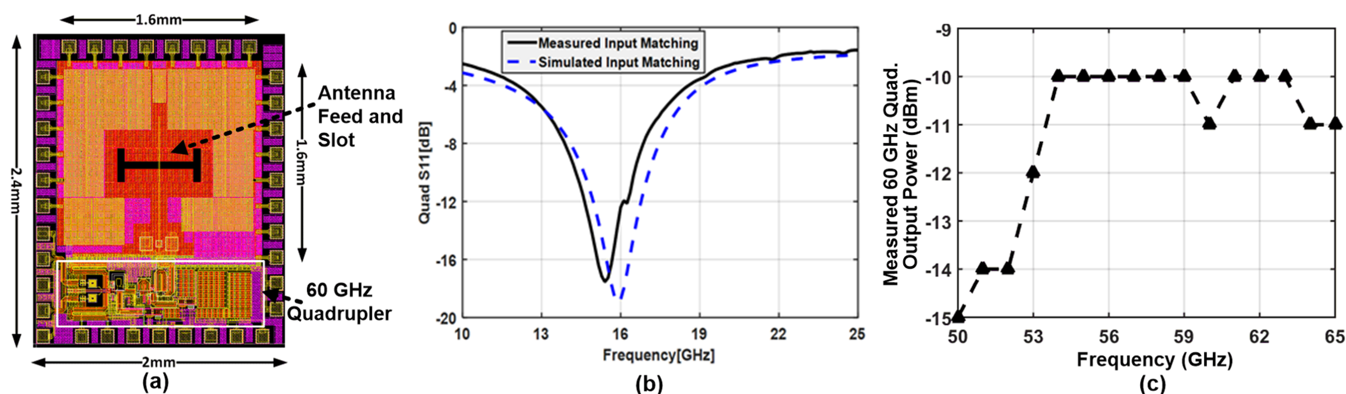

Fig. 3. (a) Die photo of 60-GHz quadrupler integrated with on-chip feed/slot and off-chip patch, (b) Measured 60-GHz quadrupler input matching, and (c) Measured 60-GHz quadrupler output power.

TABLE I
ON-CHIP ANTENNA DESIGN PARAMETERS

Parameters	Value	Parameters	Value
W_p	1.25mm	L_g	1.6mm
L_p	0.95mm	h_{LCP}	100μm
W_{slot}	60μm	ϵ_{LCP}	3.14
L_{slot}	650μm	$\tan\delta_{LCP}$	0.0025
W_{end}	365μm	ϵ_{si}	11.7
L_{stub}	375μm	$\tan\delta_{si}$	0.015
W_g	1.6 mm	h_{si}	75μm

>10% and can impact antenna performance. For example, metal-fill reduces efficiency in [5] from 40% to 29%. The proposed approach is relatively insensitive to metal fill since the ground plane in the lowest three metal layers shields the antenna from the higher metal layers. Simulations with floating metal structures have negligible impact on performance (Fig. 2(b,c)), demonstrating the advantages of this approach. Density rules also require slots in the ground plane, however a continuous ground plane is achieved by stitching together the lowest three metal layers. Table I shows all design parameters which include the impact of finite ground plane. As shown in Fig. 2(c), the structure achieves 52% simulated efficiency (including antenna feed, with 2.8-μm top-metal thickness and loss of 10.5 $m\Omega$/sq) and $>$ 9-GHz bandwidth at 60 GHz.

IV. MEASUREMENT RESULTS

The proposed antenna and IC co-integration is implemented in 0.18-μm TowerJazz SiGe technology. Fig. 3(a) shows the IC die photograph which includes 60-GHz antenna feed and slot structures. Antenna testing is simplified by integrating a 60-GHz quadrupler along with the antenna. The quadrupler requires a 15-GHz input signal. The technology has a 2.8-μm thick top metal layer and 0.52-μm thick bottom layers. Test pads are included in the structure to measure the quadrupler output power, and hence, the input power to the antenna feed. In this measurement, the antenna-feed is disconnected using ion-beam trimming and test pads are accessed in a probe-based setup. The quadrupler input match across frequency is shown in Fig. 3(b). As shown in Fig. 3(c), the DC bias and input power settings are varied to achieve $\sim$-10 dBm at quadrupler output across the 60 GHz band in the probe-based setup.

The antenna and IC are characterized using a test fixture shown in Fig. 4. Measured antenna patterns are shown at

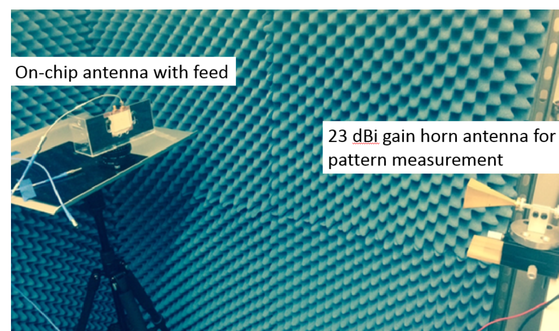

Fig. 4. Measurement setup to characterize 60-GHz antenna pattern and gain

56 GHz, 57.2 GHz, 59.2 GHz and 61.52 GHz in Fig. 5 and Fig. 6. Measured performance is compared to simulations with and without the measurement setup. In simulation and measurement, the setup introduces assymmetry in measured patterns and limits correlation, particularly at oblique angles. Data from two measurements is plotted to verify repeatability. As discussed in Section III the slot-structure causes radiation from the top of the IC as well with a measured front-to-back ratio of $\sim$6-8 dB at four different frequencies. The measured antenna efficiency (Fig. 7) is estimated by averaging the output power in $\pm 20^o$ in the E and H plane to calculate the effective radiated power and compared to simulations including measurement setup. Table II shows comparison with the state-of-the-art demonstrating efficiency higher than purely on-chip antenna approaches and comparable to superstrate approaches [6], while providing simpler packaging and test.

V. CONCLUSION

A wafer-scale compatible mm-wave IC-antenna co-integration approach is presented that demonstrated efficiency and bandwidths comparable to system-level performance with AiP techniques. A 60-GHz prototype using the proposed aperture-coupled backside radiation approach was fabricated with an on-chip quadrupler and antenna feed. The prototype achieves 0-dBi gain, 40% efficiency, and 10-dB cross-pol ratio and is well-suited for wafer-scale packaging. Further improvements in bandwidths are feasible with stacked patches and polarization ratio can be improved with better alignment between the patch and on-chip slot. The proposed approach can enable on-chip calibration for large-scale mm-wave arrays.

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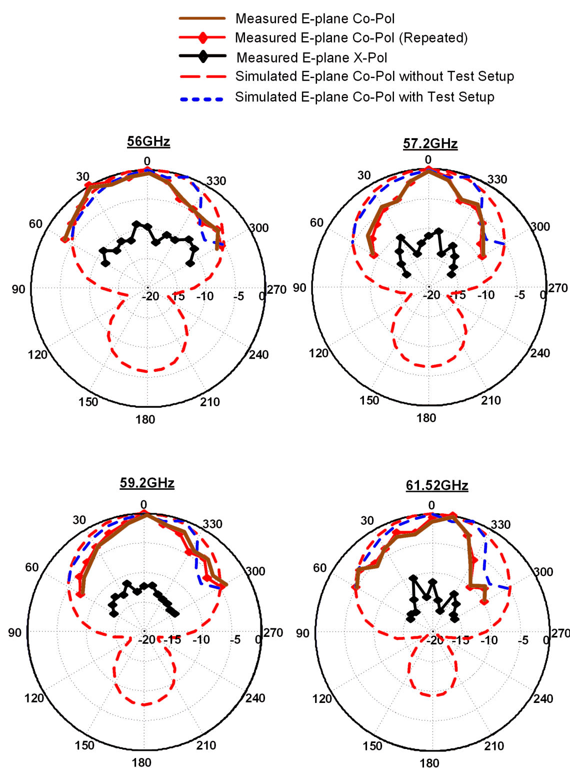

Fig. 5. E-plane co-pol and cross-pol patterns at 56 GHz, 57.2 GHz, 59.2 GHz and 61.5 GHz

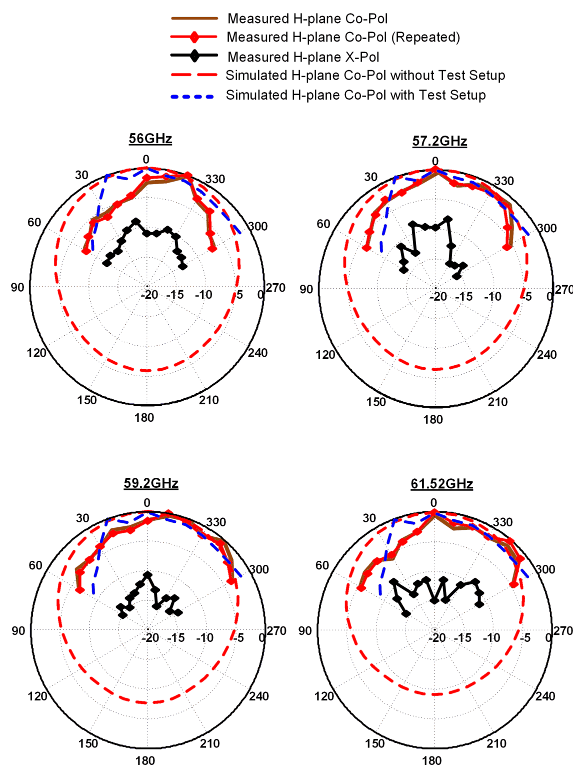

Fig. 6. H-plane co-pol and cross-pol patterns at 56 GHz, 57.2 GHz, 59.2 GHz and 61.5 GHz

TABLE II
COMPARISON WITH THE STATE-OF-THE-ART

Ref.	Approach	Freq (GHz)	BW (GHz)	Gain (dBi) (Eff.)
This work	Aperture-coupled to patch on LCP substrate	60	8	0 (40%)
[6]	Proximity-coupling to patch on quarz superstrate	94	7.5	3 (50%)
[13]	Leaky-wave thin AMC	94	10	-2.5
[5]	Elliptical Slot with quartz superstrate	94	3.6	0.7 (26%)
[14]	Slot-folded dipole antenna	94	33	-4 (20%)

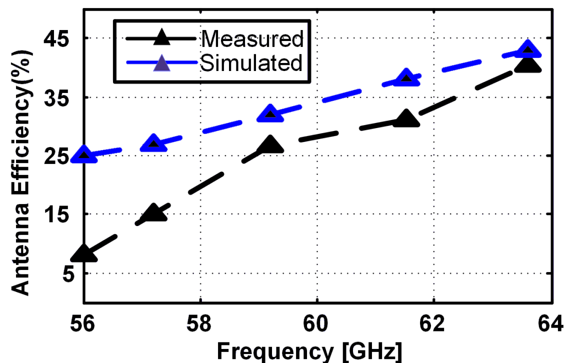

Fig. 7. Measured antenna efficiency based on pattern in Fig. 5 and Fig. 3(c).

VI. ACKNOWLEDGEMENT

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