

KVL Analysis with Spice

"Spice" or its derivatives (ngspice, Hspice, Pspice) are used to simulate the behavior of electrical circuits. Using a circuit simulator is a good way of confirming your intuition about a circuit or confirming a hand analysis. It should basically be used as *confirmation* or *optimization* tool. It should not be used as a design tool. In this class, ngspice will serve as an easy and quick way to check almost any homework problem you can think of. Think of it as the ultimate answer key. In figure 1 below shows the circuit we analyzed by hand earlier. We see that the steps of selecting a reference direction for the current I and element voltages have been done.

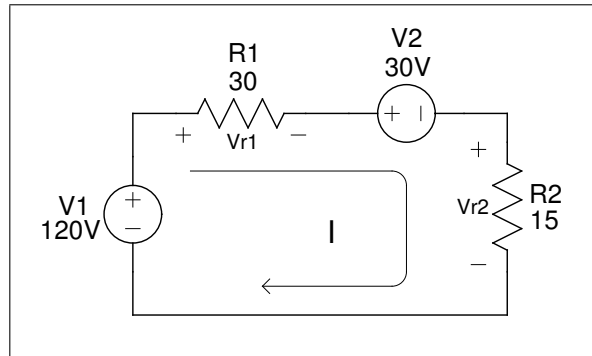


Figure 1: KVL Spice problem.

In Spice, circuits are described as "netlists". Netlists are a textual description of how the elements in the circuit are connected. We describe the connection of the elements by telling which node each terminal of an element is connected to. We must mark all the nodes in the circuit with unique node names. These are shown below as the letters A, B and C. The ground node is signified with the ground symbol. Note that all Spice netlists must have a ground node in the circuit. Spice will accept the name "gnd" or the number "0" (zero) as ground. The other node names are circled for clarity.

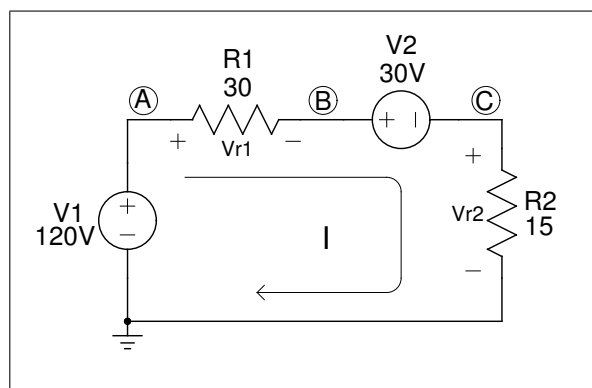


Figure 2: Convert to netlist.

Each element in the netlist must be distinct from the others. Therefore, we need to distinguish the two voltage sources with reference designators. For this circuit, the designators are "v1" and "v2".

Note that r1 and r2 are already marked. The new annotated schematic is shown below. Now we can write the netlist. Note that for the most part, spice is case insensitive. The exception is when specifying unit magnitudes.

The Spice netlist for the circuit above is placed in a text file with your choice of editor. It looks like this:

Listing 1: Spice file for KVL problem

```
.title class example problem
***** netlist follows *****
v1      a      gnd      120
r1      a      b        30
r2      c      gnd      15
v2      b      c        30
***** netlist done *****
.control
  set numdgt=2
  op
  echo Node voltages:
  print line v(a) v(b) v(c)
  echo
  show r1
  quit
.endc
.end
```

A description of the spice file above follows. The first line is always the title line. With or without the `.title`, the first line is still the title. Following that comes the netlist, the part of the file that describes the elements and their connection. The body of the netlist is shown below. It is the exact description of the circuit. Note that this netlist has been annotated with extra text to show the elements of the listing and would not normally be included. Note that the currents through the elements in the netlist are implied by the positive and negative terminal definitions.

Listing 2: Netlist body format

```
type of element and its reference designation
r = resistor
v = voltage source
i = current source
|
|           node which positive element terminal is connected
|           |
|           |           node which negative element terminal is connected
|           |           |
|           |           |           value of the element
|           |           |           |
v1          1           gnd          120
r1          1           2            30
r2          3           gnd          15
v2          2           3            30
```

Following the netlist comes the simulation directives. This section, bracketed by the `.control` and `.endc` commands, tells the simulator what to do. The `set numdgt=2` statement tells the simulator how many digits to display. The `echo` statement simply prints out the text string that follows it. The statement `print line` causes the simulator to print the voltages at nodes a, b and c. The statement `show r1` makes the simulator print all its information about r1. Finally, the `quit` command stops the simulator and control returns to the invoking terminal. The mandatory `.end` statement indicates the end of a Spice file. Comments follow the `$`, `;` or `*` delimiters.

If we name this file `kv1.sp`, `ngspice` is invoked on the file at the prompt by typing:

```
ngspice kv1.sp > output
```

The results from the simulation are redirected via the `>` character into in the file *output* as seen below.

Listing 3: Contents of file output

```
Circuit: class example problem

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

No. of Data Rows : 1
node voltages:
v(1) = 1.20e+02
v(2) = 6.00e+01
v(3) = 3.00e+01

Resistor: Simple linear resistor
  device      r1
  model       R
  resistance   30
  ac          30
  dtemp       0
  noisy       1
  i           2
  p           120

ngspice-2lplus done
```

We see that the loop current is identical to the hand calculated value of 2 Amps.