Introducing the EMC Newsletter

Rodger Richey
Senior Applications Manager

Welcome to the first issue of the EMC Newsletter created by the Application Engineers at Microchip Technology. This newsletter will focus on ideas and design tips to improve Electromagnetic Compatibility or EMC when using our products. Each issue, published every other month, will have a major theme, two to three articles supporting that theme, definitions of some commonly used EMC terms, and a tip or a trick. We hope to convey the best practices that we have found to improve EMC performance.

As application engineers, we usually get involved with customer issues at the end of the design cycle after a lot of time and resources have been dedicated to a project. Many of the solutions require layout or component changes. These changes are very costly to implement at this point in the design cycle. Therefore, this is the goal of the EMC Newsletter: to communicate techniques to improve EMC performance and lower development costs based on real-world examples, before the start of the design cycle.

Issue #1 is an introduction into EMC, specifically Electrostatic Discharge (ESD), Electrical Fast Transient (EFT) and Latch-up. Looking ahead, Issue #2 will cover PCB layout including articles on ground planes, component placement and layout for high-speed digital signals. Future issues will cover EFT and ESD/ Latch-up in depth, circuit design and more layout techniques.

If you have ideas for an article or wish to see an article on a specific topic, or have any comments regarding this newletter and its contents, please send an email to EMC@microchip.com.

What is EMC?

Rodger Richey
Senior Applications Manager

Electromagnetic Compatibility (EMC) is the ability of a system to operate in its environment without disturbing anything else in that environment, including itself. A system is said to be electromagnetically compatible if:

1. It does not cause interference with other systems;
2. It is not susceptible to emissions from other systems, and
3. It does not cause interference with itself.

Interference can be broken up into one of four categories: radiated emissions, radiated susceptibility, conducted emissions and conducted susceptibility. The term *radiated* (when used in the context of EMC) means the propagation of electromagnetic waves through the air. The term *conducted* means the propagation of electromagnetic waves through a physical medium such as a cable between two systems. *Emission* means to produce electromagnetic waves and propagate them either through the air (radiate) or through a physical medium such as a cable (conduct). *Susceptibility* is a sensitivity to electromagnetic waves received through the air (radiated) or through a cable (conducted).

The key to success in solving EMC issues with a system is to first understand which of the four basic groups the interference falls under. Once that is determined, the designer can then suppress the emission at its source, reduce the efficiency of the coupling path (air or cables), or make the system less susceptible to the emission. In most cases, the designer has no control over the emission source and must rely on techniques to make the path inefficient or make the system less susceptible.

In This Issue

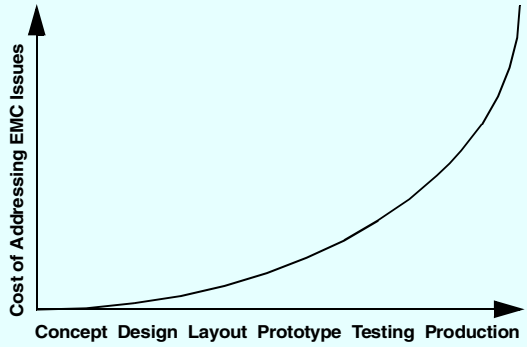
Recommended Reading

Introduction to Electromagnetic Compatibility
by Clayton R. Paul, ISBN 0-471-54927-4

This book deals with the topic of interference (electromagnetic compatibility) in electronic systems. It builds on basic undergraduate electrical engineering concepts and principles and applies them to the design of electronic systems that operate compatibly with other electronic systems and do not create interference phenomena.

Tips and Tricks

It is far cheaper to address EMC at the beginning of a design rather than waiting after conformance testing. To provide effective EMC solutions, you must first understand the environment the application will be operating in.



What is ESD?

Gaurang Kavaiya
Microcontroller Systems Group Manager

Electrostatic Discharge (ESD) is probably the most familiar EMC term. However, familiarity is often limited to the term, with most people not knowing much beyond that. This article will give some insight into this subject.

The word *electrostatic* indicates static electricity. In science class you may have done some experiments with static electricity. For example, if you rub a glass rod with a silk cloth or if you rub a piece of amber with wool, the glass and amber will develop a static charge that can attract small bits of paper or plastic. If you connect this glass rod to some earthen metal object then the accumulated charge will be discharged. This is called Electrostatic Discharge or ESD. The electrical spark and shock you sometimes experience when you touch a metal shelf in a store is another example.

You may wonder why you don't see sparks or feel an electrical shock every time you touch a metal object. This is because the amount of charge is dependent on the materials involved and the environment. See Figure 1 and Table 1 for examples. For practical purposes, ESD is mostly associated with human interaction. If any system is subject to human interaction then an ESD event could occur. It is possible that a machine can also generate an ESD event. However, its scope is limited compared to that of human interaction.

FIGURE 1: MAX VALUE OF ESD VOLTAGES

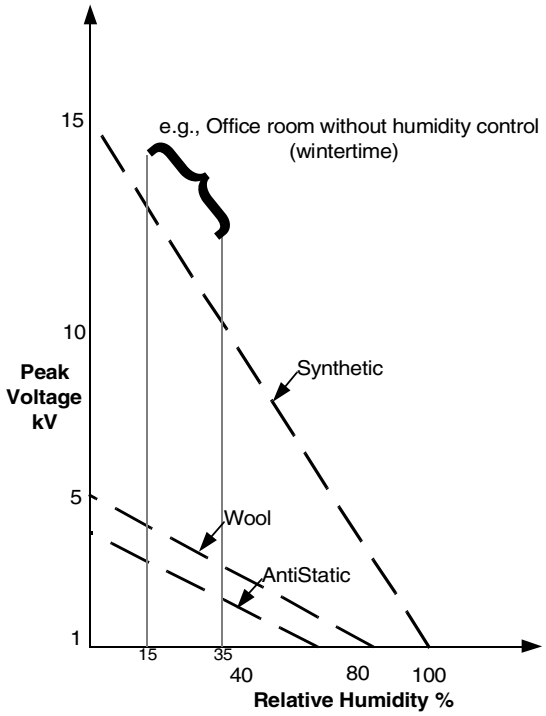


TABLE 1: COMMON STATIC VOLTAGES

Static Voltages as a Function of Relative Humidity (RH)	20% RH (kV)	80% RH (kV)
Walking across a vinyl floor	12	0.25
Walking across a synthetic carpet	35	1.5
Arising from a foam cushion	18	1.5
Picking up a polyethylene bag	20	0.6
Sliding a styrene box on a carpet	18	1.5
Removing mylar tape from a PC board	12	1.5
Shrinkable film on a PC board	16	3.0
Triggering a vacuum solder remover	8	1.0
Aerosol circuit freeze spray	15	5.0

ESD is a context-sensitive subject. The effect, testing and solution depend on the environment. If we look at embedded systems then we are mainly looking at semiconductor, system manufacturing, and an end-user perspective.

First, let's talk about the semiconductor perspective. Microchip Technology Inc. is a semiconductor manufacturer so, we'll also look at the Microchip perspective. A semiconductor device goes through lots of human interaction before it is mounted onto a board. It is possible that a device may be subjected to an ESD event during this period. Almost all CMOS devices tend to have protection circuitry to avoid damage in this condition. As a part of the quality process, all Microchip devices are tested against two JEDEC standards. They are:

- JESD22-A114B for Human Body Model (HBM)
- JESD22-A115A for Machine Model (MM).

For more information, please refer to the *Microchip Overview, Quality Systems And Customer Interface Systems Handbook* (DS00169), available in Adobe® PDF format from the Microchip web site. The human body model uses a waveform similar to ESD by human interaction. Typically, the machine model limits are one-tenth of HBM. It is believed that human interaction can generate only one pulse as it takes time for them to accumulate charge. A machine can generate multiple pulses so the peak amplitude is low to keep energy the same (model does not use a series resistor; therefore, pulses depend on the resonance of the system). Please note that devices are **not biased (not powered)** during this testing. This test verifies the ESD behavior of a device when a human handles it, for example, when you touch a device without wearing an anti-static wristband.

Second is the system manufacturer perspective. Here we're mainly dealing with anti-static workstations, wristbands and grounded equipment. This is mostly driven by the quality systems of that industry.

Third and last is the end-user perspective. Most systems require human interaction which can generate an ESD event on the exterior of the system. For example, when you operate your microwave oven you may generate an ESD event. In this case, the ESD event is generated on the exterior surface of the system/equipment. The ESD sensitive object may see different ESD events based on the assembly and leakage/conductivity path in the system. Therefore, this approach differs from the semiconductor perspective in testing. In the case of the semiconductor perspective, testing is performed on individual components, whereas addressing the end-user perspective, one needs to test final assembly. One of the popular standards that addresses system level testing is International Electrotechnical Commission (IEC) 61000-4-2[(1)]. This standard defines test waveform, levels, set up, procedure and also the requirements for test equipment.

IEC 61000-4-2

Figure 2 shows an ESD test waveform while Table 2 shows some important parameters associated with it. Did you notice the two most important characteristic of the waveform? The first one is rise time; it's extremely fast (0.7 to 1 nS). This results in a spectrum of 1 GHz. Therefore, many fixes require the mind set of an RF designer rather than the embedded designer. The second important parameter is peak current. For Level 4, the peak current is as high as 30 Ampere.

FIGURE 2: ESD TEST WAVEFORM

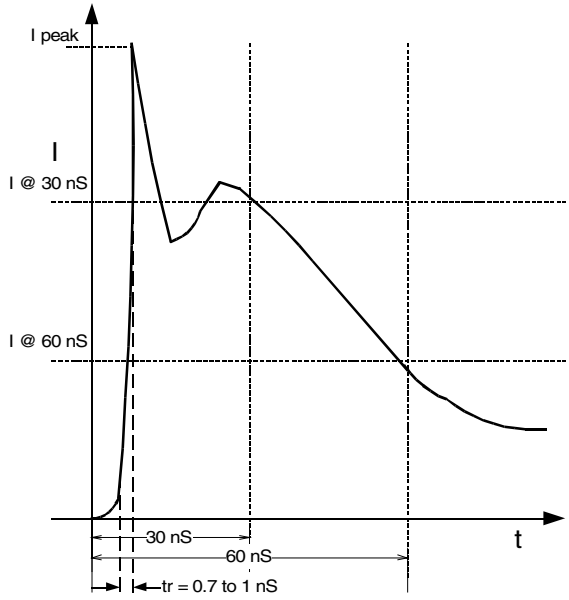


TABLE 2: WAVEFORM PARAMETERS

Level	Voltage (kV)	Rise time tr (ns)	Ipeak (A)	I @ 30 nS (A)	I @ 60 nS (A)
1	2	0.7 to 1	7.5	4	2
2	4	0.7 to 1	15	8	4
3	6	0.7 to 1	22.5	12	6
4	8	0.7 to 1	30	16	8

Table 3 shows the peak voltage for various test levels of contact discharge and air discharge. In the case of a contact discharge test, a sharp point tip is used with an ESD gun. The charge is directly discharged to Equipment Under Test (EUT) through direct contact. In the case of an air discharge test, a round tip is used with an ESD gun. The charge is transferred through the air to EUT.

TABLE 3: DISCHARGE METHOD VERSUS TEST LEVELS

Level	Contact Discharge	Air Discharge
	Test Voltage (kV)	**Test Voltage (kV)**
1	2	2
2	4	4
3	6	8
4	8	15
X	Open	Open

ESD system testing is common across a wide range of industries such as automotive, appliance, consumer, industrial and so on. Typically, many customers try to achieve Level 4 or higher compliance. Many customers check for 15 kV contact discharge and look for user noticeable operational differences. This IEC standard test is done on end systems on the exterior of the system (i.e., door of a refrigerator). The extremely fast rise-time and very high peak current makes it a tough noise to handle. The best way to handle the ESD issue is to identify the first point of contact and control potential damaging effects by limiting current. Another important fix is to use low inductance ground to avoid a huge ground bounce. The primary goal is to keep energy away from sensitive circuitry in the system.

[(1)]International Electrotechnical Commission. 2001. IEC 61000-4-2, *Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test.* ISBN 2-8318-5687-6

What is EFT?

Gaurang Kavaiya
Microcontroller Systems Group Manager

How many times have you overheard discussions on EFT testing? You may be wondering what it is? Why do we need it, and how they do it? This article will try to address these basic questions.

First let's clarify the acronym; we aren't talking about Electronic Funds Transfer. EFT stands for Electrical Fast Transients. As the name suggests, it is one kind of noise signal that is fast in nature. By definition it is, "a burst of interference pulses that simulates inductively loaded switches". Sounds complicated!

Let's look at a simple example of a power drill. The electrical motor in most simple power drills is an inductive load. When you run your power drill it generates lots of noise on power lines. Any other equipment on the same power line will be subject to that noise. If you have your freezer in your garage, you wouldn't want it to be affected when you run your drill. Would you keep a freezer if its compressor randomly starts switching or acts strangely when you turn on your drill? If your answer is no, then that's the reason why appliance manufacturers care about EFT. The appliance industry is not the only industry that cares about EFT. The industrial environment is even worse than a home environment. Therefore, you will find many manufacturers concerned about EFT behavior.

So the next question is: what should you test? You can't use a power drill from XYZ manufacture to test equipment. You definitely need a more defined/controlled setup.

The International Electrotechnical Commission (IEC) has defined a system level standard, IEC 61000-4-4[(1)] to address this issue. This standard defines test waveform, levels, set up, procedure and also the requirement for test equipment. Figure 1 shows a test waveform, while Table 1 shows some important parameters of the test waveform for different test levels. The signal can have either positive or negative polarity and it's asynchronous to the power supply. It can be coupled on Line, Neutral or Power Earth or a combination of all three. The normal practice is to couple noise on power lines; however, the IEC standard does specify a mechanism to couple noise on I/O and communication ports. The IEC-compatible EFT generator provides all these options.

FIGURE 1: EFT WAVEFORM

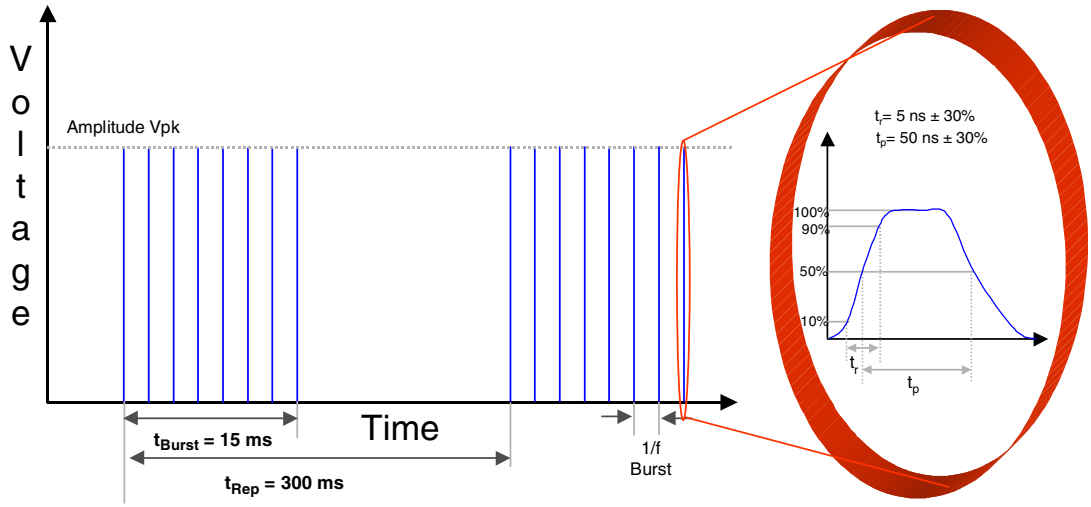


TABLE 1: WAVEFORM TEST PARAMETERS

Level	Power Supply Ports		I/O Signal, Data and Control Ports	
	Vpk kV	Burst Freq kHZ	Vpk kV	Burst Freq kHZ
1	0.5	5	0.25	5
2	1	5	0.5	5
3	2	5	1	5
4	4	2.5	2	5
X	Open	Open	Open	Open

Typically most customers try to achieve level 3 or level 4 compliance. The fast rise-time (5 nS) and amplitude (up to 4000V) of transients makes it troublesome for electronic circuits. Typically, transformerless power supply and Switch Mode Power Supply (SMPS)-based systems face more EFT issues compared to iron core transformer-based systems. Most EFT issues are addressed by using line filters, transient protectors, isolation transformers, voltage regulators and an isolated high-power circuit.

[(1)]International Electrotechnical Commission. 2001. IEC 61000-4-4, *Electromagnetic compatibility (EMC) – Part 4-4: Testing and measurement techniques – Electrical fast transient/burst immunity test.* ISBN 2-8318-5854-2

What is Latch-up?

Ruan Lourens
Principal Applications Engineer

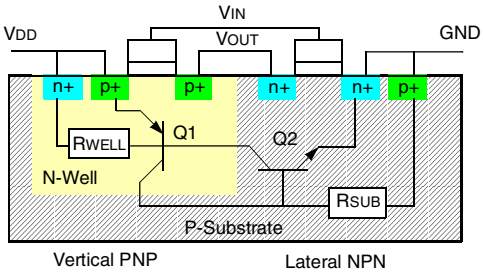
Introduction

Many engineers have run into latch-up problems when working with CMOS devices such as discrete logic or microcontrollers. Latch-up is normally experienced in high noise environments and typically leads to some sort of catastrophic failure. The device, when subjected to out-of-specification transients, collapses V_{DD} to V_{SS}. What is meant by this is that the part seems to pull V_{DD} down to ground thus causing excessive current to flow into the part. Depending on the application, this can either lead to damage to the device itself or to the supply if it is not current limited. The latch-up condition can be cleared by either turning the power completely off or reducing the latch-up current to a low enough value to clear the condition. The minimum holding current to maintain a latch-up event differs between CMOS processes, and can be anywhere from 3 mA to 50 mA or more.

Latch-up in CMOS

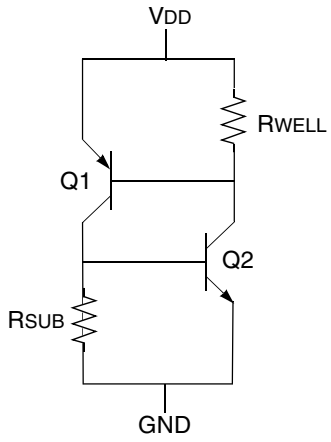
All CMOS logic devices will latch-up when exposed to a strong enough voltage transient on either an input pin or a supply pin. Before addressing possible preventative measures to latch-up let's first explain how it happens. A cross section of a CMOS logic inverter is shown in Figure 1. It also shows the pair of parasitic bipolar (BJT) transistors that are formed.

FIGURE 1: CROSS SECTIONAL VIEW OF AN INVERTER



The equivalent circuit that is formed by the parasitic BJTs is shown in Figure 2, the transistors thus form a parasitic Silicon Controlled Rectifier (SCR). An SCR turns on when triggered, and stays on until the current flow is reduced to a value below the minimum holding current. Triggering can happen when sufficient current is forced to flow through either the N-well or substrate impedance to cause a voltage drop of about 0.6 volts or greater with the appropriate polarity. The triggered SCR or latch-up condition thus forms a self-sustaining low impedance path between V_{DD} and ground.

FIGURE 2: EQUIVALENT CIRCUIT



Increasing Latch-up Immunity

The device manufacturer can control latch-up immunity to some extent, but it will increase the cost of the device if high levels of latch-up immunity are required. For most applications, latch-up immunity improvements are most cost effective when addressed from a board/system design perspective. Detailed solutions are beyond the scope of this article but here are a few guidelines.

Power Supply Noise Control

- Use transient voltage suppressors (TVS) that are essentially high energy and speed Zener diodes to reduce over voltage conditions
- Use ceramic decoupling caps close to the supply pins; when in doubt add more….
- Use parallel decoupling caps that cover a range of values; choose the size of the decoupling caps about 2 or 3 decades apart
- Use proper power distribution techniques, have separate high power, analog and digital power paths and use double passive π filters for low-power sections
- Where possible place a resistor in series with the supply that is large enough to clear a latch-up event by limiting the latch-up current to a value less than the minimum holding current.

Other Considerations

- Use high frequency printed circuit board techniques; look into common mode chokes, current return paths, radiation, etc.
- Treat every trace as an RF antenna
- Increase the impedance connected to I/O pins as far as possible
- Use passive filters to suppress transients in signals that connect high-power sections with sensitive low-power sections.

Conclusion

CMOS devices are capable of latching-up, but the circuit designer can increase the system's latch-up immunity by using inexpensive voltage suppressors, passive filters and proper layout techniques. Not only will these efforts improve immunity to latch-up but may also contribute to EMI/EMC compatibility.

NOTES:

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