EE6378 Power Management Circuits

Lecture 4: Voltage References

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Introduction

- Here, we will learn to build a reference voltage to provide a stable and accurate supply voltage. The ***voltage reference is an electronic circuit to provide an accurate and stable DC voltage that is very insensitive to the change in supply voltage and temperature***

- How accurate is a voltage reference? E.g. Weston cell is an electrochemical device which provides a reproducible voltage of 1.018636 V at 20^{o}C with a small temperature coefficient of 40 ppm/^{o}C. For integrated circuit implementation, active solid-state devices can achieve a tempco of 1-4 ppm/^{o}C if appropriate compensation technique is employed

- Note
  - ***To minimize error due to self-heating, voltage reference usually operates with modest current (e.g. < 1mA)***
  - ***Tempco = temperature coefficient, usually expressed in ppm/^{o}C (parts per million/^{o}C or 10^{-6}/^{o}C***

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Overview

- Performance Requirements
- Zener Diode Voltage Reference
- Bandgap Voltage References
- Bandgap Voltage References Implemented in CMOS technologies

Performance Parameters (1)

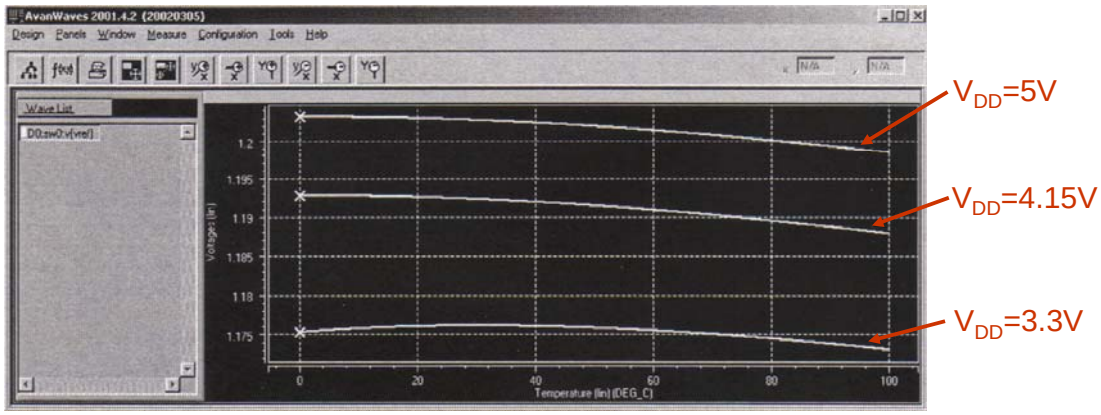
The primary requirements of a voltage reference are accuracy and stability. Some qualitative parameters are:

- Load Regulation = $\Delta V_o/\Delta I_o$ (usually expressed in mV/mA or mV/A) or
  Load Regulation = $100(\Delta V_o/\Delta I_o)$ (in %/mA or %/A)
- Line Regulation = $\Delta V_o/\Delta V_{in}$ (usually expressed in mV/V) or
  Line Regulation = $100(\Delta V_o/\Delta V_{in})$ (in %/V)
- Power Supply Rejection Ratio (PSRR) is a measure of the ripple in the reference voltage due to the ripples in the supply voltage

$$PSRR = 20\log_{10}\frac{V_{ri}}{V_{ro}} \quad \text{(in dB)}$$

Performance Parameters (2)

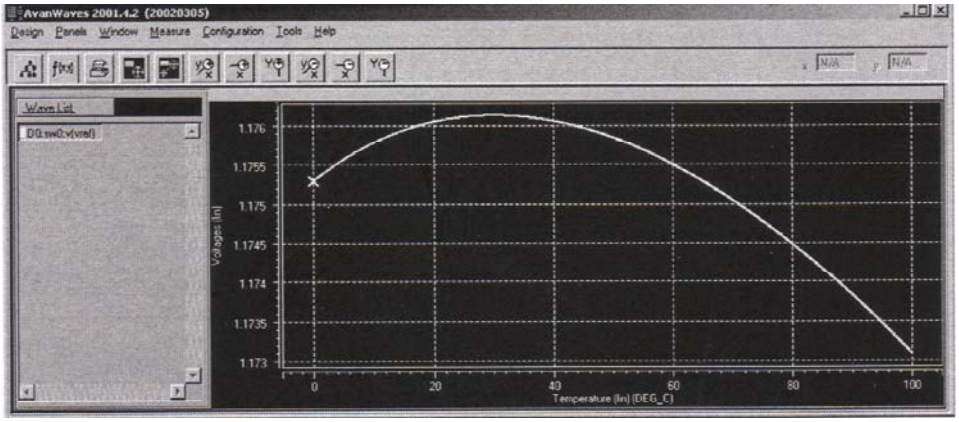
Example of line regulation / supply-voltage dependence at V_{DD} = 3.3, 4.15 and 5V (step size of 0.85V)



Line regulation at $T = 27^{o}C$ is

$$\frac{V_{ref}(V_{DD}=5V)-V_{ref}(V_{DD}=3.3V)}{5-3.3}=\frac{1.201-1.176}{5-3.3}=14.7mV/V$$

Performance Parameters (3)



The maximum ($V_{ref(max)}$) and minimum ($V_{ref(min)}$) reference voltages are 1.1761V and 1.1731V, respectively. The reference voltage at T = 27°C (V_{ref}) is 1.1761V. The tempco in ppm/°C can be found by

$$\text{Tempco}=\frac{V_{ref(\max)}-V_{ref(\min)}}{V_{ref}}\times\frac{10^6}{(T_{\max}-T_{\min})}=\frac{1.1761-1.1731}{1.1761}\times\frac{10^6}{(100-0)}=25.5ppm/^{O}C$$

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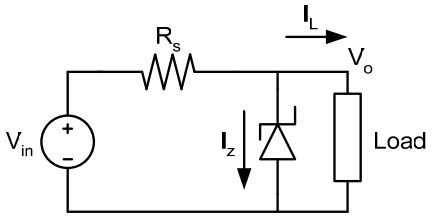
Review on Zener Diode Voltage Reference

- The Zener diode described in Lecture 2 can be considered as a voltage reference. Since the breakdown voltage due to Zener breakdown mechanism has a negative temperature coefficient, and the breakdown voltage due to the avalanche multiplication has a positive coefficient, the reference voltage is somewhat independent of the change of temperature

$$V_o = \frac{r_z}{R_s + r_z} V_{in} + \frac{R_s}{R_s + r_z} V_{ZK} - \frac{R_s r_z}{R_s + r_z} I_L$$

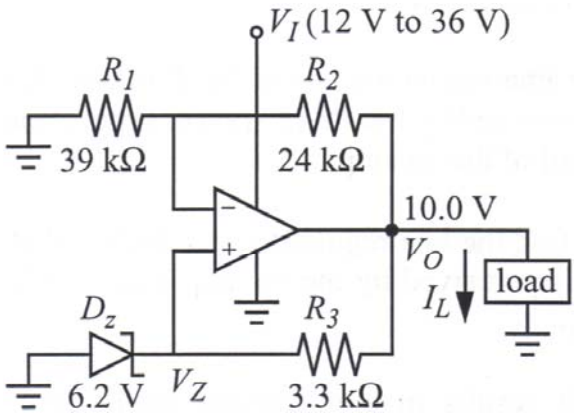


$$\text{Line Regulation} = \frac{\Delta V_o}{\Delta V_{in}} = \frac{r_z}{R_s + r_z}$$

$$\text{Load Regulation} = \frac{\Delta V_o}{\Delta I_L} = -\frac{R_s r_z}{R_s + r_z}$$

Improved Zener Diode Reference (1)

- In the case of Zener diode, the output voltage V_o heavily depends on the load current I_L, which in most cases are not good. It would be better if we could shield the V_z from the influence of the load. This can be done with the help of an op amp as shown below. This method refers to self regulation which shifts the burden of line and load regulations from the diode to the op amp



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Improved Zener Diode Reference (2)

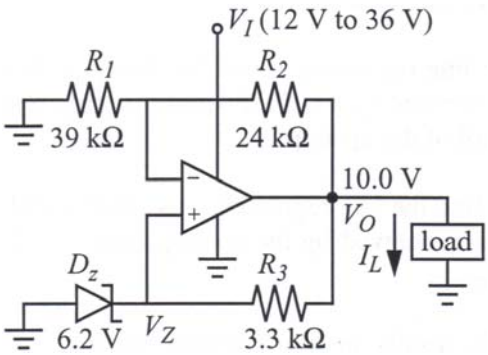
- By inspection,

$$V_o = (1+\frac{R_2}{R_1})V_z = (1+\frac{24k}{39k})6.2 = 10V.$$

- The output voltage is also adjustable via R_2
- The load current I_L is supplied from the opamp such that the current flowing through the Zener diode is almost constant at

$$I_z = \frac{V_o - V_z}{R_3} = \frac{10.0 - 6.2}{3.3k} = 1.15mA.$$

- Since the diode current is independent of the load current, the diode voltage is insensitive to the load
- R_3 can be raised to avoid unnecessary power wastage and self-heating effects



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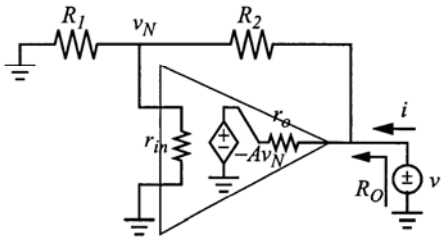
Load Regulation (1)

- The load regulation is directly related to the output impedance. To find R_o, we suppress the input source V_z and apply the test-voltage technique. By voltage divider formula:

$$v_N = \frac{R_1 // r_{in}}{R_1 // r_{in} + R_2} v$$



- Summing currents at the output node

$$i + \frac{v_N - v}{R_2} + \frac{-Av_N - v}{r_o} = 0$$

- Eliminating v_N and solving for the R_o=v/I, we obtain

$$R_o = \frac{r_o}{1 + [(A + r_o / R_1 + r_o / r_{in}) / (1 + R_2 / R_1 + R_2 / r_{in})]}$$

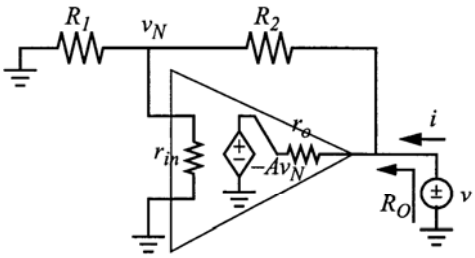
$$\approx \frac{r_o}{1 + Ab} \quad \text{where} \quad b = \frac{R_1}{R_1 + R_2}$$

Load Regulation (2)

- Typically r_{in} is in the MΩ range or greater, R_1 and R_2 are in kΩ range and r_o is on the order of 10^2 Ω. The terms r_o/R_1, r_o/r_{in}, and R_2/r_{in} can thus be ignored to yield $R_o \approx r_o/(1+Ab)$

- The load regulation $R_o \approx r_o/(1+Ab)$ which is much smaller than the Zener diode voltage reference without opamp

- Since r_o and A are frequency dependent, so are the load regulation. In general, load regulation tends to degrade with frequency



Thermal Stability (1)

- Thermal stability is one of the most demanding performance requirement of voltage references due to the fact that semiconductor components are strongly influenced by temperature
- The forward-bias voltage V_D and current I_D of a silicon pn junction, which forms the basis of the diodes and BJTs, are related as $V_D=V_T\ln(I_D/I_S)$, where V_T is the thermal voltage and I_S is the saturation current. Their expressions are

$$V_T = kT/q \qquad \text{and} \qquad I_S = BT^3 \exp(-V_{G0}/V_T)$$

where

k=1.381×10^{-23} is Boltzmann's constant

q=1.602 ×10^{-23} C is the electron charge

T is the absolute temperature

B is a proportionality constant

V_{G0} = 1.205V is the bandgap voltage for silicon

Thermal Stability (2)

- The temperature coefficient (TC) of the thermal voltage:

$$\text{TC}(V_T) = \frac{\partial V_T}{\partial T} = \frac{k}{q} = 0.0862\text{mV/}^{\text{o}}\text{C}$$

$$\text{TC}(V_D) = \frac{\partial V_T}{\partial T}\ln\left(\frac{I_D}{I_S}\right) + V_T\frac{\partial[\ln\frac{I_D}{I_S}]}{\partial T} = \frac{V_D}{T} - V_T\frac{\partial(3\ln T - \frac{V_{G0}}{V_T})}{\partial T} = -\left(\frac{V_{G0}-V_D}{T} + \frac{3k}{q}\right)$$

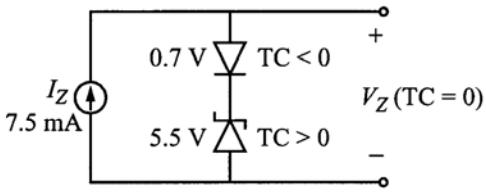
Assume V_D=650mV at 25$^{\text{o}}$C, we get TC(V_D) ≈ -2.1mV/$^{\text{o}}$C.

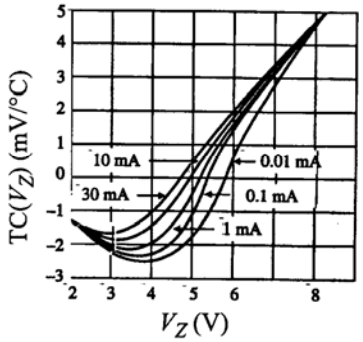
- TC(V_T) have a positive tempco and TC(V_D) have a negative tempco, so these two equations form the basis of two common approaches to thermal stabilization, namely, thermal compensated Zener diode references and bandgap references

Thermally Compensated Zener Diode Reference

- Idea of thermally compensated Zener diode is to connect a forward-biased diode in series with a Zener diode having an equal but opposing tempco as shown below

- Since TC(V_z) is a function of V_z and I_z. We can fine tune I_z to drive the tempco of the composite device to zero. In this case, a 7.5mA is used to give a reference voltage of V_z = 5.5+0.7 = 6.2V with tempco ranging from 100ppm/^{o}C to 5ppm/^{o}C





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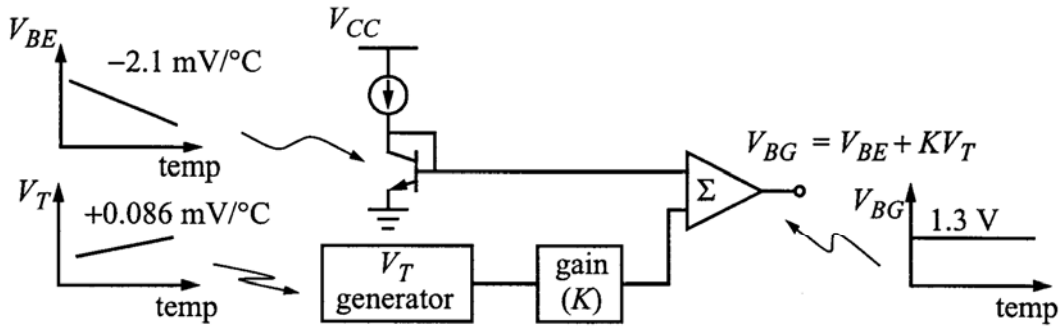
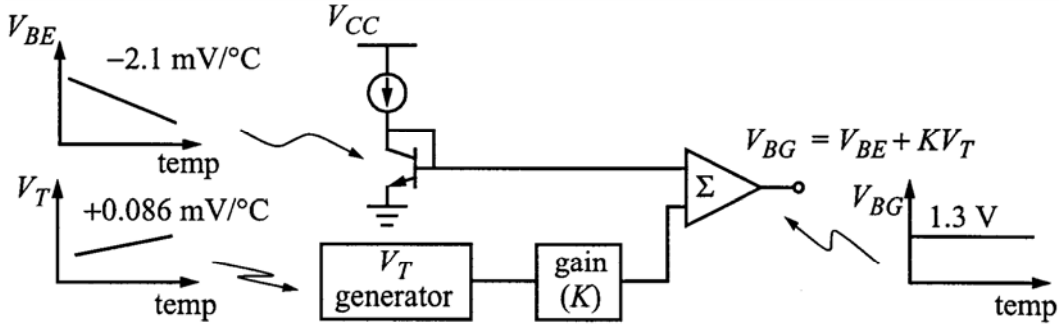
Bandgap Voltage Reference (1)

- Since the best breakdown voltages of the Zener diode references range from 6 to 7V, they usually require supply voltages on the order of 10V to operate. This can be a drawback in systems powered from lower supplies, such as 5V. This limitation is overcome by bandgap voltage references, so called because their output is determined primarily by the bandgap voltage of silicon V_{G0} = 1.205V



Bandgap Voltage Reference (2)



- Addition of the voltage drop V_{BE} of a base-emitter junction, which has a negative tempco, to a voltage proportional to the thermal voltage V_T, which has a positive tempco, to generate a reference voltage, which is independent of temperature

- As TC(V_{BE}) ≈ -2.1mV/°C and TC(V_T) = 0.0086mV/°C, then zero tempco is achieved at a particular temperature (e.g. T=300K):

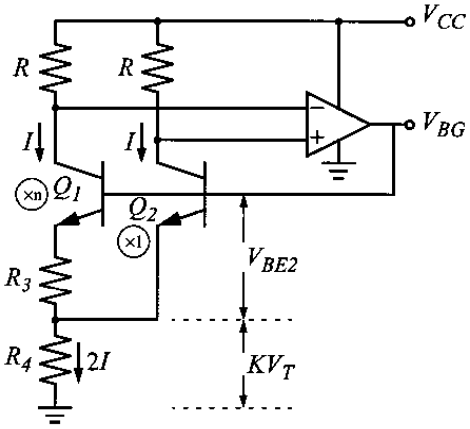
$$V_{BG} = V_{BE} + KV_T$$
$$\text{i.e. } TC(V_{BG})\big|_{300K} = TC(V_{BE}) + K \cdot TC(V_T) = 0$$
$$\Rightarrow K = \frac{-TC(V_{BE})}{TC(V_T)} = \frac{2.1}{0.086} = 24.4$$

- If for a particular transistor with certain bias current such that V_{BE} = 650mV, then

$$V_{BG} = V_{BE} + KV_T = 0.65 + 24.4(0.0259) = 1.28\ \text{V}.$$

- Note that $V_T = kT/q \propto T$, i.e. V_T is proportional to absolute temperature. We call V_T a Proportional To Absolute Temperature voltage, or in short, PTAT voltage

- From the figure, the emitter area of Q1 is n times as large as the emitter area of Q2, then $I_{s1}/I_{s2} = n$
- By op amp action with identical collector resistances, the collector currents are also identical, i.e. $I_{C1} = I_{C2}$. Ignore the base currents, we have $KV_T = R_4(I_{C1}+I_{C2}) = 2R_4I$



$$IR_3 = V_{BE2} - V_{BE1} = V_T \ln\left(\frac{I_{C2}I_{S1}}{I_{C1}I_{S1}}\right) = V_T \ln(n)$$

Combine two equations give

$$K = \frac{2R_4}{V_T}\frac{V_T}{R_3} = 2\frac{R_4}{R_3}\ln(n)$$

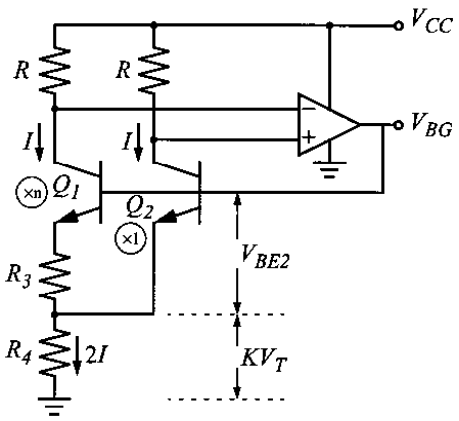
$$\Rightarrow V_{BG} = V_{BE2} + KV_T = V_{BE2} + (2\frac{R_4}{R_3}\ln n)V_T$$

Bandgap Voltage Reference Circuit (2)

- From the previous discussion, for a zero tempco voltage reference V_{BG}, K ≈ 24, with n = 4, then

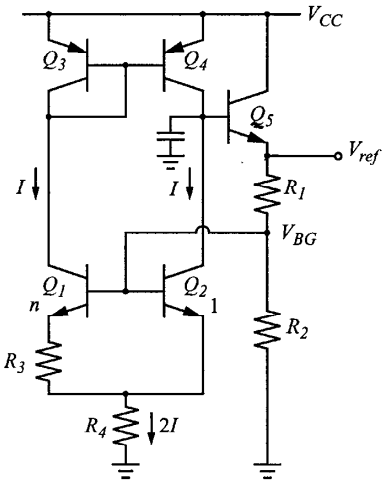
$$\frac{R_4}{R_3} = \frac{K}{2\ln 2} = \frac{24.4}{2\ln 4} \approx 8.8$$

- Note that $I = V_T \ln(n)/R_3 \propto V_T$, I is a PTAT current



Brokaw Cell

- Brokaw cell is commonly used bandgap-cell realization circuit and is shown in the figure
- The function of op amp is replaced by Q_3, Q_4 and Q_5. Q_3 and Q_4 form a current mirror to enforce the collector currents of Q_1 and Q_2 are identical
- The emitter follower Q_5 raises the reference voltage to $V_{ref} = (1+R_1/R_2)V_{BG}$



Stability of a Bandgap Reference

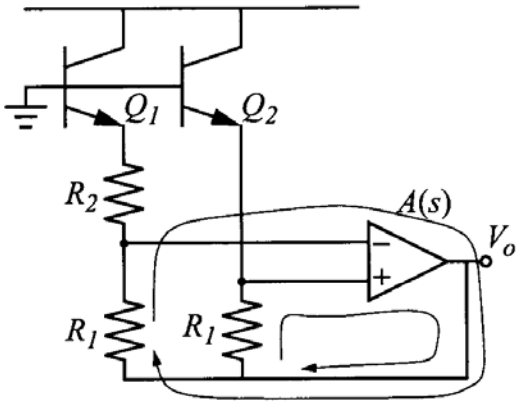
- In a bandgap reference, there exists 2 feedback loops, 1 positive loop and 1 negative loop.
- For the negative loop (the outer loop),

$$\text{Negative Loop Gain} = \frac{R_2 + 1/g_{m1}}{R_1 + R_2 + 1/g_{m1}} A(s)$$

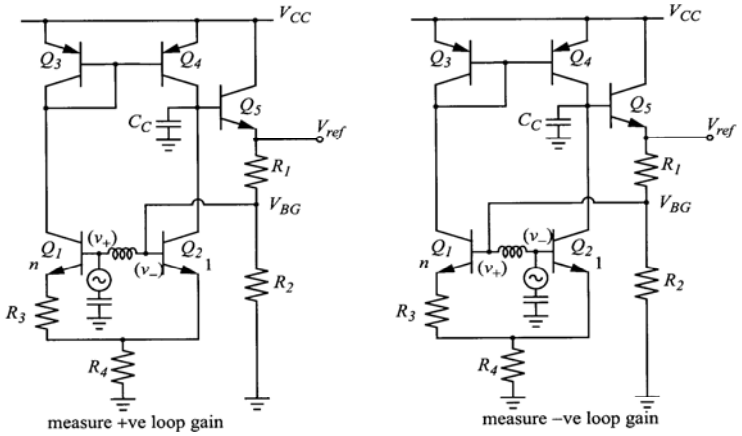
- For the positive loop (the inner loop),

$$\text{Positive Loop Gain} = \frac{1/g_{m1}}{R_1 + 1/g_{m1}} A(s)$$

- For stability, we must have a negative loop gain magnitude > positive loop gain magnitude. This is true as ((a+c)/(b+c))>(a/b) for b>a

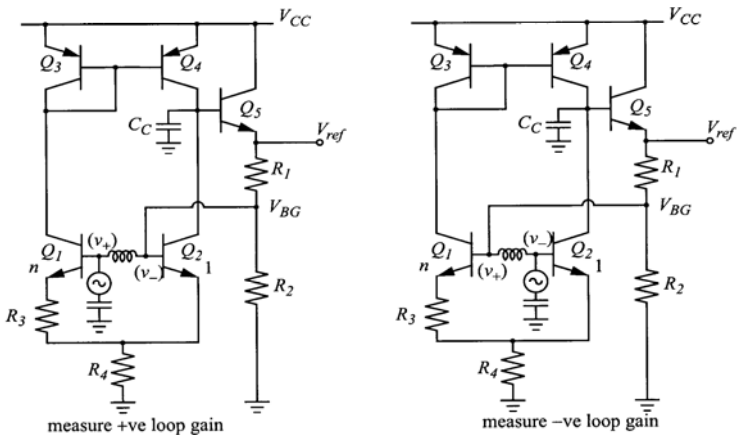


Stability of Simple Brokaw Cell (1)



- If we neglect R_3, then clearly Q1 and Q2 form a differential pair with positive and negative terminals tied together
- Above is the way to break the loop for measuring loop gain. The circuit should have a DC closed loop and AC open loop. The DC closed loop is for biasing and the AC loop is to measure loop gain

Stability of Simple Brokaw Cell (2)



- With the presence of R_3, the positive loop looks like an amplifier with degenerated emitter $\Rightarrow$ the gain is smaller than that with R_3. Therefore, negative loop gain magnitude > positive loop gain magnitude, i.e. stability requirement is satisfied
- C_c is the compensation capacitor. Here, dominant pole compensation is employed

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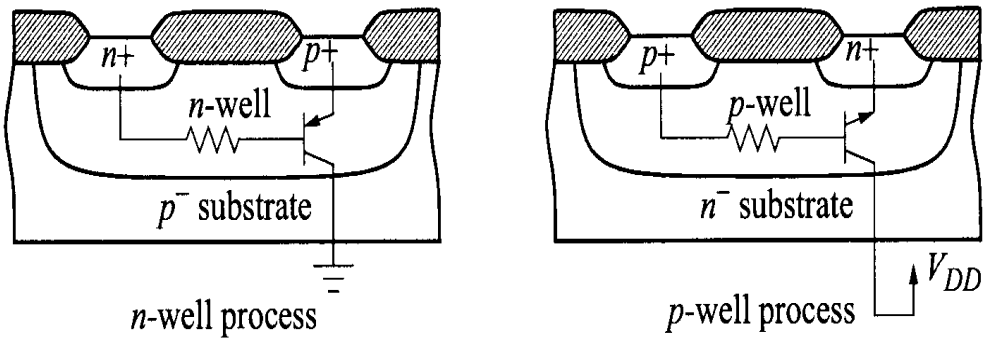
CMOS Bandgap References (1)

- CMOS is the dominant technology for both digital and analog circuit design nowadays
- Independent bipolar transistors are not available in CMOS technology
- CMOS voltage reference, however, can be achieved by making use of the concept of voltage reference. These CMOS circuits rely on using ***well transistors***. These devices are ***vertical bipolar transistors that use wells as their bases and the substrate as their collectors***

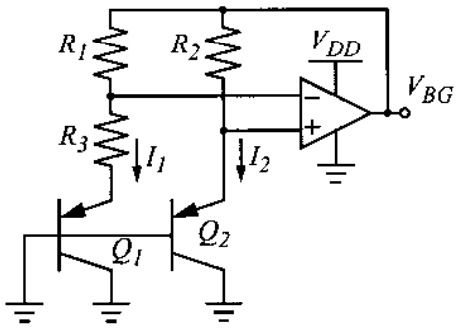
CMOS Bandgap References (2)



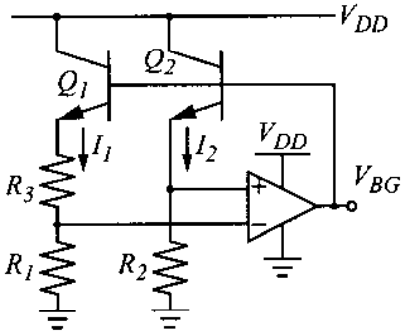
- These vertical bipolar well transistors have reasonable current gain (≈ 25), but very high series base resistance (≈ 1kΩ/□) due to the fact that the base contact is far away from the base
- The maximum collector current is thus limited to less than 0.1mA to minimize errors due to the base resistance

CMOS Bandgap References (3)

Two possible implementations:



n-well CMOS process



p-well CMOS process

- For example, in the n-well CMOS implementation, what is V_{BG} of the reference circuit?

CMOS Bandgap References (4)

$$V_{BG} = V_{EB2} + V_{R2}$$

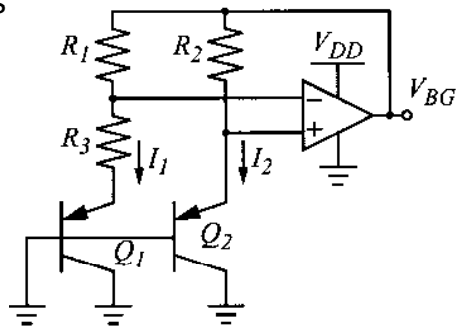
- Assume the op amp has very large gain and very small input currents such that its input terminals are at the same voltage, then

$$V_{R3} = V_{EB2} - V_{EB1} = \Delta V_{EB}$$

- Since the current through R_1 is the same as in R_3

$$\frac{V_{R1}}{R_1} = \frac{V_{R3}}{R_3} \quad \text{or} \quad V_{R1} = \frac{R_1}{R_3} V_{R3} = \frac{R_1}{R_3} \Delta V_{EB}$$

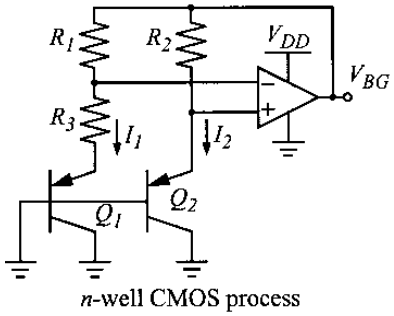
$$V_{BG} = V_{EB2} + \frac{R_1}{R_3} \Delta V_{EB}$$



n-well CMOS process

CMOS Voltage References (5)

- In CMOS realization, the bipolar transistors are often taken the same size, and different current densities (I_C/I_S) are realized by taking R_1 greater than R_2, which causes I_2 to be greater than I_1:



n-well CMOS process

$$V_{R1} = V_{R2} \Rightarrow I_1 R_1 = I_2 R_2 \quad \text{or} \quad \frac{I_2}{I_1} = \frac{R_1}{R_2}$$

$$\Delta V_{EB} = V_{EB2} - V_{EB1} = \frac{kT}{q}\ln\left(\frac{I_2}{I_1}\right)$$

$$\Rightarrow V_{BG} = V_{EB2} + \frac{R_1}{R_3}\frac{kT}{q}\ln\left(\frac{R_1}{R_2}\right) \quad \text{with} \quad K = \frac{R_1}{R_3}\ln\left(\frac{R_1}{R_2}\right)$$

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Example

- Find the resistances of a bandgap voltage reference based on the CMOS n-well process where $I_1 = 5\mu A$, $I_2 = 40\mu A$ and $V_{EB} = 0.65V$ at T = 300K. Assume $V_{BG} = 1.24V$
- Ans. $R_1 = 118k\Omega$, $R_2 = 14.8k\Omega$ and $R_3 = 10.1k\Omega$

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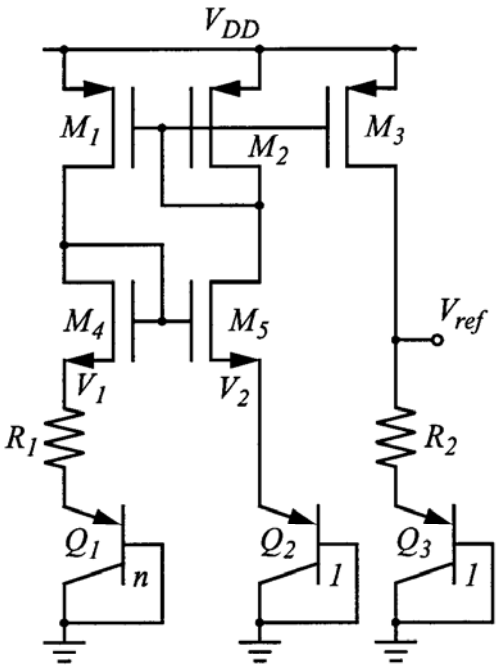
Other CMOS References

- Current mirror enforces equal currents at M1, M2 and M3
- Voltage clamping by M4 and M5 to enforce V1=V2
- PTAT loop formed by Q1, Q2 and R1

$$I = V_T \ln(N)/R_1$$

$$V_{ref} = V_{EB3} + \frac{R_2}{R_1}\ln(N)\cdot V_T$$

- Cascode current mirror or other forms for better current matching at different supply voltages



(a) simple current mirror

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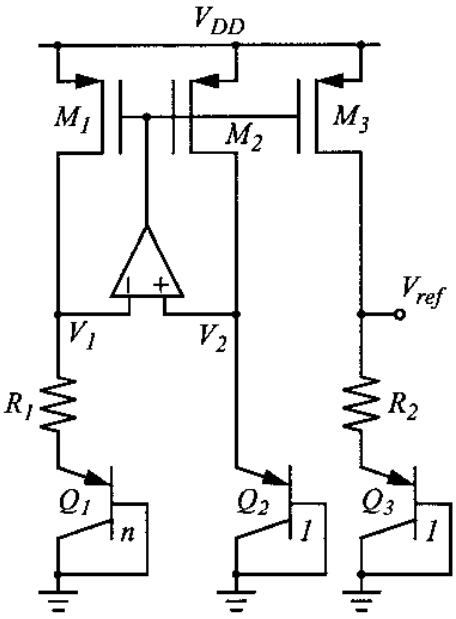
Current Mirror with Op Amp

- In CMOS reference using current mirror with op amp, an op amp is used to enforce the drain voltage of M_1 the same as of M_2. This allows a better current matching of drain currents of M_1 and M_2



(b) current mirror with op amp

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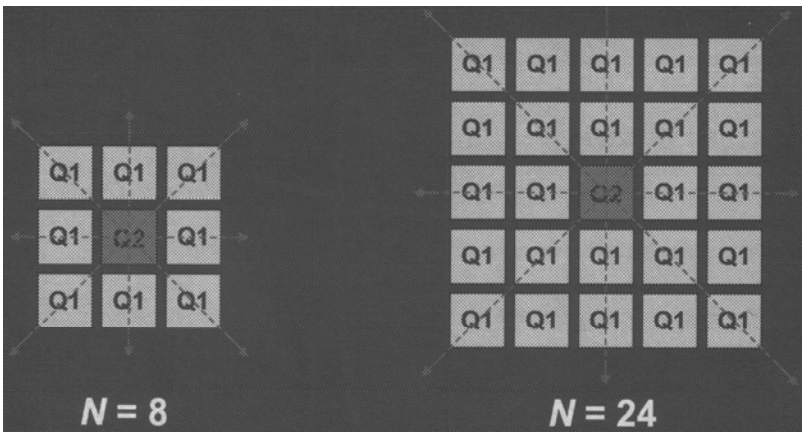
Error Sources in Voltage-Reference Design

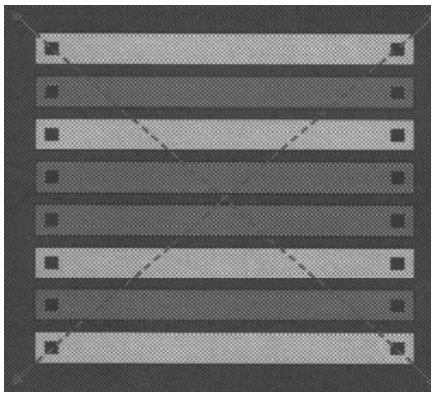
- Current mirror
- Voltage-clamping circuit
- BJT emitter area ratio (BJT matching)
- Resistor ratio (resistor matching)
- Base current
- Base resistance
- Systematic offset at different supply voltages
- Random offset of devices
- Temperature gradient within a chip

Design Considerations: BJTs

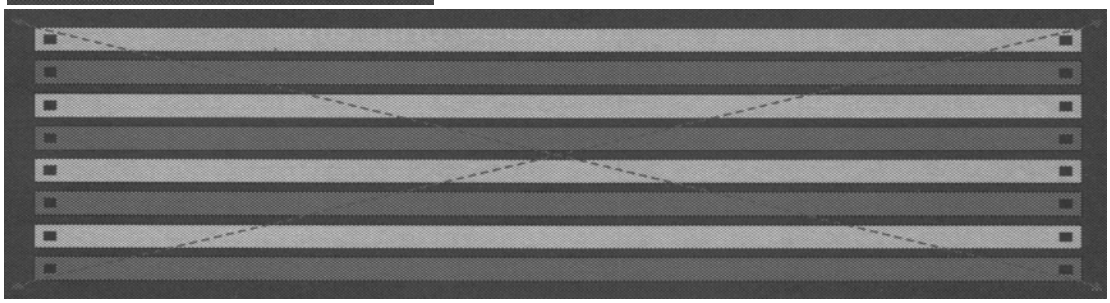


- Closely packed common-centroid layout
- Large N does not provide significant change due to the logarithm relation
- Generally, N=8 is chosen based on chip area consideration

Design Considerations: Resistors



- Matching is important to obtain an accurate resistance ratio
- Square-like common-centroid layout



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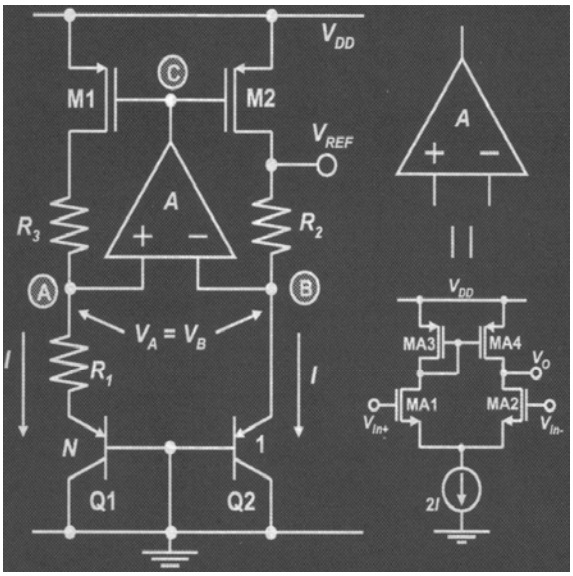
Typical Low-Voltage Implementation

- Error-amplifier current mirror enforces $V_A = V_B$
- Min $V_{DD} = V_{REF} + |V_{ov,M2}|$
- Offset voltage → error
- Offset voltage = function of V_{TH}, mobility and transistor size → temperature dependent
- Use simple amplifier
- Reduce both systematic and random offset



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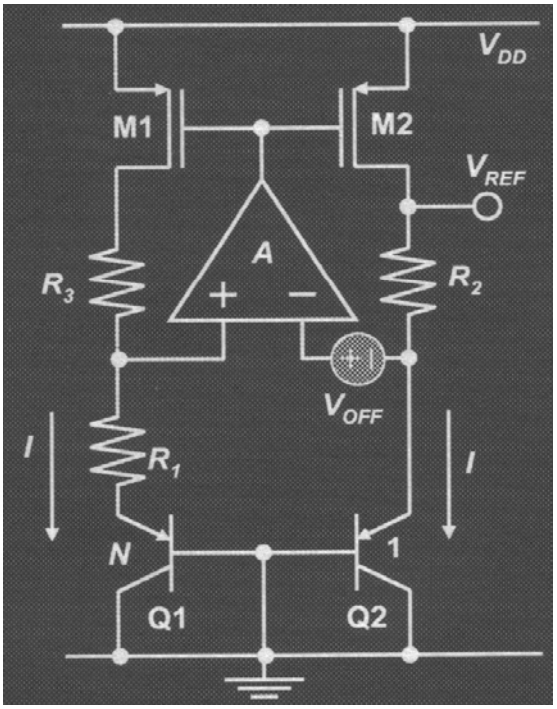
Offset Voltage Consideration

$$I = \frac{V_T \ln(N) + V_{OFF}}{R_1}$$

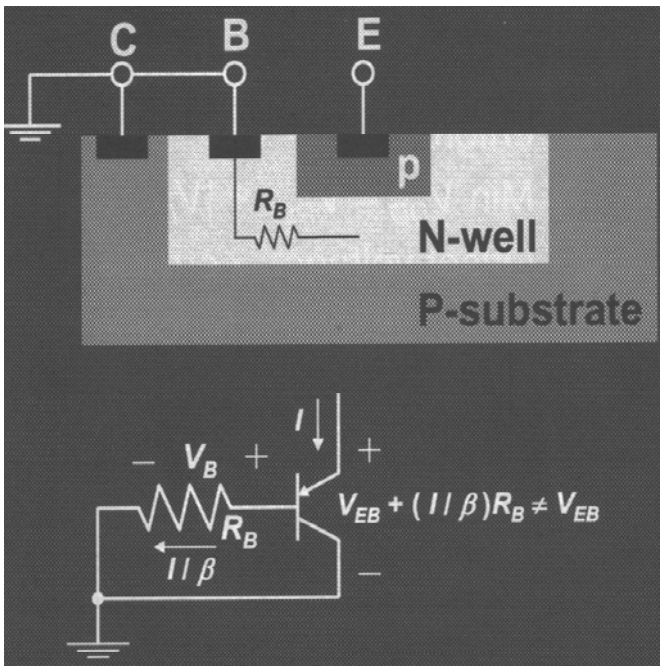
$$\Rightarrow V_{ref} = V_{EB2} + (\frac{R_2}{R_1})[V_T \cdot \ln(N) + V_{OFF}]$$

- A larger N is used to minimize the required R_2/R_1, and the effect of the amplifier offset
- Increase chip area



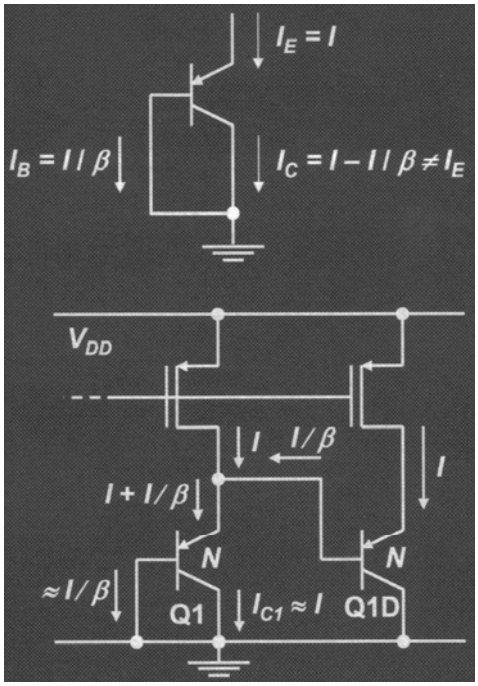
Base Resistance Consideration

- Large base resistance of parasitic vertical BJT
- Diode-connected BJT ≠ V_{EB}
- As mentioned before, I < 0.1mA
- Not due to low-power design, but due to reduce voltage across R_B
- On layout, more N-well contacts to reduce R_B



Base Current Compensation

- β is small in CMOS technology
- $I_C \neq I_E$ and I_C is a function of β
- Introduced β in I_C causes extra errors and temperature dependence
- Base current compensation by a dummy transistor Q1D
- I_E of Q1 = I + I/β
  I_C of Q1 = I
- Q1D must match with Q1



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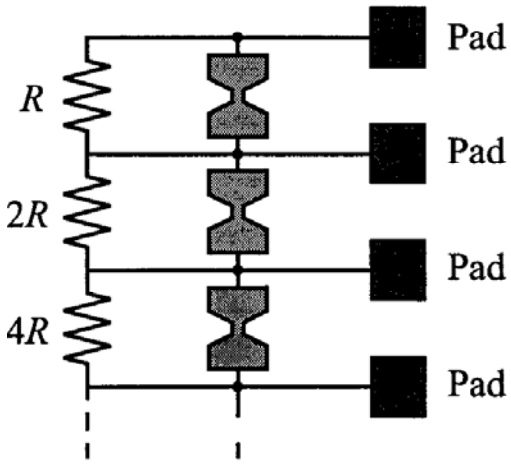
Resistor Trimming

- Resistor ratio can be fine-tuned by using a series of resistor network associated with fuse
- By burning the fuse, the resistor value can be adjusted to fine-tune the reference voltage and the temperature with zero tempco to a particular value



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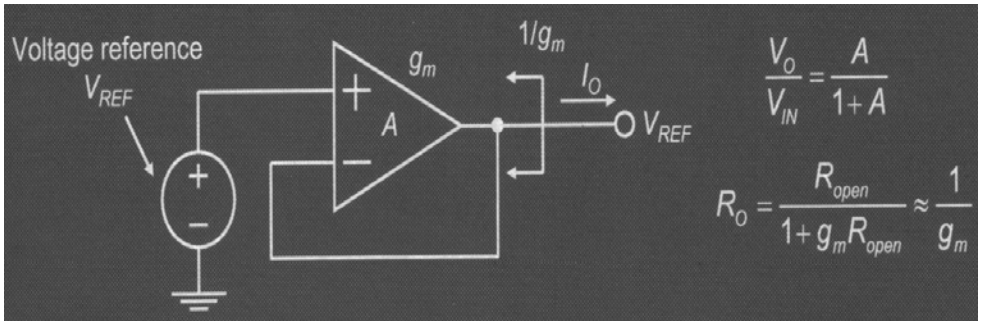
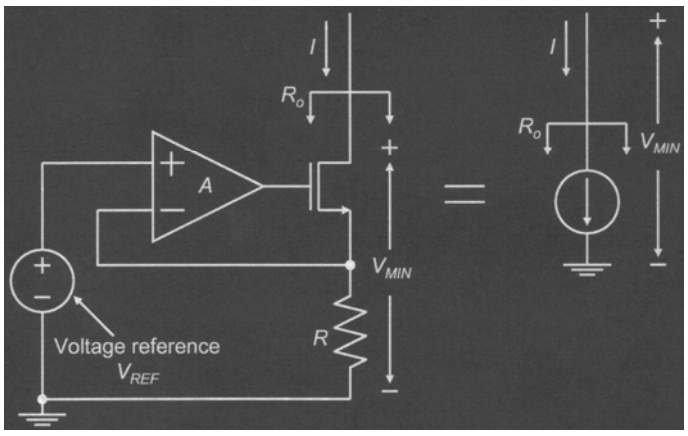
Buffered Voltage Reference



- Series-shunt feedback
- High output current to drive resistive load
- Low output resistance
- Isolation to reduce cross-talk through reference circuit

Current Source Generated by a Voltage Reference

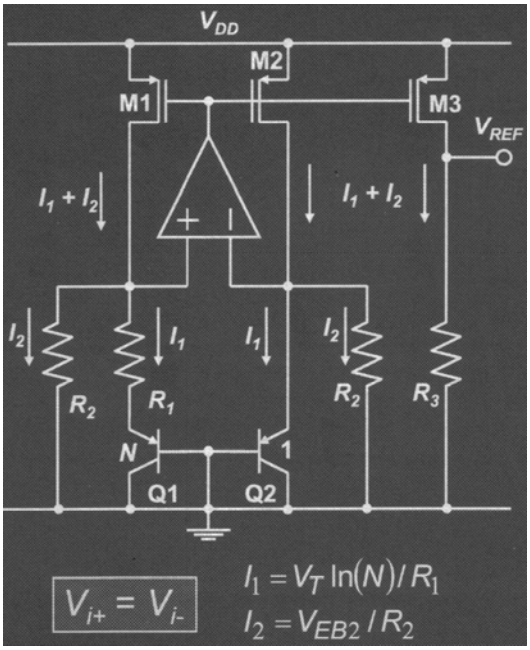


- Series-series feedback
- $I = V_{REF}/R$
- $V_{MIN} = V_{ov} + V_{REF}$

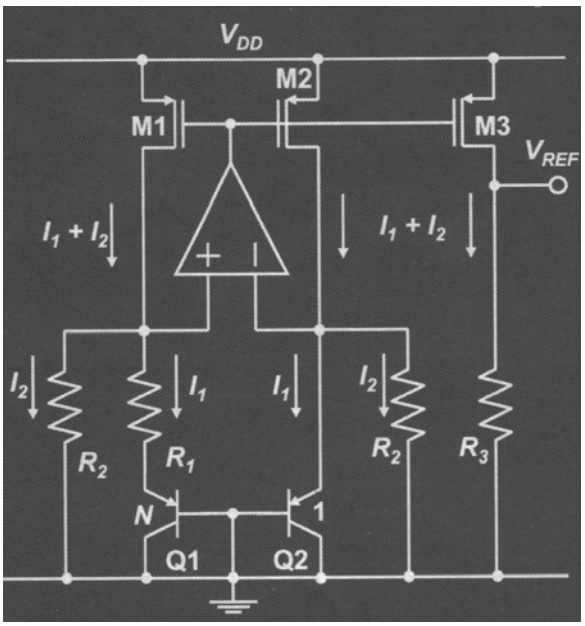
CMOS Bandgap Reference with Sub-1-V Operation (1)

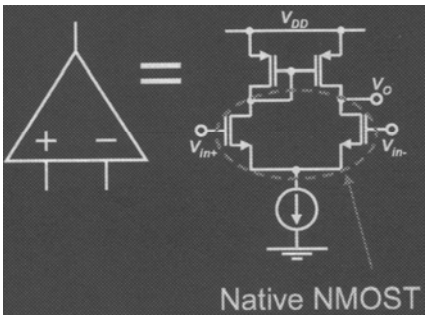
$$V_{REF} = (\frac{R_3}{R_2})(V_{EB2} + (\frac{R_2}{R_1})\ln(N) \cdot V_T)$$

- R_1, R_2 & R_3 of same material
- Good matching R_1 and R_2 for optimizing tempco
- Good matching R_2 and R_3 for adjusting the value of V_{REF}
- M1, M2 & M3 of equal W, L
- $V_{REF} \approx$ 0.5-0.7 V for matching V_{DS} of M1-M3 at different V_{DD}



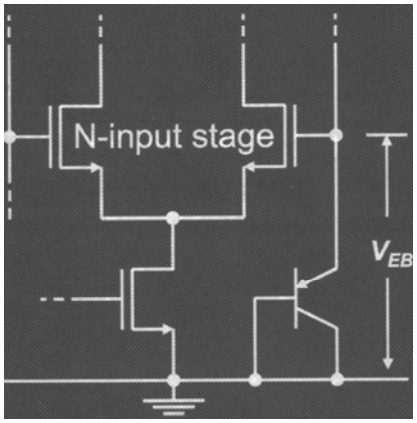
CMOS Bandgap Reference with Sub-1-V Operation (2)



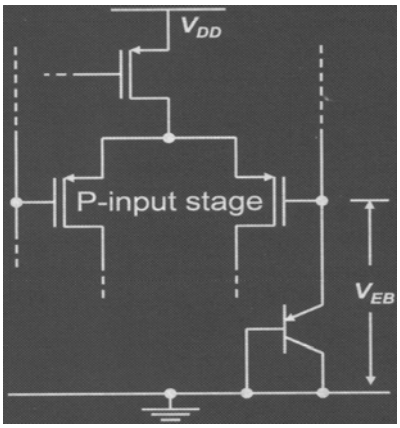


- Native NMOST : V_{THN} = 0.2V
- Not available in standard CMOS technologies

Low-Voltage Design Problem of Error Amplifier



- Worst case (smallest) V_{EB} at maximum operational temperature
- $V_{EB} > V_{THN} + 2V_{ov}$
- Low-V_{THN} (<0.4V) technology
- Body effect increases V_{THN}



- Worst case (largest) V_{EB} and $|V_{THP}|$ at minimum temperature
- $V_{EB} < V_{DD} - |V_{thp}| - 2|V_{ov}|$
- $V_{DD(min)} = V_{EB} + |V_{THP}| + 2V_{ov}$

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- H. Banba, *et. al.* "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 670-674, May 1999.
- K. N. Leung, *et. al.* "A sub-1-V 15-ppm/°C CMOS bandgap voltage reference without requiring low threshold voltage device," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 526-530, Apr. 2002.
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