For your protection

Most CMOS chips include two protection diodes at every I/O pad, wired as clamps. These diodes limit the input voltage from going much higher than V_{CC} or lower than ground. This limitation on the input voltage prevents gate-oxide blowout or latch-up of the entire chip, either of which might otherwise easily occur on an unprotected I/O pad during an ESD transient.

On a schematic, ESD-protection diodes resemble the diodes engineers sometimes use to limit overshoot and undershoot on a high-speed bus, but with one significant difference: the expected *lifetime* of the diode. An overshoot-limiting diode is huge compared with its ESD-protection cousin, and, because of its large size, the overshoot-limiting diode can absorb pulse after pulse of high-powered current transients, lasting essentially forever. ESD-protection diodes, on the other hand, are small, have limited strength, and aim to handle *only a few events* in their lifetime.

If you depend on ESD-protection diodes to clamp transients on a high-speed bus, you risk burning them out. Because a burned-out diode fails in the open state, obliterating its clamping effect, the next ESD blast that roars through your system will likely cause permanent damage.

Can you test ESD-protection diodes to measure their robustness? Yes, an accelerated-life-testing strategy exists that works fairly well, but a better option is to limit your transient peaks so this question never arises.

Accelerated-life testing of ESD diodes depends on the use of Black's equation for the MTTF of a metallization trace (**Reference 1**). The metallization trace leading to your protection diode, and not the diode itself, will likely fail, so your testing plan focuses on the likelihood of burning out that tiny, delicate connection. The protection-diode traces are tiny, by the way, to limit both their parasitic capacitance and the space they consume on-die.

$$\text{MTTF (HOURS)} = \frac{A}{J^2}\text{EXP}\left(\frac{-E}{kT}\right).$$

In Black's equation, the constant A is experimentally determined, J is the current density (amps per square centimeter), the exponent 2 is approximately correct for ESD-protection-diode trace failure due to electromigration in aluminum traces, E is an aluminum grain-boundary activation energy of approximately 0.6 eV (see EIA/JEDEC publication 122 standards), k is Boltzmann's constant (8.616×10^{-5} eV/K), and T is the junction temperature in degrees Kelvin.

ESD-PROTECTION DIODES ARE SMALL, HAVE LIMITED STRENGTH, AND AIM TO HANDLE *ONLY A FEW EVENTS* IN THEIR LIFETIME.

If you purposefully inject dc current into an ESD-protection diode to induce failure, Black's equation suggests that the MTTF should scale inversely with the square of current. If you observe an inverse-square relationship in your experiments, then you can extrapolate backward to determine the MTBF at a much-reduced dc current. If you apply too much current, other effects, such as heating, come into play, and the result no longer scales according to Black's equation.

Pulsed currents, such as repetitive signal-integrity transients, induce failure at a rate related to the peak current but derated according to the duty cycle of the pulses. For example, a 1-nsec transient of 30 mA that occurs every 50 nsec should induce failure at 50 times the MTTF of a 30-mA dc current.

Beware that no standards exist that govern the implementation of ESD diodes in CMOS chips. Implementations vary widely. Data gathered from one manufacturer's IC process do not apply to other of its chip processes or to other manufacturers.□

Reference

1. Black, James R, "Electromigration Failure Modes in Aluminum Metallization for Semiconductor Devices," Proceedings of the IEEE, 57, No. 9, September 1969, pgs.1587 to 1594.

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