CMOS Schmitt Trigger—A Uniquely Versatile Design Component

Fairchild Semiconductor
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INTRODUCTION

The Schmitt trigger has found many applications in numerous circuits, both analog and digital. The versatility of a TTL Schmitt is hampered by its narrow supply range, limited interface capability, low input impedance and unbalanced output characteristics. The Schmitt trigger could be built from discrete devices to satisfy a particular parameter, but this is a careful and sometimes time-consuming design.

The CMOS Schmitt trigger, which comes six to a package, uses CMOS characteristics to optimize design and advance into areas where TTL could not go. These areas include: interfacing with op amps and transmission lines, which operate from large split supplies, logic level conversion, linear operation, and special designs relying on a CMOS characteristic. The CMOS Schmitt trigger has the following advantages:

- High impedance input ($10^{12}\Omega$ typical)
- Balanced input and output characteristics
  - — Thresholds are typically symmetrical to ½ V_{CC}
  - — Outputs source and sink equal currents
  - — Outputs drive to supply rails
- Positive and negative-going thresholds show low variation with respect to temperature
- Wide supply range (3V–15V), split supplies possible
- Low power consumption, even during transitions
- High noise immunity, 0.70 V_{CC} typical

Applications demonstrating how each of these characteristics can become a design advantage will be given later in the application note.

ANALYZING THE CMOS SCHMITT

The input of the Schmitt trigger goes through a standard input protection and is tied to the gates of four stacked devices. The upper two are P-channel and the lower two are N-channel. Transistors P3 and N3 are operating in the source follower mode and introduce hysteresis by feeding back the output voltage, out', to two different points in the stack.

When the input is at 0V, transistors P1 and P2 are ON, and N1, N2 and P3 are OFF. Since out' is high, N3 is ON and acting as a source follower, the drain of N1, which is the source of N2, is at $V_{CC} - V_{TH}$. If the input voltage is ramped up to one threshold above ground transistor N1 begins to turn ON, N1 and N3 both being ON form a voltage divider network biasing the source of N2 at roughly half the supply. When the input is a threshold above ½ V_{CC}, N2 begins to turn ON and regenerative switching is about to take over. Any more voltage on the input causes out' to drop. When out' drops, the source of N3 follows its gate, which is out', the influence of N3 in the voltage divider with N1 rapidly diminishes, bringing out' down further yet. Meanwhile P3 has started to turn ON, its gate being brought low by the rapidly dropping out'. P3 turning ON brings the source of P2 low and turns P2 OFF. With P2 OFF, out' crashes down. The snapping action is due to greater than unity loop gain through the stack caused by positive feedback through the source follower transistors. When the input is brought low again an identical process occurs in the upper portion of the stack and the snapping action takes place when the lower threshold its reached.

Out' is fed into the inverter formed by P4 and N4; another inverter built with very small devices, P5 and N5, forms a latch which stabilizes out'. The output is an inverting buffer capable of sinking 360 µA or two LPTTL loads.

The typical transfer characteristics are shown in *Figure 2*; the guaranteed trip point range is shown in *Figure 3*.

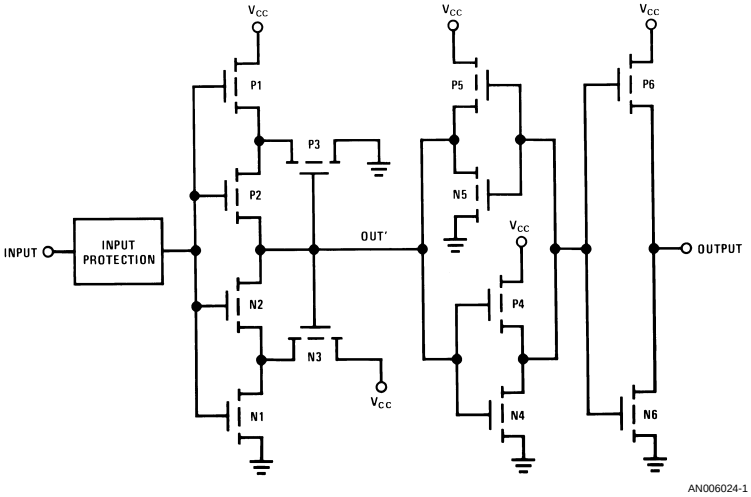


FIGURE 1. CMOS Schmitt Trigger

WHAT HYSTERESIS CAN DO FOR YOU

Hysteresis is the difference in response due to the direction of input change. A noisy signal that traverses the threshold of a comparator can cause multiple transitions at the output, if the response time of the comparator is less than the time between spurious effects. A Schmitt trigger has two thresholds: any spurious effects must be greater than the threshold difference to cause multiple transitions. With a CMOS Schmitt at V_{CC} = 10V there is typically 3.6V of threshold difference, enough hysteresis to overcome almost any spurious signal on the input.

A comparator is often used to recover information sent down an unbalanced transmission line. The threshold of the comparator is placed at one half the signal amplitude (See *Figure 4b*). This is done to prevent slicing level distortion. If a 4 µs wide signal is sent down a transmission line a 4 µs wide signal should be received or signal distortion occurs. If the comparator has a threshold above half the signal amplitude, then positive pulses sent are shorter and negative pulses are lengthened (See *Figure 4c*). This is called slicing level distortion. The Schmitt trigger does have a positive offset, V_{T+}, but it also has a negative offset V_{T-}. In CMOS these offsets are approximately symmetrical to half the signal level so a 4 µs wide pulse sent is also recovered (see *Figure 4d*). The recovered pulse is delayed in time but the length is not changed, so noise immunity is achieved and signal distortion is not introduced because of threshold offsets.

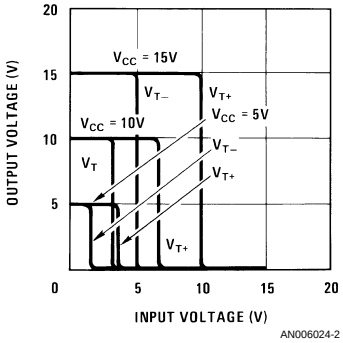


FIGURE 2. Typical CMOS Transfer Characteristics for Three Different Supply Voltages

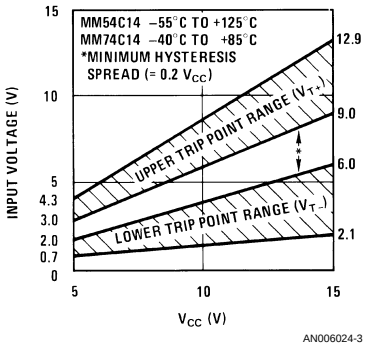


FIGURE 3. Guaranteed Trip Point Range

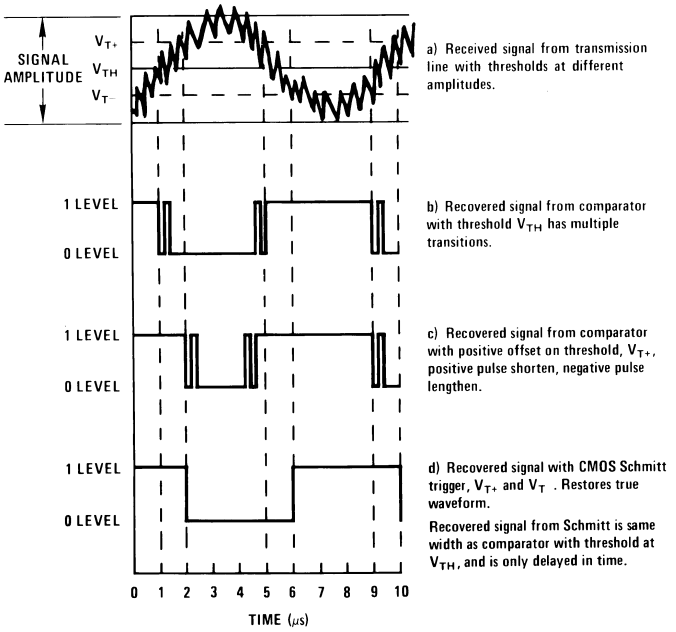
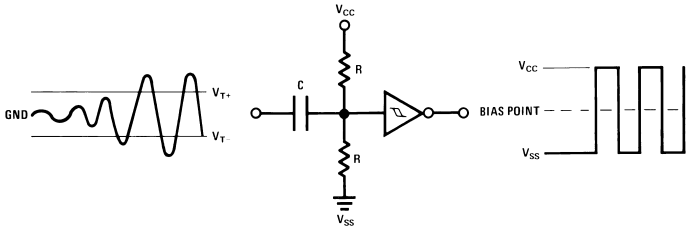
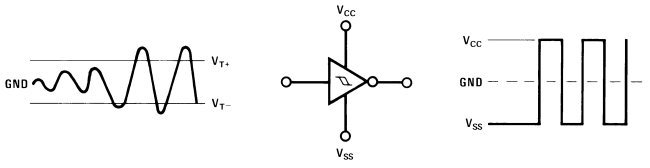


FIGURE 4. CMOS Schmitt Trigger Ignores Noise

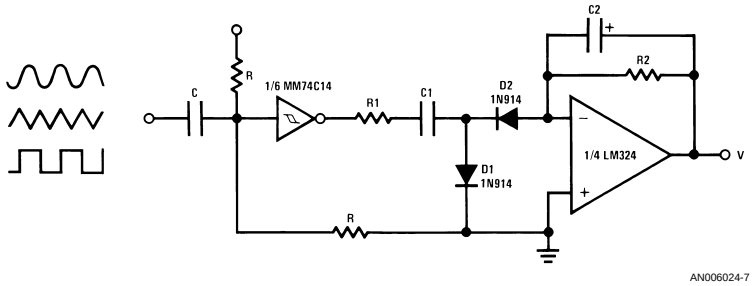


a) Capacitor impedance at lowest operating frequency should be much less than R ‖ R = ½R.



b) By using split supply (±1.5V to ±7.5V) direct interface is achieved.

FIGURE 5. Sine to Square Wave Converter with Symmetrical Level Detection



Where R1C1 ≅ $1/f_{MAX}$ and R2C2 ≅ response time of voltmeter
V_{OUT} = fR2C1Δ where ΔV = V_{CC}

FIGURE 6. Diode Dump Tach Accepts any Input Waveform

APPLICATIONS OF THE CMOS SCHMITT

Most of the following applications use a CMOS Schmitt characteristic to either simplify design or increase performance. Some of the applications could not be done at all with another logic family.

The circuit in *Figure 5a* is the familiar sine to square wave converter. Because of input symmetry the Schmitt trigger is easily biased to achieve a 50% duty cycle. The high input impedance simplifies the selection of the biasing resistors and coupling capacitor. Since CMOS has a wide supply range the Schmitt trigger could be powered from split supplies (see *Figure 5b*). This biases the mean threshold value around zero and makes direct coupling from an op amp output possible.

In *Figure 4*, we see a frequency to voltage converter that accepts many waveforms with no change in output voltage. Although the energy in the waveforms are quite different, it is only the frequency that determines the output voltage. Since the output of the CMOS Schmitt pulls completely to the supply rails, a constant voltage swing across capacitor C1 causes a current to flow through the capacitor, dependent only on frequency. On positive output swings, the current is dumped to ground through D1. On negative output swings, current is pulled from the inverting op amp node through D2 and transformed into an average voltage by R2 and C2.

Since the CMOS Schmitt pulls completely to the supply rails the voltage change across the capacitor is just the supply voltage.

Schmitt triggers are often used to generate fast transitions when a slowly varying function exceeds a predetermined level. In *Figure 7*, we see a typical circuit, a light activated switch. The high impedance input of the CMOS Schmitt trigger makes biasing very easy. Most photo cells are several kΩ brightly illuminated and a couple MΩ dark. Since CMOS has a 10^{12} typical input impedance, no effects are felt on the input when the output changes. The selection of the biasing resistor is just the solution of a voltage divider equation.

A CMOS application note wouldn't be complete without a low power application. *Figure 8* shows a simple RC oscillator. With only six R's and C's and one Hex CMOS trigger, six low power oscillators can be built. The square wave output is approximately 50% duty cycle because of the balanced input and output characteristics of CMOS. The output frequency equation assumes that $t_1 = t_2 \geq t_{pd0} + t_{pd1}$.

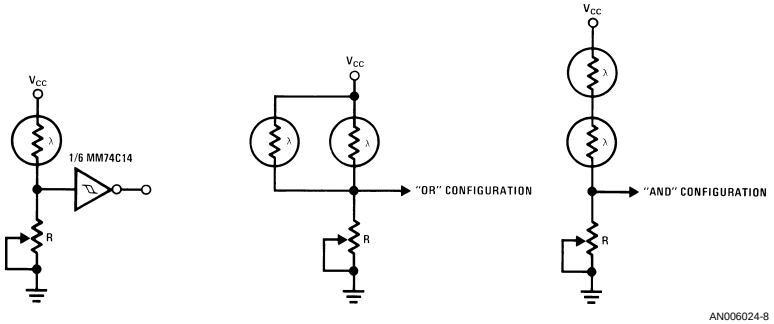
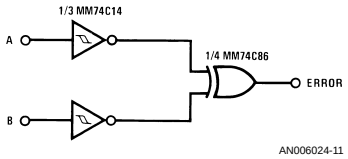


FIGURE 7. Light activated switch couldn't be simpler. The input voltage rises as light intensity increases, when V_{T+} is reached, the output will go low and remain low until the intensity is reduced significantly.

$$f_O = \frac{1}{RC\ \ell n\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

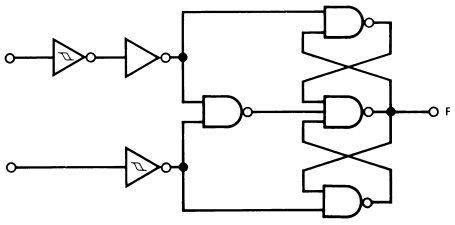
FIGURE 8. Simplest RC Oscillator? Six R's and C's make the CMOS Schmitt into six low power oscillators. Balanced input and output characteristics give the output frequency a typically 50% Duty Cycle.



$\overline{A}$ B + A$\overline{B}$ = Error

Error is detected when transmission line is unbalanced in either direction.

a) Differential Error Detector



Transmitted data appears at F as long as transmission line is balanced, unbalanced data is ignored and error is detected by above circuit.

b) Differential Line Receiver

Truth Table

A	B	F
0	0	NC
0	1	0
1	0	1
1	1	NC

NC = No Change

1/3 MM74C14 Schmitt Trigger

1/6 MM74C04 Inverter

3/4 MM74C00 2-Input NAND

1/3 MM74C10 3-Input NAND

FIGURE 9. Increase noise immunity by using the CMOS Schmitt trigger to demodulate a balanced transmission line.

We earlier saw how the CMOS Schmitt increased noise immunity on an unbalanced transmission line. *Figure 9* shows an application for a balanced or differential transmission line. The circuit in *Figure 7 a* is CMOS EXCLUSIVE OR, the MM74C86, which could also be built from inverters, and NAND gates. If unbalanced information is generated on the line by signal crosstalk or external noise sources, it is recognized as an error.

The circuit in *Figure 9b* is a differential line receiver that recovers balanced transmitted data but ignores unbalanced signals by latching up. If both circuits of *Figure 9* were used together, the error detector could signal the transmitter to stop transmission and the line receiver would remember the last valid information bit when unbalanced signals persisted on the line. When balanced signals are restored, the receiver can pick up where it left off.

The standard voltage range for CMOS inputs is V_{CC} + 0.3V and ground − 0.3V. This is because the input protection network is diode clamped to the supply rails. Any input exceeding the supply rails either sources or sinks a large amount of current through these diodes. Many times an input voltage range exceeding this is desirable; for example, transmission lines often operate from ±12V and op amps from ±15V. A solution to this problem is found in the MM74C914. This new device has an uncommon input protection that allows the input signal to go to 25V above ground, and 25V below V_{CC}. This means that the Schmitt trigger in the sine to square wave converter, in *Figure 6b*, could be powered by ±1.5V supplies and still be directly compatible with an op amp powered by ±15V supplies.

A standard input protection circuit and the new input protection are shown in *Figure 10*. The diodes shown have a 35V breakdown. The input voltage can go positive until reverse biased D2 breaks down through forward bias D3, which is 35V above ground. The input voltage can go negative until reverse biased D1 breaks down through forward bias D2, which is 35V below V_{CC}. Adequate input protection against static charge is still maintained.

CMOS can be linear over a wide voltage range if proper consideration is paid to the biasing of the inputs. *Figure 11* shows a simple VCO made with a CMOS inverter, acting as an integrator, and a CMOS Schmitt, acting as a comparator with hysteresis. The inverter integrates the positive difference between its threshold and the input voltage V_{IN}. The inverter output ramps up until the positive threshold of the Schmitt trigger is reached. At that time, the Schmitt trigger output goes low, turning on the transistor through R_S and speeding up capacitor C_S. Hysteresis keeps the output low until the integrating capacitor C is discharged through R_D. Resistor R_D should be kept much smaller than RC to keep reset time negligible. The output frequency is given by

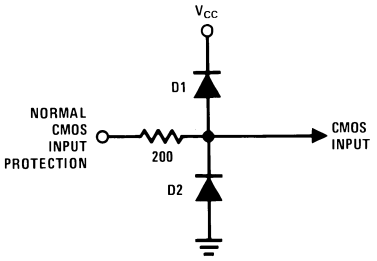
$$f_O = \frac{V_{TH} - V_{IN}}{(V_{T+} - V_{T-})R_{CC}}.$$

The frequency dependence with control voltage is given by the derivative with respect to Vin. So,

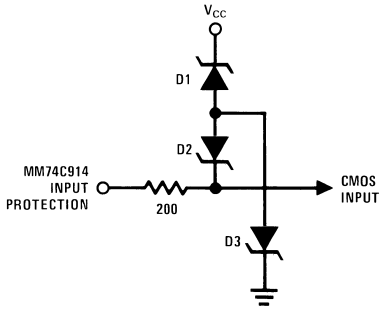
$$\frac{d f_O}{d V_{IN}} = \frac{-1}{(V_{T+} - V_{T-})\,RC},$$

where the minus sign indicates that the output frequency increases as the input is brought further below the inverter threshold. The maximum output frequency occurs when V_{IN}

is at ground and the frequency will decrease as V_{IN} is raised up and will finally stop oscillating at the inverter threshold, approximately 0.55 V_{CC}.

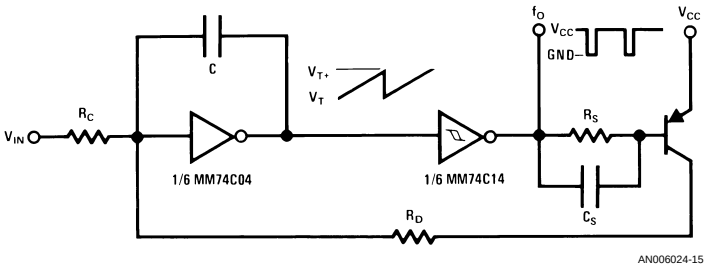


a)



b)

FIGURE 10. Input protection diodes, in a) Normally limit the input voltage swing to 0.3V above V_{CC} and 0.3V below ground. In b) D2 or D1 is reverse biased allowing input swings of 25V above ground or 25V below V_{CC}.



$$f_O = \frac{V_{TH} - V_{IN}}{(V_{T+} - V_T)\, R_C C}$$

$$\frac{d f_O}{d V_{IN}} = \frac{-1}{(V_{T+} - V_T)\, R_C C}$$

$0 \leq V_{IN} \leq \frac{1}{2} V_{CC}$

FIGURE 11. Linear CMOS (Voltage Controller Oscillator)

The pulses from the VCO output are quite narrow because the reset time is much smaller than the integration time. Pulse stretching comes quite naturally to a Schmitt trigger. A one-shot or pulse stretcher made with an inverter and Schmitt trigger is shown in *Figure 12*. A positive pulse coming into the inverter causes its output to go low, discharging the capacitor through the diode D1. The capacitor is rapidly discharged, so the Schmitt input is brought low and the output goes positive. Check the size of the capacitor to make sure that inverter can fully discharge the capacitor in the input pulse time, or

$$I_{SINK\ INVERTER} > \frac{C\,\Delta V}{\Delta T} + \frac{\Delta V}{R}$$

where $\Delta V = V_{CC}$ for CMOS, and ΔT is the input pulse width.

For very narrow pulses, under 100 ns, the capacitor can be omitted and a large resistor will charge up the CMOS gate capacitance just like a capacitor.

When the inverter input returns to zero, the blocking diode prevents the inverter from charging the capacitor and the resistor must charge it from its supply. When the input voltage of the Schmitt reaches V_{T+} , the Schmitt output will go low sometime after the input pulse has gone low.

THE SCHMITT SOLUTION

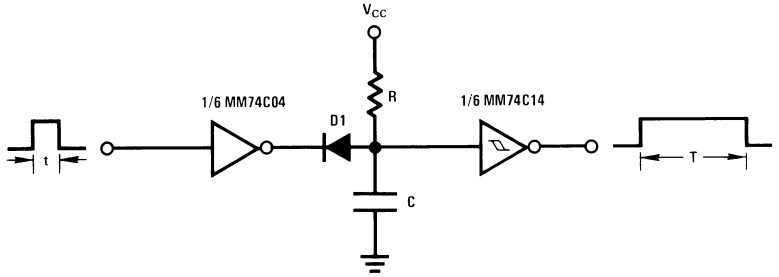
The Schmitt trigger, built from discrete parts, is a careful and sometimes time-consuming design. When introduced in integrated TTL, a few years ago, many circuit designers had renewed interest because it was a building block part. The input characteristics of TTL often make biasing of the trigger input difficult. The outputs don't source as much as they sink, so multivibrators don't have 50% duty cycle, and a limited supply range hampers interfacing with non-5V parts.

The CMOS Schmitt has a very high input impedance with thresholds approximately symmetrical to one half the supply. A high voltage input is available. The outputs sink and source equal currents and pull directly to the supply rails.

A wide threshold range, wide supply range, high noise immunity, low power consumption, and low board space make the CMOS Schmitt a uniquely versatile part.

Use the Schmitt trigger for signal conditioning, restoration of levels, discriminating noisy signals, level detecting with hysteresis, level conversion between logic families, and many other useful functions.

The CMOS Schmitt is one step closer to making design limited only by the imagination of the designer.



$T_O = t_{IN} + T$

$$T = RC\,\ell n\left(\frac{V_{CC} - V_{BE}}{V_{CC} - V_{T+}}\right) \quad \text{BE SURE THAT } I_{SINK\ INVERTER} > \frac{C\,V_{CC}}{t} + \frac{V_{CC}}{R}$$

FIGURE 12. Pulse Stretcher. A CMOS inverter discharges a capacitor, a blocking diode allows charging through R only. Schmitt trigger output goes low after the RC delay.

Fairchild Semiconductor Corporation
Americas
Customer Response Center
Tel: 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

www.fairchildsemi.com