ECE473 Quiz 4 Oct 27, 2008

Name: KEY

Consider the schematic and code snippet below. The function of the circuit is to display the buttons pressed on the bar graph display. No debouncing is required. Switches are to be checked (read) every 1/128 sec. Timing diagram is to be followed in regards to data transmitted and received (order and logic level). All the setup is done in main(). All processing of the data is done in the timer/counter zero ISR. SPI is not using interrupts.

Fill in the code below:

```
ISR(TIMERØ_OVF_vect      ){
→ PORTB &= ~(Øx Ø1); //Assert ss_n to allow HC165 to shift
 SPDR = ØxØØ; // send dummy data out to get switch input
 while(bit_is_clear(SPSR, SPIF){}; //spin till data is all in MISO
 SPDR = SPDR;
 while(bit_is_clear(SPSR,SPIF){}; //spin till data is out of MOSI
→ PORTB |= (ØxØ1); // deassert ss_n to both load HC165 + to
                   // clock HC595 output registers

}//ISR

main(){
  DDRB  |= ØxØ7; // bit Ø is output mode, sclk+ MOSI too
  PORTB |= ØxØ1; // SS_n is initially one
  //setup TCNT0 for overflow interrupt at 128hz rate with 32khz osc, normal mode
  ASSR  |= (1<<ASØ); // use 32khz osc ————> (ØxØ4)
  TIMSK |= (1<< TOIEØ); // enable interupts on overflow (ØxØ1)
  TCCR0 |= (1<< CSØØ); //no prescaling of 32khz ——> (ØxØ1) 0b00000001
  //setup SPI: master mode, 8Mhz sclk, MSB first, clk starts low
  SPCR |= (1<<SPE) | (1<<MSTR); → (Øx5Ø)
  SPSR |= (1<<SPI2X); ————> (ØxØ1)
  sei();        //enable global interrupts
  while(1){}    //loop forever
}//end main
```

[main, 28pts; ISR, 28pts]