10. Battery Backup System

10.1 Features

- Integrated battery backup system ensuring continuos, real-time clock during main power failure
- Battery backup power supply from dedicated V_{BAT} pin to power:
  - One 32-bit real-time counter
  - One ultra low power 32.768kHz crystal oscillator with failure detection monitor
  - Two battery backup registers
- Automatic power switching between main power and battery backup power:
  - Switching from main power to battery backup power at main power loss
  - Switching from battery backup power to main power at main power return

10.2 Overview

Many applications require a real-time clock that keeps running continuously, even in the event of a main power loss or failure. The battery backup system includes functions for this through automatic power switching between main power and a battery backup power supply. No external components are required. Figure 10-1 on page 119 shows an overview of the system.

On devices with a battery backup system, a backup battery can be connected to the dedicated V_{BAT} power pin. If the main power is lost, the backup battery will continue and power the real-time counter (RTC32), a 32.768kHz crystal oscillator with failure detection monitor, and two backup registers. The battery backup system does not provide power to other parts of the volatile memory in the device, such as SRAM and I/O registers outside the system.

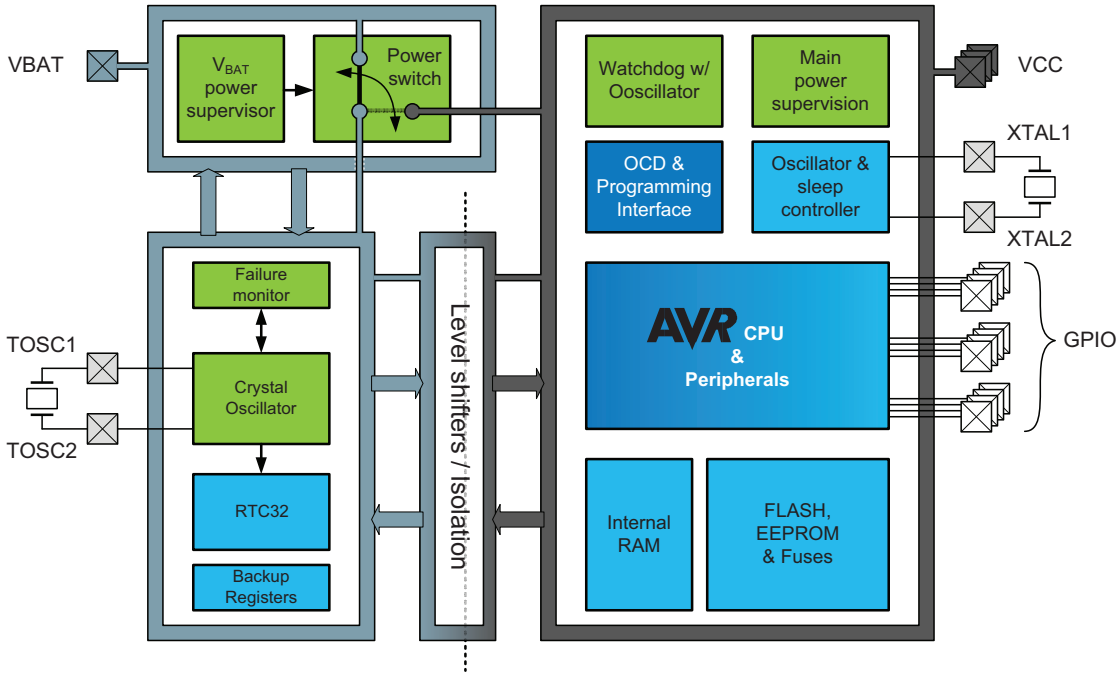
The device uses its BOD to detect main power loss and switch to power from the V_{BAT} pin. After main power is restored, the battery back system will automatically switch back to being powered from the main power again. The backup battery is drained only when main power is not present, and this ensures maximum battery life.

On devices with the battery backup system, the RTC32 will keep running in all sleep modes.

10.3 Battery Backup System

The battery backup system consists of a V_{BAT} power supervisor, a power switch, a crystal oscillator with failure monitor, a 32-bit real-time counter (RTC32), and two backup registers.

Figure 10-1. Battery backup system and its power domain implementation.



10.3.1 Power Supervisor

The power supervisor monitors the voltage on the V_{BAT} pin. It performs three main functions:

The power-on detection (BBPOD) function detects when power is applied to the V_{BAT} pin, i.e., when the backup battery is inserted. When this happens the battery backup power-on detection flag (BBPODF) is set and the power switch is disconnected to prevent the backup battery from being drained before the device is configured.

The brown-out detection (BBBOD) function monitors the V_{BAT} voltage level when the system is powered from the V_{BAT} pin. If the V_{BAT} voltage drops below a threshold voltage, the battery backup bod flag (BBBODF) is set. The BBBOD samples the V_{BAT} voltage level at around a 1Hz rate, and is designed for detecting slow voltage changes. The BBBOD is turned off when the device runs from the main power.

The power detection (BBPWR) function controls the V_{BAT} voltage after a reset. If no voltage is present on the V_{BAT} pin, the battery backup power flag will be set. This indicates that the backup battery is not present or has been drained. BBPODF, BBBODF, and the BBPWR flag are later referred to as the power supervision flags.

10.3.2 Power Switch

The power switch switches between main power and the V_{BAT} pin to power the system. This happens automatically, and is controlled from the main BOD in the device.

10.3.3 Crystal Oscillator with Failure Monitor

The crystal oscillator (XOSC) supports connection of a external 32.768kHz crystal. It provides a prescaled clock output selectable to 1.024kHz or 1Hz. The crystal oscillator is designed for ultra low power consumption and by default is configured for low ESR and load capacitance crystals. It is possible to enable a high ESR mode to drive crystals with high ESR or load capacitance, but this will increase current consumption. The crystal oscillator failure monitor will detect if the crystal is permanently or temporarily stopped and then set the crystal oscillator failure flag.

10.3.4 32-bit Real-time Counter

The 32-bit real-time counter (RTC32) will count each clock output from the crystal oscillator. It provides a one-millisecond or one-second resolution, depending on the crystal oscillator clock output selection. For more details on the 32-bit RTC, refer to the “RTC32 – 32-bit Real-Time Counter” on page 219.

10.3.5 Backup Registers

The two backup registers can be used to store volatile data parameters when Vcc is not present.

10.4 Configuration

During device initialization, the battery backup system and RTC32 must be configured before they can be used. The recommended configuration sequence is:

1. Apply a reset
2. Set the access enable bit
3. Optionally configure the oscillator output and ESR selection
4. Optionally enable the crystal oscillator failure monitor and the required delay before continuing configuration
5. Enable the crystal oscillator
6. Wait until the crystal oscillator ready flag is set
7. Configure and enable the RTC32

10.5 Operation

The main BOD monitors the main voltage (Vcc) level and controls the power switching. This must always be enabled. In active and idle modes, the BOD must be in continuos mode. In deep sleep modes, the BOD can be in continuos or sampled mode. The system is designed as a power backup system for the RTC. Reset sources other than the BOD and power loss (i.e. external reset, watchdog reset, and software reset) must be treated as a system reset. In this case, the device state should be treated as unknown and lead to complete re-initialization, including battery backup system configuration.

10.5.1 Main Power Loss

When Vcc drops below the programmed BOD threshold voltage, the device will:

1. Switch the battery backup system to be powered from the V_{BAT} pin and enable the BBBOD.
2. Ignore any input signals to the system to prevent accidental or partial configuration.
3. Stretch the 1Hz / 1.024kHz clock signal to avoid a clock edge when switching is active.
4. Reset the part of the device not powered from the V_{BAT} pin.

The battery backup system will continue to run as normal during the power switch and afterwards. When main power is lost, it is not possible to access or read the status from the registers.

10.5.2 Main Power Restore and Start-up Sequence

At every startup after main power is restored, the software should:

1. Control the main reset source to determine that a POR or BOD took place.
2. Check for power on the V_{BAT} pin by reading the BBPWR flag.
3. Read the power supervisor flags to determine further software action:

1. If all power supervision flags are cleared, the battery backup system runs as normal. The software should enable access to the battery backup system and check the crystal oscillator failure flag. If the flag is set, the software should assume that the RTC32 counter value is invalid and take appropriate action.
2. If any power supervision flags are set, it indicates the battery backup system has lost power sometime during the period when the rest of the device was unpowererd. Software should assume that the configuration and RTC32 value are invalid and take appropriate action.

10.6 Register Description

10.6.1 CTRL: Control register

Bit	7	6	5	4	3	2	1	0
+0x00	–	–	HIGHESR	XOSCSEL	XOSCEN	XOSCFDEN	ACCEN	RESET
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
initial Value	0	0	0	0	0	0	0	0

- **Bit 7: 6 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write this bit to zero when this register is written.

- **Bit 5 – HIGHESR: High ESR Mode**
  Setting this bit will increase the current used to drive the crystal and increase the swing on the TOSC2 pin. This allows use of crystals with higher load and higher ESR.

- **Bit 4 – XOSCSEL: Crystal Oscillator Output Selection**
  This bit selects the prescaled clock output from the 32.768kHz crystal oscillator. After reset, this bit is zero, and the 1Hz clock output is used as input for the RTC32. Setting this bit will select the 1.024kHz clock output as input for the RTC32. This bit cannot be changed when XOSCEN is set.

- **Bit 3 – XOSCEN: Crystal Oscillator Enable**
  Setting this bit will enable the 32.768kHz crystal oscillator. Writing the bit to zero will have no effect, and the oscillator will remain enabled until a battery backup reset is issued. The Crystal oscillator can also be used as 32.768kHz system clock after performing step one to three described in “Configuration” on page 120.

- **Bit 2 – XOSCFDEN: Crystal Oscillator Failure Detection Enable**
  Setting this bit will enable the crystal oscillator monitor. The monitor will detect if the crystal is stopped or loses connection temporarily. At least 64 swings must be lost before the failure detection is triggered. Writing the bit to zero will have no effect, and the crystal oscillator monitor will remain enabled until a battery backup reset is issued.

- **Bit 1 – ACCEN: Module Access Enable**
  Setting this bit will enable access to the battery backup registers. After main reset, this bit must be set in order to access (read from and write to) the battery backup registers, except for the BBPODF, the BBBODF, and the BBPWR flags, which are always accessible. Writing this bit to zero will have no effect; only a device reset will clear this bit.

- **Bit 0 – RESET: Reset**
  Setting this bit will force a reset of the battery backup system lasting one peripheral clock cycle. Writing the bit to zero will have no effect. Writing a one to XOSCEN or XOSCFDEN at the same time will block writing to this bit. When this bit is set, HIGHESR, XOSCSEL, XOSCEN, and XOSCFDEN in CTRL and XOSCRDY in STATUS will be cleared.
  This bit is protected by the Configuration Change Protection mechanism. For a detailed description, refer to “Configuration Change Protection” on page 13.

10.6.2 STATUS: Status register

Bit	7	6	5	4	3	2	1	0
+0x01	BBPWR	–	–	–	XOSCRDY	XOSCFAIL	BBBODF	BBPODF
Read/Write	R/W	R	R	R	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	x	x	0	0

- **Bit 7 – BBPWR: Battery Backup Power**
  This flag is set if no power is detected on the V_{BAT} pin when the device leaves reset. The flag can be cleared by writing a one to this bit location.
- **Bit 6:4 – Reserved**
  These bits are unused and reserved for future use. For compatibility with future devices, always write these bits to zero when this register is written.
- **Bit 3 – XOSCRDY: Crystal Oscillator Ready**
  This flag is set when the 32.678kHz crystal oscillator has started and is stable and ready. The flag can be cleared by applying a reset to the battery backup system. The actual start-up time is crystal dependent. Refer to the data-sheet for the crystal oscillator used for more information.
- **Bit 2 – XOSCFAIL: Crystal Oscillator Failure**
  This flag is set if a crystal oscillator failure is detected. The flag can be cleared by writing a one to this bit location or by applying a reset to the battery backup system.
- **Bit 1 – BBBODF: Battery Backup Brown-out Detection Flag**
  This flag is set if battery backup BOD is detected when the battery backup system is powered from the V_{BAT} pin. The flag can be cleared by writing a one to this bit location. This flag is not valid when BBPWR is set.
- **Bit 0 – BBPODF: Battery Backup Power-on Detection Flag**
  This flag is set if battery backup power-on is detected; i.e., when power is connected to the V_{BAT} pin. The flag is updated only during device startup when main power is applied. Applying or reapplying power to the V_{BAT} pin while main power is present will not change this flag until main power is removed and re-applied. The flag can be cleared by writing a one to this bit location. This flag is not valid when BBPWR is set.

10.6.3 BACKUP0: Backup register 0

Bit	7	6	5	4	3	2	1	0
+0x02	BACKUP0[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	x	x	x	x	x	x	x	x

- **Bit 7:0 – BACKUP0[7:0]: Backup Value 0**
  This register can be used to store data in the battery backup system before the main power is lost or removed.

10.6.4 BACKUP1: Backup register 1

Bit	7	6	5	4	3	2	1	0
+0x03	BACKUP1[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	x	x	x	x	x	x	x	x

- **Bit 7:0 – BACKUP1[7:0]: Backup Value 1**
  This register can be used to store data in the battery backup system before the main power is lost or removed.

10.7 Register summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
+0x00	CTRL	–	–	HIGHESR	XOSCSEL	XOSCEN	XOSCFDEN	ACCEN	RESET	122
+0x01	STATUS	BBPWR	–	–	–	XOSCRDY	OSCFAIL	BBBODF	BBPODF	122
+0x02	BACKUP0	BACKUP0[7:0]								123
+0x03	BACKUP1	BACKUP1[7:0]								123