64A4U Overview - Why Xmega?

- More numerous, powerful and complex(!) peripherals than Mega
- Faster CPU that can run at 32Mhz from 2.7V
- Lower power consumption possible
- In-system programming different, 2-pin PDI interface
- Biggest benefit to this class is that the peripherals are similar to a well-equipped ARM chip but with a well-tested, and familiar toolset. Also, you don’t have to use any bloated library frameworks.
Two Databooks cover the A1U subset of parts.

- Detailed functional descriptions for all the AU parts (A1, A2, A3, A4) are in the Xmega AU Manual (8331F-AVR-04-2013).
- Electrical, timing and packaging details for the ATXmega64A4U are in: Atmel-83851-AVR-ATxmega64A4U-Datasheet-09/2014.
- Both are linked from the class web page.
64A4U Overview
64A4U Overview - ALU

- Nearly identical to Mega128.
- 8/16-bit, RISC CPU, 142 instructions (9 added)
- Hardware multiplier
- 32x8-bit registers directly connected to the ALU
- Stack in RAM
- Single cycle execution mostly
- Direct addressing up to 16MB of program memory and 16MB of data memory
- True 16/24-bit access to 16/24-bit I/O registers
- Efficient support for 8, 16, and 32-bit arithmetic
64A4U Overview - Memories

- **Flash Memory**
  - One linear address space
  - In-system programmable
  - Self-programming and boot loader support

- **Data Memory**
  - SRAM-based
  - One linear address space
  - Single-cycle access from CPU

- **EEPROM Memory**
  - Byte and page accessible
  - 2K bytes in size

- **I/O memory**
  - Config and status registers for all modules
  - 16-bit general purpose register for global variables or flags
  - Many more peripherals, looks like typical ARM part
Support for SRAM, SDRAM, Memory-mapped external HW
Production signature row memory (factory programmed)
ID for each uC device type, and device serial number
Calibration bytes for factory calibrated peripherals
User signature row
  One flash page in size
  Can be read and written from software
  Content kept after chip erase
64A4U Overview - Clock System
64A4U Overview - Clock System

- Safe run-time clock switching
- Internal oscillators:
  - 32MHz run-time calibrated and tunable oscillator
  - 2MHz run-time calibrated oscillator
  - 32.768kHz calibrated oscillator
  - 32kHz ultra low power (ULP) oscillator with 1kHz output
- External clock options
  - 0.4MHz - 16MHz crystal oscillator
  - 32.768kHz crystal oscillator
  - External clock
- PLL with 20MHz - 128MHz output frequency
  - Not for CPU
  - 1x to 31x multiplication
- Clock prescalers with 1x to 2048x division
- Fast peripheral clocks running at two and four times the CPU clock
Power management adjusts power consumption and what peripherals are "on".

Five sleep modes:
- Idle
- Power down
- Power save
- Standby
- Extended standby
Changes driven by end users

No 5V compatibility

No pin compatibility between Mega and X-Mega

Consistency between parts/ports/modules

Analog functions always on Port A and B.

TWI, USART, SPI always on Ports D and E.

Module register access defined in C structures: typedef struct

Module registers consistent across part families
64A4U Overview - I/O Ports

- 78 General purpose IO pins with individual configuration
- Configurable driver and pull settings:
  - Totem-pole, Wired-AND, Wired-OR, Bus-keeper, Inverted I/O
  - Optional pull-up and pull-down resistor on input
  - Slew rate control
- Input with synchronous and/or asynchronous sensing
- Sense both edges, rising edges, falling edges, logic low level
- Asynchronous pin change can wake device from all sleep modes
- Two port interrupts with pin masking per I/O port
- Efficient and safe access to port pins using HW read-modify-write via dedicated toggle/clear/set registers
- Mapping of port registers into bit-accessible I/O memory space
- Selectable USART, SPI, and timer/counter input/output pin locations
64A4U Overview

TC0/1 16-bit Timer/Counter Type 0 and 1

PORTC, PORTD, PORTE and PORTF each has one timer/counter 0 and one timer/counter 1. Notation of these timer/counters are TCC0 (timer/counter C0), TCC1, TCD0, TCD1, TCE0, TCE1, TCF0, and TCF1, respectively.
64A4U Overview

- TC0/1 16-bit Timer/Counter Type 0 and 1
  - Eight 16-bit timer/counters
  - Four timer/counters of type 0, four of type 1
  - 32-bit timer/counter support by cascading two timer/counters
  - Up to four compare or capture (CC) channels
    - Four CC channels for timer/counters of type 0
    - Two CC channels for timer/counters of type 1
  - Waveform generation:
    - Frequency generation
    - Single and dual slope PWM
  - Input capture:
    - Input capture with noise canceling
    - Frequency capture
    - Pulse width capture
    - 32-bit input capture
  - Timer overflow and error interrupt events
  - High-resolution extension
    - Increases frequency and waveform resolution by 4x (2-bit) or 8x (3-bit)
TC2 Time/Counter Type 2
- Eight eight-bit timer/counters
- Four low-byte and four high-byte timer/counters
- Up to eight compare channels in each timer/counter 2
- Four compare channels for both low-byte and high-byte timer/counter
- Waveform generation
  - Single slope pulse width modulation
  - Timer underflow interrupts/events
  - One compare match interrupt/event per compare channel for the low-byte timer/counter
- Can be used to trigger DMA transactions
64A4U Overview

- TWI Two-Wire Interface (I2C)
  - Four identical two-wire interface peripherals
  - Bidirectional two-wire communication interface
  - Phillips I2C and SMBus compatible
  - Bus master or slave operation
    - Slave operation
    - Single bus master operation
    - Bus master in multi-master bus environment
    - Multi-master arbitration
  - Flexible slave address match functions
    - 7-bit, 10-bit and general call address recognition in hardware
  - Slave can operate in all sleep modes, including power-down
  - Slave address match can wake device from all sleep modes, including power-down
  - 100kHz and 400kHz bus frequency
  - Slew-rate limited output drivers
  - Input filter for bus noise and spike suppression
  - Supports arbitration between start repeated start and data bit (SMBus)
  - Slave arbitration allows support for address resolve protocol (SMBus)
64A4U Overview

- SPI Serial Peripheral Interface
  - Four identical SPI peripherals
  - Full-duplex, three-wire synchronous data transfer
  - Master or slave operation
  - LSB first or MSB first data transfer
  - Eight programmable bit rates
  - Interrupt flag at the end of transmission
  - Write collision flag to indicate data collision
  - Wake up from idle sleep mode
  - Double speed master mode
64A4U Overview

- **USART**
  - Eight identical USART peripherals
  - Full-duplex operation
  - Asynchronous or synchronous operation
  - Supports serial frames with 5, 6, 7, 8, or 9 data bits and 1 or 2 stop bits
  - Fractional baud rate generator
  - Built-in error detection and correction schemes
    - Odd or even parity generation and parity check
    - Data overrun and framing error detection
    - Noise filtering includes false start bit detection and digital low-pass filter
  - Separate interrupts for: TX complete, TX data register empty, RX complete
  - Master SPI mode with clock of one half peripheral frequency
  - IRCOM module for IrDA 1.4 with baud rates to 115.2Kbps
64A4U Overview

- RTC 16-bit Real-Time Counter

Figure 20-1. Real-time counter overview.
64A4U Overview

- RTC 16-bit Real-Time Counter
  - 16-bit resolution
  - Selectable clock sources
    - 32.768kHz external crystal
    - External clock
    - 32.768kHz internal oscillator
    - 32kHz internal ULP oscillator
  - Programmable 10-bit clock prescaling
  - One compare register
  - One period register
  - Clear counter on period overflow
  - Optional interrupt/event on overflow and compare match
ADC  12-bit Analog to Digital Converter
64A4U Overview

- **ADC 12-bit Analog to Digital Converter**
  - Two 12-bit ADCs and up to two mega samples per second
  - Two inputs can be sampled simultaneously with 1x gain stage
  - Down to 2.5s conversion time with 8-bit resolution
  - Down to 3.5s conversion time with 12-bit resolution
- **Differential and single-ended input**
  - Up to 16 single-ended inputs
  - 16x4 differential inputs without gain, 8x4 differential input with gain
  - Internal differential amp has gain options of: 1/2x, 1x, 2x, 4x, 8x, 16x, 32x, and 64x
- **Single, continuous and scan conversion options**
- **Four internal inputs**
  - Internal temperature sensor
  - DAC output
  - AVCC voltage divided by 10
  - 1.1V bandgap voltage
  - Internal and external reference options
- **Optional DMA transfer of conversion results**
- **Optional interrupt/event on compare result**
64A4U Overview

- DAC 12-bit Digital to Analog Converter
64A4U Overview

- DAC 12-bit Digital to Analog Converter
  - Two 12-bit DACs with independent, continuous-drive output channels
  - Up to one million samples per second conversion rate per DAC channel
  - Built-in calibration removes offset error and gain error
  - High output drive for resistive and capacitive loads
  - Internal and external reference options
  - DAC output available as input to analog comparator and ADC
  - Low-power mode, with reduced drive strength
  - Optional DMA transfer of data
64A4U Overview

- Analog Comparator

- Two Analog Comparators
- Selectable hysteresis: none, small, large
- Analog comparator output available on pin
- Flexible input selection
  - All pins on the port
  - Output from the DAC
  - Bandgap reference voltage
  - 64-level programmable voltage scaler of the internal AVCC voltage
- Interrupt and event generation on rising, falling edge or toggle
- Constant current source with configurable output pin selection