

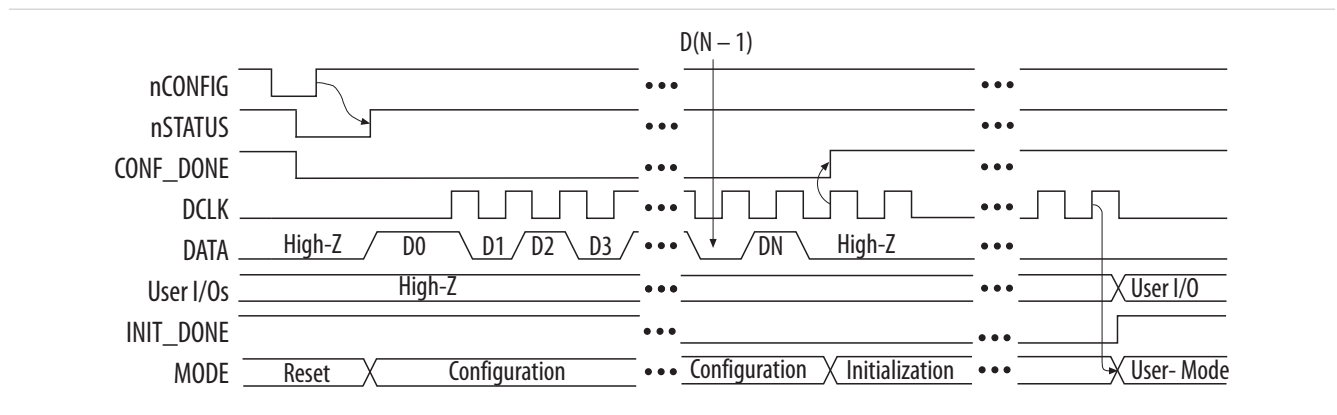


This document describes the types of configuration schemes for Altera® FPGAs

Device Configuration Overview for Passive Schemes

During device operation, Altera FPGAs store configuration data in SRAM cells. Because SRAM memory is volatile, the SRAM cells must be loaded with configuration data each time the device powers up. After the device is configured, its registers and I/O pins must be initialized. After initialization, the device enters user mode for in-system operation.

Figure 1: Configuration Cycle Waveform



The low-to-high transition of `nCONFIG` on the FPGA begins the configuration cycle. The configuration cycle consists of 3 stages—reset, configuration, and initialization. While `nCONFIG` is low, the device is in reset. When the device comes out of reset, `nCONFIG` must be at a logic high level in order for the device to release the open-drain `nSTATUS` pin. After `nSTATUS` is released, it is pulled high by a pull-up resistor and the FPGA is ready to receive configuration data. Before and during configuration, all user I/O pins are tri-stated. Stratix® series, Arria® series, and Cyclone® series have weak pull-up resistors on the I/O pins which are on, before and during configuration.

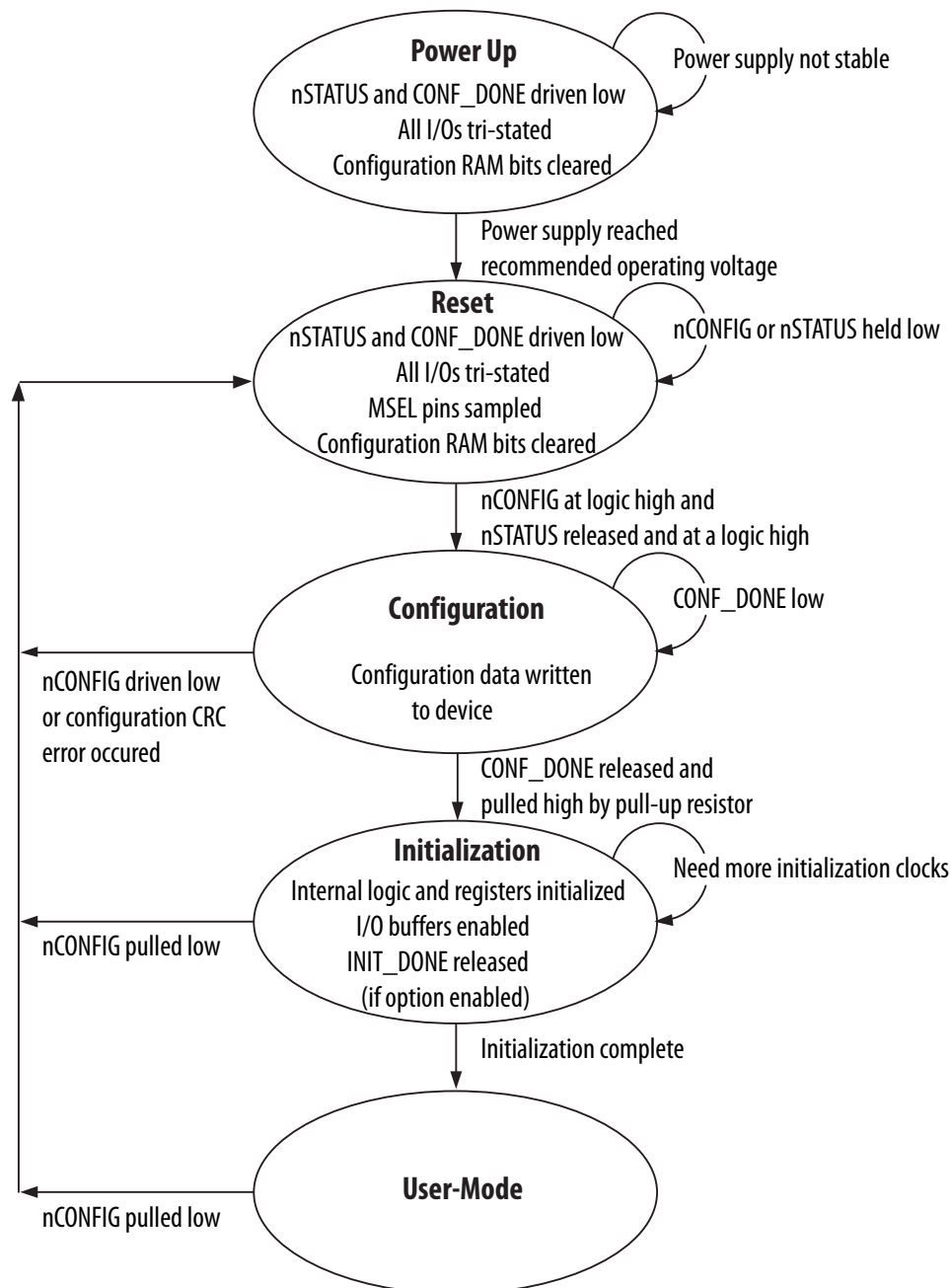
To begin configuration, `nCONFIG` and `nSTATUS` must be at a logic high level. You can delay configuration by holding the `nCONFIG` low. The device receives configuration data on its `DATA0` pins. Configuration data is latched into the FPGA on the rising edge of `DCLK`. After the FPGA has received all configuration data successfully, it releases the `CONF_DONE` pin, which is pulled high by a pull-up resistor. A low to high transition on `CONF_DONE` indicates configuration is complete and initialization of the device can begin.

An optional `INIT_DONE` pin is available, which signals the end of initialization and the start of user mode. During initialization, internal logic and I/O registers are initialized and I/O buffers are enabled. When

initialization is finished, the `INIT_DONE` pin is released and pulled high by an external pull-up resistor. After entering user mode, the user I/O pins will no longer have a weak pull up and will function as assigned in your design. After configuration, you must not leave the `DATA0` pins floating. Drive the pin high or low, whichever is convenient, on your board.

You can initiate a reconfiguration by toggling the `nCONFIG` pin from high to low and then back to high. When `nCONFIG` is pulled low, `nSTATUS` and `CONF_DONE` are also pulled low and all I/O pins are tri-stated. After `nCONFIG` and `nSTATUS` return to a logic high level, configuration begins.

Figure 2: Configuration Cycle State Machine



Selecting a Configuration Scheme

You can load the configuration data for Altera devices using an active, passive, or JTAG configuration scheme. When using an active configuration scheme with a serial configuration (EPCS) or quad-serial configuration (EPCQ) device, the target FPGA generates the control and synchronization signals. When both devices are ready to begin configuration, the EPCS or EPCQ device sends data to the FPGA.

When you use any passive configuration scheme, the Altera device is incorporated into a system with an Altera configuration device or an intelligent host, such as a microprocessor, that controls the configuration process. The configuration device or host supplies configuration data from a storage device such as a configuration device, a hard disk, RAM, or other system memory. When you use passive configuration scheme, you can change the target device's functionality while the system is in operation by reconfiguring it.

Altera devices support a number of configuration schemes. After you have decided on the appropriate configuration scheme for your system, you need to drive the dedicated mode select control pins, `MSEL`, of the FPGA to set the configuration mode.

Note: For more information about how to set the `MSEL` pins for your target device, refer to the configuration chapter in the appropriate device handbook.

Active Serial Configuration

You can perform an active serial (AS) configuration using EPCS or EPCQ devices. During AS configuration, the FPGA device is the master and the EPCS or EPCQ device is the slave. Configuration data is transferred one bit per clock cycle.

Passive Serial Configuration

You can perform a passive serial (PS) configuration using an Altera download cable, an Altera configuration device, or an intelligent host, such as a microprocessor. During PS configuration, configuration data is transferred from a storage device, such as a configuration device or flash memory, to the FPGA on the `DATA0` pin. This configuration data is latched into the FPGA on the rising edge of `DCLK`. Configuration data is transferred one bit per clock cycle.

Fast Passive Parallel Configuration

You can perform a fast passive parallel (FPP) configuration using an Altera configuration device or an intelligent host, such as a microprocessor. During FPP configuration, configuration data is transferred from a storage device, such as a configuration device or flash memory, to the FPGA on the `DATA[7..0]` pins. This configuration data is latched into the FPGA on the rising edge of `DCLK`. Configuration data is transferred one byte per clock cycle.

JTAG Configuration

You can perform a JTAG configuration using an Altera download cable or an intelligent host, such as a microprocessor. JTAG configuration uses the IEEE Std 1149.1 JTAG interface pins and supports the Jam™ Standard Test and Programming Language (STAPL) standard.

Document Revision History

Date	Version	Changes
December 2014	2014.12.15	Updated Configuration Cycle Waveform figure.
September 2014	3.2	Added EPCQ device support.
August 2012	3.1	Updated Figure 1.
January 2012	3.0	Reorganizing the content for this document.
October 2008	2.2	<ul style="list-style-type: none">• Updated Table 1-1 and Table 1-2.• Updated Figure 1-2.• Updated “Introduction”, “Device Configuration Overview for Passive Schemes”, and “Selecting a Configuration Scheme” sections.• Added “Active Parallel Configuration” and “Document Revision History” sections.