ECE 474 - Quiz 1 - Spring 2015

Name and last 4 of ID: _____

1. [30] Give three advantages of using an HDL.
   increased productivity, code reuse, automatic documentation, vendor/technology independence, complexity hiding, abstraction is easy, use of logic synthesis, can use code development tools, easy to try alternative approaches, languages used are standards.

2. [10] When vlog is invoked on an rtl-level file such as fadder.sv, what input file is necessary?
   only the rtl file name is necessary such as "fadder.sv".

3. [10] What does vlog produce when invoked on a file such as fadder.sv?
   vlog produces an executable imagae of the design, in the /work directory, that vsim can invoke on.

4. [15] Name three things that our simulation "do file" did for you.
   among other things...list the signals, display them on a waveform viewer, apply inputs to pins, advance simulation time, quit the simulator

5. [15] What was the difference between the contents of the files fadder.sv and fadder.gate.v? Be specific.
   fadder.sv contained a behaviorial description of the design. fadder.gate.sv contained a gate-level realization of the design, post synthesis.

6. [10] Why is writing synthesizable HDL code different to writing an algorithm for any other language?
   Writing HDL code is actually describing a inherrently parallel hardware structure, not an algorithm for sequential execution on a processor.

7. [10] Upon what entity do you invoke the simulator upon?
   The module name, in our case, "fadder", with no file suffix

8. [2] What concept or step was unclear to you in these first two lectures?