ECE 474 - Quiz 2 - Spring 2015

Name and last 4 of ID: _____

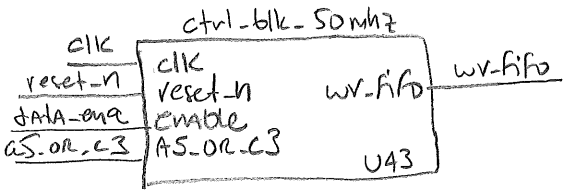
1. [30] Name two differences between a design modeled in Verilog at the behavioral level versus Verilog at the RTL level.
   Behavioral: no timing implied, no structure implied, no implementation implied, no internal wires or signals are defined
   RTL: clock period accurate timing, structure implied, implementation defined, wires and internal signals are defined

2. [10] Name two differences between a design modeled in Verilog at the RTL level versus Verilog at the gate level.
   RTL: no gates are used, no gate delays are included; gate level description has both of these

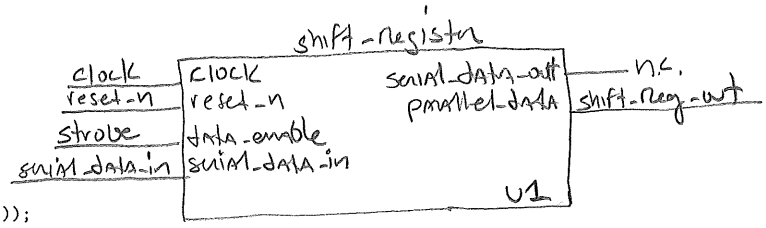
3. [10] What is the most powerful argument for not coding a design in Verilog at the gate level.
   It's too low of a level of abstraction. Thus you have poor productivity.

4. [15] For the following code snippets, draw the block diagram showing the module, its pins, and the wires connected to it with their names.

```
ctrl_blk_50mhz U43 (
  .clk       (clk_50),
  .reset_n   (reset_n),
  .enable    (data_ena),
  .a5_or_c3  (a5_or_c3),
  .wr_fifo   (wr_fifo));
```




```
shift_register U1 (
  .clock,
  .reset_n,
  .data_enable     (strobe),
  .serial_data_in,
  .serial_data_out (      ),
  .parallel_data   (shift_reg_out));
```



5. [15] How does a repeatedly instantiated Verilog module in an IC differ from object code in a program created by a C function that is called repeatedly.
   A Verilog module that is instantiated repeatedly will result in multiple gate implementations of the function, whereas a C function call is compiled to one copy of object code that is reused by every call of the function.

6. [2] What concept or step was unclear to you in these first two lectures?