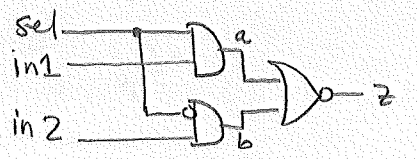
ECE 474 - Quiz 3 - Spring 2015

Name and last 4 of ID: Key

1. [70] Draw a correct gate realization for the following code snippets.

```
module one(
  input in1, in2, sel,
  output z
  );
  wire a,b;
  assign z = ~(a | b);
  assign a = in1 &  sel;
  assign b = in2 & ~sel;
endmodule
```



An inverting MUX

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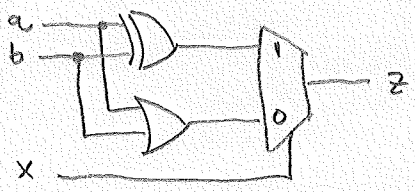
```
module two(
  input       a, b, x,
  output reg  z
  );
  always_comb
    if (x)
      z = a ^ b;
    else
      z = a | b;
endmodule
```



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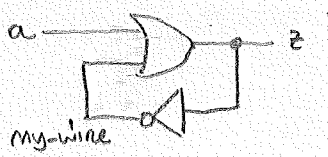
2. [20] What is wrong with the code here? It compiles without error. Explain what would happen.

```
module three(
  input       a,
  output reg  z
  );
  wire my_wire;       //declare an internal wire
  assign z = a | my_wire;
  assign my_wire = ~z;
endmodule
```



When "a" goes low during simulation, an oscillation is formed, causing the simulator to issue a warning about the iteration limit (delta cycles)

3. [10] Complete this saying: "`If` without `else` gives a latch".
4. [2] What was unclear to you in this last week's lecture or lab?