# **Digital Standard Cell Library**

## SAED\_EDK90\_CORE

## DATABOOK



Revision: 1.4Technology: SAED90nmProcess: SAED90nm 1P9M 1.2v / 2.5v

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### 1. Introduction

This Databook describes possibilities, peculiarities of SAED\_EDK90\_CORE Digital Standard Cell Library and technical parameters of separate cells included in it. The library is free from intellectual property restrictions. It is one of the components of SAED\_EDK90 Educational Design Kit (EDK). SAED\_EDK90 EDK is anticipated for the use of educational purposes aimed at training highly qualified specialists in the area of microelectronics in:

- SYNOPSYS Customer Education Services
- Universities included in SYNOPSYS University Program

SAED\_EDK90 is foreseen to support the trainees to better master:

- Advanced design methodologies
- Capabilities of SYNOPSYS tools.

For the use of EDK it is assumed that European or North American bundle of SYNOPSYS EDA tools is available to trainees.

SAED\_EDK90\_CORE Digital Standard Cell Library is anticipated for designing different integrated circuits (ICs) by the application of 90nm technology and SYNOPSYS EDA tools.

The SAED\_EDK90\_CORE Digital Standard Cell Library has been built using SAED90nm 1P9M 1.2V/2.5V design rules. The library has been created aimed at optimizing the main characteristics of designed ICs by its help. The library includes typical miscellaneous combinational and sequential logic cells for different drive strengths. Besides, the library contains all the cells which are required for different styles of low power (multi-voltage, multi-threshold) designs (www.synopsys.com/products/power/multivoltage\_bkgrd.pdf, www.synopsys.com/sps/pdf/optimum\_sleep\_transistor\_vlsi\_dat06.pdf). Those are the following: Isolation Cells, Level Shifters, Retention Flip-Flops, Always-on Buffers and Power Gating Cells. The presence of all these cells provides the support of IC design with different core voltages to minimize dynamic and leakage power.

### 2. General Information

The used symbols of logic elements' states are shown in Table 2.1.

Symbol	State	
L ("0")	LOW Logic Level	
H ("1")	HIGH Logic Level	
Z	High-impedance State	
LH ("0"→"1")	LOW to HIGH Transition	
HL ("1"→"0")	HIGH to LOW Transition	
Х	Either HIGH or LOW Logic Level	

Table 2.1. Symbols of logic elements' states

DC parameters and measurement conditions of the elements included in SAED\_EDK90\_CORE Digital Standard Cell Library are shown in Table 2.2.

No	Parameter	Unit	Symbol	Figure	Definition
1	Voltage Transfer Characteristic	-	VTC		DC functional dependence between input and output voltages.
2	Output high level voltage (nominal)	V	V <sub>OHN</sub> =V <sub>DD</sub>		Output high voltage at nominal condition, usually equals to V <sub>DD</sub>
3	Output low level voltage (nominal)	V	V <sub>OLN</sub> =0 (V <sub>OLN</sub> =V <sub>SS</sub> )		Output low voltage at nominal condition, usually V <sub>OLN</sub> =0
4	Switching point voltage	V	V <sub>SP</sub>	V <sub>DD</sub> V <sub>DD</sub> V <sub>SP</sub> V <sub>SP</sub> V <sub>IN</sub>	Point on VTC where V <sub>OUT</sub> =V <sub>IN</sub>
5	Output high level minimum voltage	V	V <sub>OHMIN</sub>	VOUT VDD VOHMIN 0 VDD VOHMIN	Highest output voltage at slope= -1.

Table 2.2. DC Parameters and measurement conditions of	digital cells
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No	Parameter	Unit	Symbol	Figure	Definition
6	Output low level maximum voltage	V	V <sub>olmax</sub>	V <sub>OUT</sub> V <sub>DD</sub> V <sub>OLMAX</sub> V <sub>OLMAX</sub>	Lowest output voltage at slope= -1
7	Input minimum high voltage	V	V <sub>IHMIN</sub>	V <sub>DD</sub> V <sub>DD</sub> V <sub>OMAX</sub> 0 V <sub>IHMIN</sub> V <sub>DD</sub> V <sub>IN</sub>	Highest input voltage at slope = -1
8	Input maximum low voltage	V	V <sub>ILMAX</sub>	VOUT VDD OHMIN 0 VILMAX VDD VIN	Lowest input voltage at slope = -1
9	High state noise margin	V	NMH= =V <sub>OHMIN</sub> - V <sub>IHMIN</sub>	Voltage	The maximum input noise voltage which does not change the output state when its value is subtracted from the input high level voltage
10	Low state noise margin	V	NML= =V <sub>ILMAX</sub> - V <sub>OLMAX</sub>	Voltage	The maximum input noise voltage which does not change the output state when added to the input low level voltage
	Static leakage current	uA	I <sub>LEAKH</sub>	None	The current consumed when the output is high
11	consumption at output on high state	uA	I <sub>LEAKL</sub>	None	I he current consumed when the output is low
12	Leakage power consumption	pW	P <sub>LEAKH</sub> = =V <sub>DD</sub> x I <sub>LEAKH</sub>	None	The power consumed when the output is high
12	(dissipation) at output	pW	P <sub>LEAKL</sub> = =V <sub>DD</sub> x I <sub>LEAKL</sub>	None	The power consumed when the output is low

AC parameters and measurement conditions of the elements included in SAED\_EDK90\_CORE Digital Standard Cell Library are shown in Table 2.3.

No	Parameter	Unit	Symbol	Figure	Definition
1	Rise transition time	ns	t <sub>R</sub>	$V_{DD}$ $V_{DD}$ $V_{DD}$ $V_{SS}$ $t_{R}$	The time it takes a driving pin to make a transition from $kV_{DD}$ to $(1-k)V_{DD}$ value. Usually k=0.1 (also possible k=0.2, 0.3, etc)
2	Fall transition time	ns	t <sub>F</sub>		The time it takes a driving pin to make a transition from $(1-k)V_{DD}$ to $kV_{DD}$ value. Usually k=0.1 (also possible k=0.2, 0.3, etc)
3	Propagation delay low-to-high (Rise propagation)	ns	t <sub>PLH</sub> (t <sub>PR</sub> )		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.5V_{DD}$ when the output signal is changing from low to high
4	Propagation delay high-to-low (Fall propagation)	ns	t <sub>PHL</sub> (t <sub>PF</sub> )		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.5V_{DD}$ when the output signal is changing from high to low
5	Average supply current	uA	$I_{V_{DD}AVG} = {\stackrel{T}{_{0}}} I_{V_{DD}}(t)dt$	None	The power supply current average value for a period (T)
6	Supply peak current	uA	$I_{VDDPEAK} =$ =max( $I_{VDD}(t)$ ) $t \in [0;T]$	None	The peak value of power supply current within one period (T)
7	Dynamic power dissipation	рW	P <sub>DISDYN</sub> = =I <sub>VDDAVG</sub> x V <sub>DD</sub>	None	The average power consumed from the power supply
8	Power-delay product	nJ	PD=P <sub>DISDYN</sub> x x max (t <sub>PHL</sub> ,t <sub>PLH</sub> )	None	The product of consumed power and the largest propagation delay
9	Energy-delay product	nJs	ED=PD x x max(t <sub>PHL</sub> ,t <sub>PLH</sub> )	None	The product of PD and the largest propagation delay

Table 2.3.	AC P	arameters	and	measurement	conditions	of digital	cells
Table 2.3.	AC F	alameters	anu	measurement	CONDITIONS	ul ulyilai	CEII2

No	Parameter	Unit	Symbol	Figure	Definition
10	Switching fall power	nJ	$P_{SWF} =$ $= (C_{LOAD} + C_{OUT}$ $F) X$ $X V_{DD}^{2}/2$	None	The energy dissipated on a fall transition. ( $C_{OUTF}$ is the output fall capacitance)
11	Switching rise power	nJ	$P_{SWR} = (C_{LOAD} + C_{OUT})$ $R \times C_{DD}^{2}/2$	None	The energy dissipated on a rise transition. $(C_{OUTR}$ is the output rise capacitance)
12	Minimum clock pulse (only for flip- flops or latches)	ns	t <sub>PWH</sub> (t <sub>PWL</sub> )		The time interval during which the clock signal is high or low, so that it ensures proper operation of a flip-flop or a latch
13	Setup time (only for flip- flops or latches)	ns	t <sub>su</sub>	0.5V <sub>DD</sub> DATA 0.5Vbb CLOCK	The minimum period in which the input data to a flip-flop or a latch must be stable before the active edge of the clock occurs
14	Hold time (only for flip- flops or latches)	ns	t <sub>H</sub>		The minimum period in which the input data to a flip-flop or a latch must remain stable after the active edge of the clock has occurred
15	Clock-to- output time (only for flip- flops or latches)	ns	t <sub>clkq</sub>		The amount of time that takes the output signal to change after clock's active edge is applied
16	Removal time (only for flip- flops or latches with asynchronous Set or Reset).	ns	t <sub>REM</sub>	SET (RESET) 0.5VDD CLOCK	The minimum time in which the asynchronous Set or Reset pin to a flip-flop or latch must remain enabled after the active edge of the clock has occurred
17	Recovery time (only for flip- flops and latches with asynchronous Set or Reset)	ns	t <sub>REC</sub>	0.5V <sub>DD</sub> SET (R <u>ESET)</u> CLOCK 0.5V <sub>DD</sub>	The minimum time in which Set or Reset must be held stable after being deasserted before next active edge of the clock occurs
18	From high to Z-state entry time, (only for tri-state output cells)	ns	t <sub>HZ</sub>	None	The amount of time that takes the output to change from high to Z-state after control signal is applied

## SYNOPSYS

No	Parameter	Unit	Symbol	Figure	Definition
19	From low to Z- state entry time, (only for tri-state output cells)	ns	t <sub>LZ</sub>	None	The amount of time that takes the output to change from low to Z-state after control signal is applied
20	From Z to high-state exit time (only for tri- state output cells)	ns	t <sub>zH</sub>	None	The amount of time that takes the output to change from Z to high-state after control signal is applied
21	From Z to low- state exit time (only for tri- state output cells)	ns	t <sub>zL</sub>	None	The amount of time that takes the output to change from Z to low-state after control signal is applied
22	Input pin capacitance	pF	C <sub>IN</sub>	None	Defines the load of an output pin
23	Maximum capacitance	pF	C <sub>MAX</sub>	None	Defines the maximum total capacitive load that an output pin can drive

### 3. Operating conditions

SAED\_EDK90\_CORE Digital Standard Cell Library is anticipated for 1.2V operation. The used process technology is SAED90nm 1P9M 1.2V/2.5V, but only the 1P1M option is used.

The operating conditions of SAED\_EDK90\_CORE Digital Standard Cell Library are shown in Table 3.1.

Table 3.1. C	perating	conditions
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Parameter	Min	Тур	Max	Units
Power Supply (VDD) range	0.7	1.2	1.32	V
Operating Temperature range	-40	+25	+125	°C
Operating Frequency (F)	-	300	-	MHz

### 4. Input signal slope, standard load and drive strengths

Standard load ( $C_{sl}$ ) has been selected as the input pin capacitance of INVX1 cell. The INVX1 cell itself is tuned to drive 4 loads.

Drive Strength	Cell Load
X0	0.5x C <sub>sl</sub>
X1	1x C <sub>sl</sub>
X2	2x C <sub>sl</sub>
X3	3x C <sub>sl</sub>
X4	4x C <sub>sl</sub>
X8	8x C <sub>sl</sub>
X12	12x C <sub>sl</sub>
X16	16x C <sub>sl</sub>
X24	24x C <sub>sl</sub>
X32	32x C <sub>sl</sub>

Table 4.1. Definition of drive strength

### **5. AC Characteristics**

### **5.1.** Characterization corners

Composite Current Source (CCS) modeling technology has been applied for characterization to meet the contemporary methods of low power design. The application of that technology supports timing, noise, and power analyses simultaneously with consideration of the relevant nanometer dependencies. It allows meeting the requirements of variation-aware analysis. The characterization results are given for 12 process/voltage/temperature (PVT) conditions shown in Table 5.1.

Corner Name	Process (NMOS proc. – PMOS proc.)	Temperature ( <sup>0</sup> C)	Power Supply (V)	Notes
TTNT1p20v	Typical - Typical	25	1.2	Typical corner
TTHT1p20v	Typical - Typical	125	1.2	Typical corner
TTLT1p20v	Typical - Typical	-40	1.2	Typical corner
SSNT1p08v	Slow - Slow	25	1.08	Slow corner
SSHT1p08v	Slow - Slow	125	1.08	Slow corner
SSLT1p08v	Slow - Slow	-40	1.08	Slow corner
FFNT1p32v	Fast - Fast	25	1.32	Fast corner
FFHT1p32v	Fast - Fast	125	1.32	Fast corner
FFLT1p32v	Fast - Fast	-40	1.32	Fast corner
	Low Voltage (	Operating Cond	litions	
TTNT0p08v	Typical - Typical	25	0.8	Typical corner
TTHT0p08v	Typical - Typical	125	0.8	Typical corner
TTLT0p08v	Typical - Typical	-40	0.8	Typical corner
SSNT0p07v	Slow - Slow	25	0.7	Slow corner
SSHT0p07v	Slow - Slow	125	0.7	Slow corner
SSLT0p07v	Slow - Slow	-40	0.7	Slow corner
FFNT0p09v	Fast - Fast	25	0.9	Fast corner
FFHT0p09v	Fast - Fast	125	0.9	Fast corner
FFLT0p09v	Fast - Fast	-40	0.9	Fast corner

Functionality has also been checked at the following additional simulation corners:

Corner	Process	Temperature	Power
Name	(NMOS proc. – PMOS proc.)	( <sup>0</sup> C)	Supply (V)
FSHT1p08v	Fast - Slow	125	1.08
FSLT1p08v	Fast - Slow	-40	1.08
FSHT1p32v	Fast - Slow	125	1.32
FSLT1p32v	Fast - Slow	-40	1.32
SFHT1p08v	Slow - Fast	125	1.08
SFLT1p08v	Slow - Fast	-40	1.08
SFHT1p32v	Slow - Fast	125	1.32
SFLT1p32v	Slow - Fast	-40	1.32
	Low Voltage Operating Co	onditions	
FSHT0p70v	Fast - Slow	125	0.7
FSLT0p70v	Fast - Slow	-40	0.7
FSHT0p90v	Fast - Slow	125	0.9
FSLT0p90v	Fast - Slow	-40	0.9
SFHT0p70v	Slow - Fast	125	0.7
SFLT0p70v	Slow - Fast	-40	0.7
SFHT0p90v	Slow - Fast	125	0.9
SFLT0p90v	Slow - Fast	-40	0.9

#### Table 5.2. Additional simulation corners

### 5.2. The values of Output Load and Input Slope

Characterization has been realized for 7 different values of Output Load and 7 different values of Input Slope shown in Table 5.3.

Table 5.3.	The values	used for	characterization
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Parameter		Value					
Output Load	0	0.5*C <sub>sl</sub>	1*C <sub>sl</sub>	2*C <sub>sl</sub>	4*C <sub>sl</sub>	8*C <sub>sl</sub>	16*C <sub>sl</sub>
Input Slope (ns)	0.2*T <sub>isl</sub>	0.4*T <sub>isl</sub>	0.8*T <sub>isl</sub>	1.6*T <sub>isl</sub>	3.2*T <sub>isl</sub>	6.4*T <sub>isl</sub>	12.8*T <sub>isl</sub>

The calculation of Setup/Hold times has been realized for 3 different values of Data and Input Slopes shown in Table 5.4.

Table 5.4. The used values for calculating Setup/Hold Times

Parameter	Slope Values (ns)		
Data Input Slope	0.5*T <sub>isl</sub>	1*T <sub>isl</sub>	5*T <sub>isl</sub>
Clock Input Slope	0.5*T <sub>isl</sub>	1*T <sub>isl</sub>	5*T <sub>isl</sub>

### 6. Digital Standard Library Cells List

SAED\_EDK90\_CORE Digital Standard Cell Library contains 249 cells in total, the list of which is shown in Table 6.1.

Table 6.1. Digital Standard Library Cells List

No	Cell Description	Cell Name
	Inverters, Buffers	
1	Inverter	INVX0
2	Inverter	INVX1
3	Inverter	INVX2
4	Inverter	INVX4
5	Inverter	INVX8
6	Inverter	INVX16
7	Inverter	INVX32
8	Inverting Buffer	IBUFFX2
9	Inverting Buffer	IBUFFX4
10	Inverting Buffer	IBUFFX8
11	Inverting Buffer	IBUFFX16
12	Inverting Buffer	IBUFFX32
13	Non-inverting Buffer	NBUFFX2
14	Non-inverting Buffer	NBUFFX4
15	Non-inverting Buffer	NBUFFX8
16	Non-inverting Buffer	NBUFFX16
17	Non-inverting Buffer	NBUFFX32
18	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX1

19         Tri-state Non-inverting Buffer w/ High-Active Enable         TNBUFFX2           20         Tri-state Non-inverting Buffer w/ High-Active Enable         TNBUFFX4           21         Tri-state Non-inverting Buffer w/ High-Active Enable         TNBUFFX16           23         Tri-state Non-inverting Buffer w/ High-Active Enable         TNBUFFX32           Logic Gates	No	Cell Description	Cell Name
20         Tri-state Non-inverting Buffer w/ High-Active Enable         TNBUFFX4           21         Tri-state Non-inverting Buffer w/ High-Active Enable         TNBUFFX6           23         Tri-state Non-inverting Buffer w/ High-Active Enable         TNBUFFX6           24         AND 2-input         AND2X1           25         AND 2-input         AND2X2           26         AND 2-input         AND2X2           27         AND 3-input         AND2X2           28         AND 3-input         AND3X2           29         AND 3-input         AND3X2           29         AND 3-input         AND3X2           20         AND 4-input         AND3X4           30         AND 4-input         AND4X2           31         AND 2-input         AND4X2           32         AND 4-input         AND4X4           33         NAND 2-input         NAND2X2           34         NAND 2-input         NAND2X2           35         NAND 2-input         NAND2X4           36         NAND 2-input         NAND2X4           37         NAND 2-input         NAND2X4           38         NAND 3-input         NAND3X4           39         NAND 3-input	19	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX2
21     Tri-state Non-inverting Buffer w/ High-Active Enable     TNBUFFX8       22     Tri-state Non-inverting Buffer w/ High-Active Enable     TNBUFFX32       24     AND 2-input     AND2X1       25     AND 2-input     AND2X4       26     AND 2-input     AND2X4       27     AND 3-input     AND2X4       28     AND 3-input     AND3X1       29     AND 3-input     AND3X2       20     AND 4-input     AND3X2       30     AND 4-input     AND4X1       31     AND 4-input     AND4X2       30     AND 4-input     AND4X2       31     AND 2-input     AND4X2       32     AND 4-input     AND4X2       34     NAND 2-input     NAND2X1       35     NAND 2-input     NAND2X2       36     NAND 2-input     NAND2X2       37     NAND 2-input     NAND2X2       38     NAND 2-input     NAND3X2       39     NAND 2-input     NAND3X2       31     NAND 2-input     NAND3X2       38     NAND 2-input     NAND3X2       39     NAND 2-input     NAND3X2       30     NAND 3-input     NAND3X2       31     NAND 3-input     NAND3X2       34     NAND	20	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX4
22         Tri-state Non-inverting Buffer w/ High-Active Enable         TNBUFFX16           23         Tri-state Non-inverting Buffer w/ High-Active Enable         TNBUFFX32           24         AND 2-input         AND2X1           25         AND 2-input         AND2X2           26         AND 2-input         AND2X2           27         AND 3-input         AND3X2           28         AND 3-input         AND3X2           29         AND 4-input         AND3X2           30         AND 4-input         AND3X2           31         AND 4-input         AND4X4           32         AND 4-input         AND4X4           33         NAND 2-input         AND4X4           34         NAND 2-input         NAND2X1           35         NAND 2-input         NAND2X3           36         NAND 2-input         NAND2X4           37         NAND 3-input         NAND2X4           38         NAND 3-input         NAND3X3           38         NAND 3-input         NAND3X3           39         NAND 3-input         NAND3X4           39         NAND 3-input         NAND3X4           30         NAND 3-input         NAND3X4      <	21	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX8
23         Tri-state Non-inverting Buffer w/ High-Active Enable         TNBUFFX32           Logic Gates         AND 2-input         AND2X1           24         AND 2-input         AND2X1           25         AND 2-input         AND2X2           26         AND 2-input         AND3X1           28         AND 3-input         AND3X2           29         AND 3-input         AND3X2           29         AND 3-input         AND3X2           30         AND 4-input         AND4X2           30         AND 4-input         AND4X2           31         AND 2-input         AND4X2           32         AND 2-input         NAND2X2           34         NAND 2-input         NAND2X2           35         NAND 2-input         NAND2X2           36         NAND 2-input         NAND2X2           37         NAND 3-input         NAND3X2           38         NAND 3-input         NAND3X1           39         NAND 3-input         NAND3X2           40         NAND 3-input         NAND3X2           41         NAND 3-input         NAND3X2           42         NAND 3-input         NAND3X2           43 <td< td=""><td>22</td><td>Tri-state Non-inverting Buffer w/ High-Active Enable</td><td>TNBUFFX16</td></td<>	22	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX16
Logic GatesAND 2-inputAND2X124AND 2-inputAND2X226AND 2-inputAND2X226AND 3-inputAND3X127AND 3-inputAND3X129AND 3-inputAND3X229AND 4-inputAND3X430AND 4-inputAND4X231AND 4-inputAND4X233NAND 2-inputAND4X234NAND 2-inputNAND2X135NAND 2-inputNAND2X136NAND 2-inputNAND2X237NAND 2-inputNAND2X238NAND 2-inputNAND2X239NAND 3-inputNAND2X230NAND 3-inputNAND2X431NAND 3-inputNAND3X232NAND 3-inputNAND3X234NAND 3-inputNAND3X235NAND 3-inputNAND3X240NAND 3-inputNAND3X241NAND 4-inputNAND3X242NAND 4-inputNAND3X443OR 2-inputOR2X444OR 2-inputOR2X445OR 2-inputOR3X248OR 3-inputOR3X449OR 4-inputOR4X450OR 4-inputOR4X451OR 2-inputOR4X452NOR 2-inputOR3X453NOR 2-inputOR3X454NOR 2-inputNOR2X555NOR 2-inputNOR3X656NOR 3-inputNOR3X657NOR 3-input<	23	Tri-state Non-inverting Buffer w/ High-Active Enable	TNBUFFX32
24         AND 2-input         AND2X1           25         AND 2-input         AND2X2           26         AND 3-input         AND3X1           27         AND 3-input         AND3X2           28         AND 3-input         AND3X1           28         AND 3-input         AND3X2           29         AND 3-input         AND3X2           20         AND 4-input         AND4X3           31         AND 4-input         AND4X2           32         AND 4-input         AND4X3           31         AND 2-input         AND4X3           32         AND 2-input         NAND2X3           34         NAND 2-input         NAND2X3           35         NAND 2-input         NAND2X4           36         NAND 2-input         NAND2X3           37         NAND 3-input         NAND3X3           38         NAND 3-input         NAND3X4           39         NAND 3-input         NAND3X3           39         NAND 3-input         NAND3X4           41         NAND 3-input         NAND3X4           39         NAND 3-input         NAND3X4           41         NAND 4-input         NAND3X4		Logic Gates	
25         AND 2-input         AND2X2           26         AND 3-input         AND3X4           27         AND 3-input         AND3X2           28         AND 3-input         AND3X2           29         AND 3-input         AND3X3           30         AND 4-input         AND4X3           31         AND 4-input         AND4X4           32         AND 2-input         AND4X3           31         NAND 2-input         NAND2X0           34         NAND 2-input         NAND2X1           35         NAND 2-input         NAND2X21           36         NAND 2-input         NAND2X2           36         NAND 2-input         NAND2X2           37         NAND 2-input         NAND2X2           38         NAND 2-input         NAND3X2           37         NAND 3-input         NAND3X2           38         NAND 3-input         NAND3X2           39         NAND 3-input         NAND3X2           40         NAND 4-input         NAND3X2           41         NAND 4-input         NAND4X1           42         NAND 4-input         OR2X4           44         OR 3-input         OR2X2 <td>24</td> <td>AND 2-input</td> <td>AND2X1</td>	24	AND 2-input	AND2X1
26         AND 2-input         AND3X1           27         AND 3-input         AND3X1           28         AND 3-input         AND3X1           29         AND 3-input         AND3X4           30         AND 4-input         AND4X1           31         AND 4-input         AND4X2           31         AND 4-input         AND4X2           32         AND 2-input         AND4X2           33         NAND 2-input         NAND2X0           34         NAND 2-input         NAND2X1           35         NAND 2-input         NAND2X1           36         NAND 2-input         NAND2X2           37         NAND 3-input         NAND3X2           38         NAND 3-input         NAND3X1           39         NAND 3-input         NAND3X2           40         NAND 3-input         NAND3X2           41         NAND 3-input         NAND3X4           42         NAND 4-input         NAND3X4           43         OR 2-input         NAND3X4           44         OR 2-input         OR2X1           45         OR 2-input         OR2X2           46         OR 3-input         OR3X2 <t< td=""><td>25</td><td>AND 2-input</td><td>AND2X2</td></t<>	25	AND 2-input	AND2X2
27         AND 3-input         AND3X1           28         AND 3-input         AND3X2           29         AND 3-input         AND3X4           30         AND 4-input         AND4X1           31         AND 4-input         AND4X2           32         AND 4-input         AND4X2           32         AND 2-input         AND4X2           33         NAND 2-input         NAND2X2           34         NAND 2-input         NAND2X2           35         NAND 2-input         NAND2X2           36         NAND 2-input         NAND2X2           37         NAND 2-input         NAND2X2           38         NAND 2-input         NAND2X2           37         NAND 3-input         NAND3X0           38         NAND 3-input         NAND3X2           40         NAND 3-input         NAND3X2           41         NAND 4-input         NAND3X2           42         NAND 4-input         NAND4X2           43         OR 2-input         OR2X1           44         OR 2-input         OR2X2           45         OR 3-input         OR3X1           47         OR 3-input         OR3X2 <t< td=""><td>26</td><td>AND 2-input</td><td>AND2X4</td></t<>	26	AND 2-input	AND2X4
28AND 3-inputAND3X229AND 3-inputAND3X430AND 4-inputAND4X131AND 4-inputAND4X232AND 4-inputAND4X233NAND 2-inputNAND2X034NAND 2-inputNAND2X135NAND 2-inputNAND2X236NAND 2-inputNAND2X237NAND 3-inputNAND3X038NAND 3-inputNAND3X139NAND 3-inputNAND3X240NAND 3-inputNAND3X241NAND 4-inputNAND3X443OR 2-inputOR2X144OR 2-inputOR2X245OR 2-inputOR2X246OR 3-inputOR3X147OR 3-inputOR3X149OR 4-inputOR3X249OR 4-inputOR3X250NOR 2-inputOR3X251OR 2-inputOR3X252NOR 2-inputOR3X253NOR 2-inputOR3X254NOR 2-inputOR3X255NOR 2-inputNOR2X555NOR 2-inputNOR2X555NOR 2-inputNOR2X556NOR 3-inputNOR3X057NOR 3-inputNOR3X058NOR 3-inputNOR3X158NOR 3-inputNOR3X159NOR 3-inputNOR3X150NOR 3-inputNOR3X156NOR 3-inputNOR3X157NOR 3-inputNOR3X1<	27	AND 3-input	AND3X1
29         AND 3-input         AND3X4           30         AND 4-input         AND4X1           31         AND 4-input         AND4X2           32         AND 2-input         AND4X3           31         NAND 2-input         NAND2X1           35         NAND 2-input         NAND2X1           36         NAND 2-input         NAND2X2           36         NAND 2-input         NAND2X2           37         NAND 2-input         NAND2X2           38         NAND 2-input         NAND2X2           39         NAND 3-input         NAND3X0           38         NAND 3-input         NAND3X1           39         NAND 3-input         NAND3X1           40         NAND 4-input         NAND3X4           41         NAND 4-input         NAND3X4           42         NAND 4-input         NAND3X4           43         OR 2-input         OR2X1           44         OR 2-input         OR2X4           45         OR 2-input         OR2X2           46         OR 3-input         OR3X2           49         OR 4-input         OR4X1           50         OR 4-input         OR4X1	28	AND 3-input	AND3X2
30AND 4-inputAND4X131AND 4-inputAND4X232AND 4-inputAND4X233NAND 2-inputNAND2X134NAND 2-inputNAND2X135NAND 2-inputNAND2X236NAND 2-inputNAND2X237NAND 3-inputNAND3X038NAND 3-inputNAND3X240NAND 3-inputNAND3X241NAND 4-inputNAND3X242NAND 4-inputNAND3X243OR 2-inputOR2X144OR 2-inputOR2X145OR 2-inputOR2X246OR 3-inputOR3X147OR 3-inputOR3X149OR 4-inputOR3X249OR 4-inputOR3X251NAPUOR3X252NOR 2-inputOR3X253NOR 2-inputOR3X254OR 3-inputOR3X255NOR 2-inputOR4X256NOR 2-inputNOR2X257NOR 2-inputNOR2X258NOR 2-inputNOR2X259NOR 2-inputNOR2X251OR 4-inputNOR2X254NOR 2-inputNOR2X255NOR 2-inputNOR2X256NOR 3-inputNOR3X057NOR 3-inputNOR3X158NOR 3-inputNOR3X159NOR 3-inputNOR3X254NOR 3-inputNOR3X255NOR 3-inputNOR3X156 <td>29</td> <td>AND 3-input</td> <td>AND3X4</td>	29	AND 3-input	AND3X4
31AND 4-inputAND4X232AND 4-inputAND4X433NAND 2-inputNAND2X034NAND 2-inputNAND2X135NAND 2-inputNAND2X236NAND 2-inputNAND2X237NAND 3-inputNAND3X038NAND 3-inputNAND3X139NAND 3-inputNAND3X240NAND 3-inputNAND3X241NAND 4-inputNAND3X441NAND 4-inputNAND4X042NAND 4-inputOR2X143OR 2-inputOR2X144OR 2-inputOR2X145OR 2-inputOR2X246OR 3-inputOR3X147OR 3-inputOR3X149OR 4-inputOR4X150OR 4-inputOR4X251OR 4-inputOR4X452NOR 2-inputOR4X453NOR 2-inputOR4X454NOR 2-inputOR4X455NOR 2-inputNOR2X554NOR 2-inputNOR2X655NOR 2-inputNOR2X656NOR 3-inputNOR2X657NOR 3-inputNOR3X658NOR 3-inputNOR3X659NOR 3-inputNOR3X650NOR 3-inputNOR3X651NOR 3-inputNOR3X652NOR 3-inputNOR3X654NOR 3-inputNOR3X655NOR 3-inputNOR3X656NOR 3-inputNOR3X7 <t< td=""><td>30</td><td>AND 4-input</td><td>AND4X1</td></t<>	30	AND 4-input	AND4X1
32AND 4-inputAND4X433NAND 2-inputNAND2X034NAND 2-inputNAND2X135NAND 2-inputNAND2X236NAND 2-inputNAND2X437NAND 3-inputNAND3X138NAND 3-inputNAND3X240NAND 3-inputNAND3X241NAND 3-inputNAND3X242NAND 4-inputNAND3X243OR 2-inputOR2X144OR 2-inputOR2X145OR 2-inputOR2X146OR 3-inputOR3X147OR 3-inputOR3X149OR 4-inputOR3X249OR 4-inputOR4X150OR 4-inputOR4X251OR 4-inputOR4X252NOR 2-inputOR4X253NOR 2-inputOR3X354OR 3-inputOR3X355NOR 2-inputNOR2X256NOR 2-inputNOR2X256NOR 3-inputNOR2X356NOR 3-inputNOR2X356NOR 3-inputNOR2X356NOR 3-inputNOR3X358NOR 3-inputNOR3X359NOR 3-inputNOR3X350NOR 3-inputNOR3X356NOR 3-inputNOR3X357NOR 3-inputNOR3X358NOR 3-inputNOR3X359NOR 3-inputNOR3X350NOR 3-inputNOR3X351NOR 3-inputNOR3X4 <td< td=""><td>31</td><td>AND 4-input</td><td>AND4X2</td></td<>	31	AND 4-input	AND4X2
33NAND 2-inputNAND2X034NAND 2-inputNAND2X135NAND 2-inputNAND2X236NAND 2-inputNAND2X437NAND 3-inputNAND3X038NAND 3-inputNAND3X139NAND 3-inputNAND3X139NAND 3-inputNAND3X140NAND 3-inputNAND3X441NAND 4-inputNAND4X242NAND 4-inputNAND4X143OR 2-inputOR2X144OR 2-inputOR2X145OR 2-inputOR2X246OR 3-inputOR3X147OR 3-inputOR3X248OR 3-inputOR3X250OR 4-inputOR4X151OR 4-inputOR4X251OR 4-inputOR4X252NOR 2-inputNOR2X053NOR 2-inputNOR2X054NOR 2-inputNOR2X155NOR 2-inputNOR2X156NOR 3-inputNOR2X156NOR 3-inputNOR2X156NOR 3-inputNOR2X156NOR 3-inputNOR2X156NOR 3-inputNOR3X157NOR 3-inputNOR3X158NOR 3-inputNOR3X159NOR 3-inputNOR3X156NOR 3-inputNOR3X157NOR 3-inputNOR3X158NOR 3-inputNOR3X159NOR 3-inputNOR3X156NOR 3-inputNOR3X1 <td>32</td> <td>AND 4-input</td> <td>AND4X4</td>	32	AND 4-input	AND4X4
34NAND 2-inputNAND2X135NAND 2-inputNAND2X236NAND 2-inputNAND2X437NAND 3-inputNAND3X038NAND 3-inputNAND3X139NAND 3-inputNAND3X240NAND 3-inputNAND3X441NAND 4-inputNAND4X042NAND 4-inputNAND4X143OR 2-inputOR2X144OR 2-inputOR2X245OR 2-inputOR3X147OR 3-inputOR3X248OR 3-inputOR3X249OR 4-inputOR4X452NOR 2-inputOR4X251OR 4-inputOR4X252NOR 2-inputOR4X253NOR 2-inputNOR2X054NOR 2-inputNOR2X155NOR 2-inputNOR2X154NOR 2-inputNOR2X155NOR 3-inputNOR2X156NOR 3-inputNOR3X057NOR 3-inputNOR3X158NOR 3-inputNOR3X158NOR 3-inputNOR3X1	33	NAND 2-input	NAND2X0
35NAND 2-inputNAND2X236NAND 2-inputNAND2X437NAND 3-inputNAND3X038NAND 3-inputNAND3X139NAND 3-inputNAND3X240NAND 3-inputNAND3X241NAND 4-inputNAND4X042NAND 4-inputNAND4X143OR 2-inputOR2X144OR 2-inputOR2X145OR 2-inputOR2X246OR 3-inputOR3X147OR 3-inputOR3X449OR 4-inputOR4X150OR 4-inputOR4X251OR 4-inputOR4X252NOR 2-inputOR4X253NOR 2-inputNOR2X054NOR 2-inputNOR2X155NOR 2-inputNOR2X256NOR 3-inputNOR3X057NOR 3-inputNOR3X158NOR 3-inputNOR3X158NOR 3-inputNOR3X158NOR 3-inputNOR3X156NOR 3-inputNOR3X157NOR 3-inputNOR3X158NOR 3-inputNOR3X2	34	NAND 2-input	NAND2X1
36NAND 2-inputNAND2X437NAND 3-inputNAND3X038NAND 3-inputNAND3X139NAND 3-inputNAND3X240NAND 3-inputNAND3X241NAND 4-inputNAND4X042NAND 4-inputNAND4X143OR 2-inputOR2X144OR 2-inputOR2X145OR 2-inputOR2X246OR 3-inputOR3X147OR 3-inputOR3X248OR 4-inputOR4X150OR 4-inputOR4X151OR 4-inputOR4X152NOR 2-inputOR4X453NOR 2-inputNOR2X254NOR 2-inputNOR2X255NOR 2-inputNOR2X256NOR 3-inputNOR3X057NOR 3-inputNOR3X158NOR 3-inputNOR3X158NOR 3-inputNOR3X156NOR 3-inputNOR3X157NOR 3-inputNOR3X158NOR 3-inputNOR3X159NOR 3-inputNOR3X156NOR 3-inputNOR3X2	35	NAND 2-input	NAND2X2
37NAND 3-inputNAND33037NAND 3-inputNAND3X038NAND 3-inputNAND3X139NAND 3-inputNAND3X240NAND 3-inputNAND3X241NAND 4-inputNAND3X441NAND 4-inputNAND4X042NAND 4-inputNAND4X143OR 2-inputOR2X144OR 2-inputOR2X245OR 2-inputOR2X446OR 3-inputOR3X147OR 3-inputOR3X248OR 3-inputOR3X449OR 4-inputOR4X150OR 4-inputOR4X251OR 4-inputOR4X252NOR 2-inputNOR2X053NOR 2-inputNOR2X154NOR 2-inputNOR2X255NOR 2-inputNOR2X156NOR 3-inputNOR3X157NOR 3-inputNOR3X158NOR 3-inputNOR3X159NOR 3-inputNOR3X150NOR 3-inputNOR3X156NOR 3-inputNOR3X157NOR 3-inputNOR3X158NOR 3-inputNOR3X159NOR 3-inputNOR3X159NOR 3-inputNOR3X159NOR 3-inputNOR3X159NOR 3-inputNOR3X159NOR 3-inputNOR3X159NOR 3-inputNOR3X159NOR 3-inputNOR3X150NOR 3-inputNOR3X1 <td>36</td> <td>NAND 2-input</td> <td>NAND2X4</td>	36	NAND 2-input	NAND2X4
38NAND 3-inputNAND 3339NAND 3-inputNAND3X240NAND 3-inputNAND3X441NAND 4-inputNAND3X441NAND 4-inputNAND4X042NAND 4-inputNAND4X143OR 2-inputOR2X144OR 2-inputOR2X245OR 2-inputOR2X446OR 3-inputOR3X147OR 3-inputOR3X248OR 3-inputOR3X449OR 4-inputOR4X150OR 4-inputOR4X251OR 4-inputOR4X252NOR 2-inputNOR2X255NOR 2-inputNOR2X154NOR 2-inputNOR2X255NOR 2-inputNOR2X156NOR 3-inputNOR3X057NOR 3-inputNOR3X158NOR 3-inputNOR3X159NOR 3-inputNOR3X150NOR 3-inputNOR3X154NOR 3-inputNOR3X155NOR 3-inputNOR3X056NOR 3-inputNOR3X157NOR 3-inputNOR3X158NOR 3-inputNOR3X159NOR 3-inputNOR3X159NOR 3-inputNOR3X159NOR 3-inputNOR3X159NOR 3-inputNOR3X159NOR 3-inputNOR3X159NOR 3-inputNOR3X1	37	NAND 3-input	NAND3X0
39NAND 3-inputNAND3X240NAND 3-inputNAND3X441NAND 4-inputNAND4X042NAND 4-inputNAND4X143OR 2-inputOR2X144OR 2-inputOR2X245OR 2-inputOR2X446OR 3-inputOR3X147OR 3-inputOR3X248OR 3-inputOR3X249OR 4-inputOR4X150OR 4-inputOR4X251OR 4-inputOR4X252NOR 2-inputNOR2X253NOR 2-inputNOR2X254NOR 2-inputNOR2X255NOR 2-inputNOR2X256NOR 3-inputNOR2X257NOR 3-inputNOR2X358NOR 3-inputNOR3X159NOR 3-inputNOR3X250NOR 3-inputNOR2X351NOR 3-inputNOR2X352NOR 3-inputNOR3X154NOR 3-inputNOR3X155NOR 3-inputNOR3X156NOR 3-inputNOR3X257NOR 3-inputNOR3X258NOR 3-inputNOR3X259NOR 3-inputNOR3X250NOR 3-inputNOR3X256NOR 3-inputNOR3X257NOR 3-inputNOR3X258NOR 3-inputNOR3X259NOR 3-inputNOR3X259NOR 3-inputNOR3X250NOR 3-inputNOR3X257 <td>38</td> <td>NAND 3-input</td> <td>NAND3X1</td>	38	NAND 3-input	NAND3X1
40NAND 3-inputNAND3X441NAND 4-inputNAND4X042NAND 4-inputNAND4X143OR 2-inputOR2X144OR 2-inputOR2X245OR 2-inputOR2X446OR 3-inputOR3X147OR 3-inputOR3X148OR 3-inputOR3X49OR 4-inputOR4X150OR 4-inputOR4X151OR 4-inputOR4X251OR 4-inputOR4X251OR 2-inputNOR2X053NOR 2-inputNOR2X154NOR 2-inputNOR2X155NOR 2-inputNOR2X156NOR 3-inputNOR3X157NOR 3-inputNOR3X158NOR 3-inputNOR3X159NOR 3-inputNOR3X150NOR 3-inputNOR3X156NOR 3-inputNOR3X157NOR 3-inputNOR3X158NOR 3-inputNOR3X254NOR 3-inputNOR3X155NOR 3-inputNOR3X156NOR 3-inputNOR3X157NOR 3-inputNOR3X158NOR 3-inputNOR3X159NOR 3-inputNOR3X250NOR 3-inputNOR3X157NOR 3-inputNOR3X256NOR 3-inputNOR3X257NOR 3-inputNOR3X256NOR 3-inputNOR3X257NOR 3-inputNOR3X258	39	NAND 3-input	NAND3X2
41NAND 4-inputNAND4X042NAND 4-inputNAND4X143OR 2-inputOR2X144OR 2-inputOR2X245OR 2-inputOR2X446OR 3-inputOR3X147OR 3-inputOR3X248OR 3-inputOR3X449OR 4-inputOR4X150OR 4-inputOR4X150OR 4-inputOR4X251OR 2-inputOR4X251OR 2-inputNOR2X053NOR 2-inputNOR2X154NOR 2-inputNOR2X255NOR 3-inputNOR2X256NOR 3-inputNOR2X157NOR 3-inputNOR3X158NOR 3-inputNOR3X159NOR 3-inputNOR3X150NOR 3-inputNOR3X151NOR 3-inputNOR3X153NOR 3-inputNOR3X154NOR 3-inputNOR3X155NOR 3-inputNOR3X156NOR 3-inputNOR3X157NOR 3-inputNOR3X158NOR 3-inputNOR3X1	40	NAND 3-input	NAND3X4
42NAND 4-inputNAND4X143OR 2-inputOR2X144OR 2-inputOR2X245OR 2-inputOR2X446OR 3-inputOR3X147OR 3-inputOR3X248OR 3-inputOR3X249OR 4-inputOR4X150OR 4-inputOR4X151OR 4-inputOR4X251OR 4-inputOR4X452NOR 2-inputNOR2X053NOR 2-inputNOR2X154NOR 2-inputNOR2X255NOR 2-inputNOR2X256NOR 3-inputNOR2X257NOR 3-inputNOR2X258NOR 3-inputNOR3X057NOR 3-inputNOR3X058NOR 3-inputNOR3X158NOR 3-inputNOR3X2	41	NAND 4-input	NAND4X0
12         1.8 a.B.2         OR           43         OR 2-input         OR2X1           44         OR 2-input         OR2X2           45         OR 2-input         OR2X4           46         OR 3-input         OR3X1           47         OR 3-input         OR3X1           47         OR 3-input         OR3X2           48         OR 3-input         OR3X2           49         OR 4-input         OR4X1           50         OR 4-input         OR4X1           50         OR 4-input         OR4X1           50         OR 4-input         OR4X1           51         OR 4-input         OR4X2           51         OR 2-input         NOR2X0           53         NOR 2-input         NOR2X0           53         NOR 2-input         NOR2X1           54         NOR 2-input         NOR2X2           55         NOR 2-input         NOR3X0           57         NOR 3-input         NOR3X1           58         NOR 3-input         NOR3X1           58         NOR 3-input         NOR3X2	42	NAND 4-input	NAND4X1
44         OR 2-input         OR2X2           45         OR 2-input         OR2X4           46         OR 3-input         OR3X1           47         OR 3-input         OR3X1           47         OR 3-input         OR3X2           48         OR 3-input         OR3X2           49         OR 4-input         OR4X1           50         OR 4-input         OR4X2           51         OR 4-input         OR4X2           52         NOR 2-input         NOR2X0           53         NOR 2-input         NOR2X1           54         NOR 2-input         NOR2X2           55         NOR 2-input         NOR2X2           56         NOR 3-input         NOR3X0           57         NOR 3-input         NOR3X1           58         NOR 3-input         NOR3X1           58         NOR 3-input         NOR3X2	43	OR 2-input	OR2X1
45OR 2-inputOR2X446OR 3-inputOR3X147OR 3-inputOR3X248OR 3-inputOR3X449OR 4-inputOR4X150OR 4-inputOR4X251OR 4-inputOR4X251OR 2-inputOR4X452NOR 2-inputNOR2X053NOR 2-inputNOR2X154NOR 2-inputNOR2X255NOR 2-inputNOR2X456NOR 3-inputNOR3X057NOR 3-inputNOR3X158NOR 3-inputNOR3X254NOR 3-inputNOR3X1	44	OR 2-input	OR2X2
46         OR 3-input         OR3X1           47         OR 3-input         OR3X2           48         OR 3-input         OR3X4           49         OR 4-input         OR4X1           50         OR 4-input         OR4X1           51         OR 4-input         OR4X2           51         OR 4-input         OR4X4           52         NOR 2-input         NOR2X0           53         NOR 2-input         NOR2X1           54         NOR 2-input         NOR2X2           55         NOR 2-input         NOR2X2           56         NOR 3-input         NOR3X0           57         NOR 3-input         NOR3X1           58         NOR 3-input         NOR3X2	45	OR 2-input	OR2X4
47       OR 3-input       OR3X2         48       OR 3-input       OR3X4         49       OR 4-input       OR4X1         50       OR 4-input       OR4X2         51       OR 4-input       OR4X2         51       OR 2-input       OR4X4         52       NOR 2-input       NOR2X0         53       NOR 2-input       NOR2X1         54       NOR 2-input       NOR2X2         55       NOR 2-input       NOR2X4         56       NOR 3-input       NOR3X0         57       NOR 3-input       NOR3X1         58       NOR 3-input       NOR3X2	46	OR 3-input	OR3X1
48         OR 3-input         OR3X4           49         OR 4-input         OR4X1           50         OR 4-input         OR4X2           51         OR 4-input         OR4X4           52         NOR 2-input         OR4X4           53         NOR 2-input         NOR2X0           53         NOR 2-input         NOR2X1           54         NOR 2-input         NOR2X2           55         NOR 2-input         NOR2X4           56         NOR 3-input         NOR3X0           57         NOR 3-input         NOR3X1           58         NOR 3-input         NOR3X2	47	OR 3-input	OR3X2
10         OR 4-input         OR4X1           49         OR 4-input         OR4X1           50         OR 4-input         OR4X2           51         OR 4-input         OR4X4           52         NOR 2-input         NOR2X0           53         NOR 2-input         NOR2X1           54         NOR 2-input         NOR2X2           55         NOR 2-input         NOR2X4           56         NOR 3-input         NOR3X0           57         NOR 3-input         NOR3X1           58         NOR 3-input         NOR3X2	48	OR 3-input	OR3X4
10         OR 4-input         OR4X2           50         OR 4-input         OR4X2           51         OR 4-input         OR4X4           52         NOR 2-input         NOR2X0           53         NOR 2-input         NOR2X1           54         NOR 2-input         NOR2X2           55         NOR 2-input         NOR2X4           56         NOR 3-input         NOR3X0           57         NOR 3-input         NOR3X1           58         NOR 3-input         NOR3X2	49	OR 4-input	OR4X1
50Stranger51OR 4-input52NOR 2-input53NOR 2-input54NOR 2-input55NOR 2-input55NOR 2-input56NOR 3-input57NOR 3-input58NOR 3-input50NOR 3-input51NOR 3-input52NOR 3-input53NOR 3-input54NOR 3-input55NOR 3-input56NOR 3-input57NOR 3-input58NOR 3-input59NOR 3-input50NOR 3-input51NOR 3-input52NOR 3-input53NOR 3-input54NOR 3-input55NOR 3-input56NOR 3-input57NOR 3-input58NOR 3-input59NOR 3-input	50	OR 4-input	OR4X2
51OR 2-input52NOR 2-inputNOR2X053NOR 2-inputNOR2X154NOR 2-inputNOR2X255NOR 2-inputNOR2X456NOR 3-inputNOR3X057NOR 3-inputNOR3X158NOR 3-inputNOR3X2	51	OR 4-input	OR4X4
52NOR 2 inputNOR2X153NOR 2-inputNOR2X154NOR 2-inputNOR2X255NOR 2-inputNOR2X456NOR 3-inputNOR3X057NOR 3-inputNOR3X158NOR 3-inputNOR3X2	52		NOR2X0
50NOR 2 input54NOR 2-input55NOR 2-input56NOR 3-input57NOR 3-input58NOR 3-input58NOR 3-input59NOR 3-input	53	NOR 2-input	NOR2X1
54         NOR 2 input         NOR2X4           55         NOR 3-input         NOR3X0           57         NOR 3-input         NOR3X1           58         NOR 3-input         NOR3X2	54	NOR 2-input	NOR2X2
55         NOR 2-input         NOR3X0           56         NOR 3-input         NOR3X1           57         NOR 3-input         NOR3X1           58         NOR 3-input         NOR3X2	55		NOR2X4
50     NOR 3 input       57     NOR 3-input       58     NOR 3-input       59     NOR 3-input	56	NOR 3-input	NOR3X0
57     Norts input       58     NOR 3-input       58     NOR 3-input	57		NOR3X1
	58		NOR3X2
50 I NOR 3-innut I NUR334	59		NOR3X4

No	Cell Description	Cell Name
60	NOR 4-input	NOR4X0
61	NOR 4-input	NOR4X1
62	XOR 2-input	XOR2X1
63	XOR 2-input	XOR2X2
64	XOR 3-input	XOR3X1
65	XOR 3-input	XOR3X2
66	XNOR 2-input	XNOR2X1
67	XNOR 2-input	XNOR2X2
68	XNOR 3-input	XNOR3X1
69	XNOR 3-input	XNOR3X2
	Complex Logic Gates	
70	AND-OR 2/1	AO21X1
71	AND-OR 2/1	AO21X2
72	AND-OR 2/2	AO22X1
73	AND-OR 2/2	AO22X2
74	AND-OR 2/2/1	AO221X1
75	AND-OR 2/2/1	AO221X2
76	AND-OR 2/2/2	AO222X1
77	AND-OR 2/2/2	AO222X2
78	AND-OR-Invert 2/1	AOI21X1
79	AND-OR Invert 2/1	AOI21X2
80	AND-OR-Invert 2/2	AOI22X1
81	AND-OR-Invert 2/2	AOI22X2
82	AND-OR-Invert 2/2/1	AOI221X1
83	AND-OR-Invert 2/2/1	AOI221X2
84	AND-OR-Invert 2/2/2	AOI222X1
85	AND-OR-Invert 2/2/2	AOI222X2
86	OR-AND 2/1	OA21X1
87	OR-AND 2/1	OA21X2
88	OR-AND 2/2	OA22X1
89	OR-AND 2/2	OA22X2
90	OR-AND 2/2/1	OA221X1
91	OR-AND 2/2/1	OA221X2
92	OR-AND 2/2/2	OA222X1
93	OR-AND 2/2/2	OA222X2
94	OR-AND-Invert 2/1	OAI21X1
95	OR-AND-Invert 2/1	OAI21X2
96	OR-AND-Invert 2/2	OAI22X1
97	OR-AND-Invert 2/2	0AI22X2
98	OR-AND-Invert 2/2/1	OAI221X1
99	$OR-\Delta NID-Invert 2/2/1$	OAI221X2
100	OR-AND-Invert 2/2/2	OAI222X1

No	Cell Description	Cell Name
101	OR-AND-Invert 2/2/2	OAI222X2
	Multiplexers	
102	Multiplexer 2 to 1	MUX21X1
103	Multiplexer 2 to 1	MUX21X2
104	Multiplexer 4 to 1	MUX41X1
105	Multiplexer 4 to 1	MUX41X2
	Decoders	
106	Decoder 2 to 4	DEC24X1
107	Decoder 2 to 4	DEC24X2
	Adders and Subtractors	
108	Half Adder 1 bit	HADDX1
109	Half Adder 1 bit	HADDX2
110	Full Adder 1 bit	FADDX1
111	Full Adder 1 bit	FADDX2
	D Flip-Flops	
112	Pos Edge DFF	DFFX1
113	Pos Edge DFF	DFFX2
114	Pos Edge DFF, w/ Async Low-Active Set	DFFASX1
115	Pos Edge DFF, w/ Async Low-Active Set	DFFASX2
116	Pos Edge DFF, w/ Async Low-Active Reset	DFFARX1
117	Pos Edge DFF, w/ Async Low-Active Reset	DFFARX2
118	Pos Edge DFF, w/ Async Low-Active Set & Reset	DFFASRX1
119	Pos Edge DFF, w/ Async Low-Active Set & Reset	DFFASRX2
120	Pos Edge DFF, w/ Sync Low-Active Set & Reset	DFFSSRX1
121	Pos Edge DFF, w/ Sync Low-Active Set & Reset	DFFSSRX2
122	Neg Edge DFF	DFFNX1
123	Neg Edge DFF	DFFNX2
124	Neg Edge DFF, w/ Async Low-Active Set	DFFNASX1
125	Neg Edge DFF, w/ Async Low-Active Set	DFFNASX2
126	Neg Edge DFF, w/ Async Low-Active Reset	DFFNARX1
127	Neg Edge DFF, w/ Async Low-Active Reset	DFFNARX2
128	Neg Edge DFF, w/ Async Low-Active Set & Reset	DFFNASRX1
129	Neg Edge DFF, w/ Async Low-Active Set & Reset	DFFNASRX2
130	Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out	DFFNASRQX1
131	Neg Edge DFF, w/ Async Low-Active Set & Reset, Only Q out	DFFNASRQX2
132	Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out	DFFNASRNX1
133	Neg Edge DFF, w/ Async Low-Active Set & Reset, Only QN out	DFFNASRNX2
	Scan D Flip-Flops	
134	Scan Pos Edge DFF	SDFFX1
135	Scan Pos Edge DFF	SDFFX2
136	Scan Pos Edge DFF w/ Async Low-Active Set	SDFFASX1
137	Scan Pos Edge DFF w/ Async Low-Active Set	SDFFASX2

No	Cell Description	Cell Name
138	Scan Pos Edge DFF w/ Async Low-Active Reset	SDFFARX1
139	Scan Pos Edge DFF w/ Async Low-Active Reset	SDFFARX2
140	Scan Pos Edge DFF w/ Async Low-Active Set & Reset	SDFFASRX1
141	Scan Pos Edge DFF w/ Async Low-Active Set & Reset	SDFFASRX2
142	Scan Pos Edge DFF w/ Async Low-Active Set & Reset, Q, QN, & S0 outs	SDFFASRSX1
143	Scan Pos Edge DFF w/ Async Low-Active Set & Reset, Q, QN, & S0 outs	SDFFASRSX2
144	Scan Pos Edge DFF w/ Sync Low-Active Set & Reset	SDFFSSRX1
145	Scan Pos Edge DFF w/ Sync Low-Active Set & Reset	SDFFSSRX2
146	Scan Neg Edge DFF	SDFFNX1
147	Scan Neg Edge DFF	SDFFNX2
148	Scan Neg Edge DFF w/ Async Low-Active Set	SDFFNASX1
149	Scan Neg Edge DFF w/ Async Low-Active Set	SDFFNASX2
150	Scan Neg Edge DFF w/ Async Low-Active Reset	SDFFNARX1
151	Scan Neg Edge DFF w/ Async Low-Active Reset	SDFFNARX2
152	Scan Neg Edge DFF w/ Async Low-Active Set & Reset	SDFFNASRX1
153	Scan Neg Edge DFF w/ Async Low-Active Set & Reset	SDFFNASRX2
	Latches	
154	RS NAND Latch	LNANDX1
155	RS NAND Latch	LNANDX2
156	High-Active Latch	LATCHX1
157	High-Active Latch	LATCHX2
158	High-Active Latch w/ Async Low-Active Set	LASX1
159	High-Active Latch w/ Async Low-Active Set	LASX2
160	High-Active Latch w/ Async Low-Active Reset	LARX1
161	High-Active Latch w/ Async Low-Active Reset	LARX2
162	High-Active Latch w/ Async Low-Active Set & Reset	LASRX1
163	High-Active Latch w/ Async Low-Active Set & Reset	LASRX2
164	High-Active Latch w/ Async Low-Active Set & Reset only Q out	LASRQX1
165	High-Active Latch w/ Async Low-Active Set & Reset only Q out	LASRQX2
166	High-Active Latch w/ Async Low-Active Set & Reset only QN out	LASRNX1
167	High-Active Latch w/ Async Low-Active Set & Reset only QN out	LASRNX2
	Clocked Gates	
168	Clock Gating cell w/ Latched Pos Edge Control Post	CGLPPSX2
169	Clock Gating cell w/ Latched Pos Edge Control Post	CGLPPSX4
170	Clock Gating cell w/ Latched Pos Edge Control Post	CGLPPSX8
171	Clock Gating cell w/ Latched Pos Edge Control Post	CGLPPSX16
172	Clock Gating cell w/ Latched Neg Edge Control Post	CGLNPSX2
173	Clock Gating cell w/ Latched Neg Edge Control Post	CGLNPSX4
174	Clock Gating cell w/ Latched Neg Edge Control Post	CGLNPSX8
175	Clock Gating cell w/ Latched Neg Edge Control Post	CGLNPSX16
176	Clock Gating cell w/ Latched Pos Edge Control Pre	CGLPPRX2
177	Clock Gating cell w/ Latched Pos Edge Control Pre	CGLPPRX8

178       Clock Gating cell w/ Latched Neg Edge Control Pre       CGLNPRX2         179       Clock Gating cell w/ Latched Neg Edge Control Pre       CGLNPRX3         Delay Lines       DELLN1X2         180       Non-inverting Delay Line, 250 ps       DELLN1X2         181       Non-inverting Delay Line, 750 ps       DELLN2X2         Pass Gates       DEXLN3X2         183       Pass Gate       PGX1         184       Pass Gate       PGX4         185       Pass Gate       PGX4         186       Bi-directional Switches       DELLN3X2         187       Bi-directional Switch w/ Low-Active Enable       BSLEX4         188       Bi-directional Switch w/ Low-Active Enable       BSLEX4         189       Hold O Isolation Cell (Logic AND)       ISOLANDX4         191       Hold O Isolation Cell (Logic AND)       ISOLANDX2         193       Hold O Isolation Cell (Logic CR)       ISOLANDX4         194       Hold O Isolation Cell (Logic CR)       ISOLANDX2         195       Hold I Isolation Cell (Logic CR)       ISOLORX1         194       Hold I Isolation Cell (Logic CR)       ISOLORX2         195       Hold I Isolation Cell (Logic CR)       ISOLORX2         196       Hold I Isolation Cell	No	Cell Description	Cell Name
179       Clock Gating cell w/ Latched Neg Edge Control Pre       CGLNPRX8         Delay Lines       0         180       Non-inverting Delay Line, 250 ps       DELLN1X2         181       Non-inverting Delay Line, 750 ps       DELLN3X2         Pass Gates       DELLN3X2         182       Pass Gate       PGX1         184       Pass Gate       PGX2         185       Pass Gate       PGX2         186       Bi-directional Switch w/ Low-Active Enable       BSLEX1         187       Bi-directional Switch w/ Low-Active Enable       BSLEX1         188       Bi-directional Switch w/ Low-Active Enable       BSLEX4         189       Hold 0 Isolation Cell (Logic AND)       ISOLANDX1         189       Hold 0 Isolation Cell (Logic AND)       ISOLANDX4         191       Hold 0 Isolation Cell (Logic AND)       ISOLANDX4         192       Hold 1 Isolation Cell (Logic CR)       ISOLORX4         193       Hold 1 Isolation Cell (Logic CR)       ISOLORX4         194       Hold 0 Isolation Cell (Logic CR)       ISOLORX4         194       Hold 1 Isolation Cell (Logic CR)       ISOLORX4         194       Hold 1 Isolation Cell (Logic CR)       ISOLORX4         195       Hold 1 Isolation Cell (Logic	178	Clock Gating cell w/ Latched Neg Edge Control Pre	CGLNPRX2
Delay Lines         DELLN1X2           180         Non-inverting Delay Line, 250 ps         DELLN1X2           181         Non-inverting Delay Line, 750 ps         DELLN2X2           182         Non-inverting Delay Line, 750 ps         DELLN3X2           Pass Gates         PGX1           183         Pass Gate         PGX2           184         Pass Gate         PGX2           185         Pass Gate         PGX4           Bi-directional Switches         Bi-directional Switch w/ Low-Active Enable         BSLEX2           186         Bi-directional Switch w/ Low-Active Enable         BSLEX4           180         Hold O Isolation Cell (Logic AND)         ISOLANDX1           180         Hold O Isolation Cell (Logic AND)         ISOLANDX2           191         Hold O Isolation Cell (Logic AND)         ISOLANDX4           192         Hold O Isolation Cell (Logic AND)         ISOLANDX4           193         Hold 1 Isolation Cell (Logic OR)         ISOLANDX2           194         Hold 1 Isolation Cell (Logic OR)         ISOLORX2           195         Hold 1 Isolation Cell (Logic OR)         ISOLORX4           194         Hold 1 Isolation Cell (Logic OR)         ISOLORX2           195         Hold 1 Isolation Cell (Logic OR)	179	Clock Gating cell w/ Latched Neg Edge Control Pre	CGLNPRX8
180     Non-inverting Delay Line, 250 ps     DELLN1X2       181     Non-inverting Delay Line, 500 ps     DELLN2X2       Pass Gates     DELLN3X2       Pass Gates     PGX1       183     Pass Gate     PGX1       184     Pass Gate     PGX1       185     Pass Gate     PGX4       186     Bi-directional Switch w/ Low-Active Enable     BSLEX1       187     Bi-directional Switch w/ Low-Active Enable     BSLEX4       188     Bi-directional Switch w/ Low-Active Enable     BSLEX4       188     Bi-directional Switch w/ Low-Active Enable     BSLEX4       180     Hold 0 Isolation Cell (Logic AND)     ISOLANDX1       190     Hold 0 Isolation Cell (Logic AND)     ISOLANDX2       191     Hold 0 Isolation Cell (Logic CR)     ISOLANDX3       192     Hold 0 Isolation Cell (Logic OR)     ISOLANDX4       194     Hold 1 Isolation Cell (Logic OR)     ISOLORX2       195     Hold 1 Isolation Cell (Logic OR)     ISOLORX4       196     Low to High Level Shifter     LSUPX1       197     Low to High Level Shifter     LSUPX2       198     Low to High Level Shifter     LSUPX4       199     Low to High Level Shifter     LSUPX4       198     Low to High Level Shifter     LSUPX4 <td< td=""><td></td><td>Delay Lines</td><td></td></td<>		Delay Lines	
181       Non-inverting Delay Line, 500 ps       DELLN2X2         182       Non-inverting Delay Line, 750 ps       DELLN3X2         Pass Gates       DELLN3X2         183       Pass Gate       PGX1         184       Pass Gate       PGX2         185       Pass Gate       PGX4         Bi-directional Switch w/ Low-Active Enable       BSLEX1         186       Bi-directional Switch w/ Low-Active Enable       BSLEX2         188       Bi-directional Switch w/ Low-Active Enable       BSLEX4         180       Hold 0 Isolation Cell (Logic AND)       ISOLANDX1         190       Hold 0 Isolation Cell (Logic AND)       ISOLANDX2         191       Hold 0 Isolation Cell (Logic CR)       ISOLANDX3         192       Hold 1 Isolation Cell (Logic CR)       ISOLORX2         193       Hold 1 Isolation Cell (Logic CR)       ISOLORX2         194       Hold 1 Isolation Cell (Logic CR)       ISOLORX2         195       Hold 1 Isolation Cell (Logic CR)       ISOLORX4         194       Hold 1 Isolation Cell (Logic CR)       ISOLORX2         195       Hold 1 Isolation Cell (Logic CR)       ISOLORX4         196       Hold 1 Isolation Cell (Logic CR)       ISOLORX4         195       Low to High Level	180	Non-inverting Delay Line, 250 ps	DELLN1X2
182       Non-inverting Delay Line, 750 ps       DELLN3X2         Pass Gates       PGX1         183       Pass Gate       PGX2         184       Pass Gate       PGX4         Bi-directional Switches       PGX4         Bi-directional Switch w/ Low-Active Enable       BSLEX2         186       Bi-directional Switch w/ Low-Active Enable       BSLEX4         187       Bi-directional Switch w/ Low-Active Enable       BSLEX4         188       Bi-directional Switch w/ Low-Active Enable       BSLEX4         189       Hold 0 Isolation Cell (Logic AND)       ISOLANDX1         190       Hold 0 Isolation Cell (Logic AND)       ISOLANDX2         191       Hold 0 Isolation Cell (Logic CAND)       ISOLANDX3         192       Hold 1 Isolation Cell (Logic CR)       ISOLANDX4         193       Hold 1 Isolation Cell (Logic CR)       ISOLORX2         194       Hold 1 Isolation Cell (Logic CR)       ISOLORX4         195       Hold 1 Isolation Cell (Logic CR)       ISOLORX2         194       Hold 1 Isolation Cell (Logic CR)       ISOLORX2         195       Hold 1 Isolation Cell (Logic CR)       ISOLORX2         196       Hold 1 Isolation Cell (Logic CR)       ISOLORX2         197       Low to High Leve	181	Non-inverting Delay Line, 500 ps	DELLN2X2
Pass Gates       PGX1         183       Pass Gate       PGX1         184       Pass Gate       PGX2         185       Pass Gate       PGX4         Bi-directional Switch w/ Low-Active Enable       BSLEX1         186       Bi-directional Switch w/ Low-Active Enable       BSLEX2         187       Bi-directional Switch w/ Low-Active Enable       BSLEX4         188       Bi-directional Switch w/ Low-Active Enable       BSLEX4         188       Hold 0 Isolation Cell (Logic AND)       ISOLANDX1         190       Hold 0 Isolation Cell (Logic AND)       ISOLANDX2         191       Hold 0 Isolation Cell (Logic CAND)       ISOLANDX4         192       Hold 1 Isolation Cell (Logic CR)       ISOLORX1         193       Hold 1 Isolation Cell (Logic CR)       ISOLORX2         194       Hold 1 Isolation Cell (Logic CR)       ISOLORX2         195       Hold 1 Isolation Cell (Logic CR)       ISOLORX4         194       Hold 1 Isolation Cell (Logic CR)       ISOLORX4         197       Low to High Level Shifter       LSUPX2         198       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX4         201       High to Low Level Shifter <t< td=""><td>182</td><td>Non-inverting Delay Line, 750 ps</td><td>DELLN3X2</td></t<>	182	Non-inverting Delay Line, 750 ps	DELLN3X2
183       Pass Gate       PGX1         184       Pass Gate       PGX2         185       Pass Gate       PGX4         Bi-directional Switches       Bi-directional Switch w/ Low-Active Enable       BSLEX1         187       Bi-directional Switch w/ Low-Active Enable       BSLEX2         188       Bi-directional Switch w/ Low-Active Enable       BSLEX4         180       Isolation Cells       Isolation Cells         198       Hold 0 Isolation Cell (Logic AND)       ISOLANDX1         190       Hold 0 Isolation Cell (Logic AND)       ISOLANDX2         191       Hold 0 Isolation Cell (Logic CR)       ISOLANDX4         192       Hold 1 Isolation Cell (Logic CR)       ISOLORX4         193       Hold 1 Isolation Cell (Logic CR)       ISOLORX2         194       Hold 1 Isolation Cell (Logic CR)       ISOLORX2         195       Hold 1 Isolation Cell (Logic CR)       ISOLORX2         196       Hold 1 Isolation Cell (Logic CR)       ISOLORX8         197       Low to High Level Shifter       LSUPX1         198       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX4         219       Low to High Level Shifter       LSDNX2         211		Pass Gates	
184       Pass Gate       PGX2         185       Pass Gate       PGX4         Bi-directional Switch w/ Low-Active Enable       BSLEX1         186       Bi-directional Switch w/ Low-Active Enable       BSLEX2         188       Bi-directional Switch w/ Low-Active Enable       BSLEX4         Isolation Cells       BSLEX1         189       Hold 0 Isolation Cell (Logic AND)       ISOLANDX1         190       Hold 0 Isolation Cell (Logic AND)       ISOLANDX2         191       Hold 0 Isolation Cell (Logic AND)       ISOLANDX3         192       Hold 0 Isolation Cell (Logic CR)       ISOLANDX4         193       Hold 1 Isolation Cell (Logic OR)       ISOLORX5         194       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         195       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         196       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         197       Low to High Level Shifter       LSUPX1         198       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSDNX2         199       Low to High Level Shifter       LSDNX2         199       Low to High Level Shifter	183	Pass Gate	PGX1
185       Pass Gate       PGX4         Bi-directional Switch w/ Low-Active Enable       BSLEX1         186       Bi-directional Switch w/ Low-Active Enable       BSLEX2         187       Bi-directional Switch w/ Low-Active Enable       BSLEX4         188       Bi-directional Switch w/ Low-Active Enable       BSLEX4         189       Hold 0 Isolation Cell (Logic AND)       ISOLANDX1         190       Hold 0 Isolation Cell (Logic AND)       ISOLANDX2         191       Hold 0 Isolation Cell (Logic AND)       ISOLANDX3         192       Hold 1 Isolation Cell (Logic AND)       ISOLANDX4         193       Hold 1 Isolation Cell (Logic OR)       ISOLORX1         194       Hold 1 Isolation Cell (Logic OR)       ISOLORX2         195       Hold 1 Isolation Cell (Logic OR)       ISOLORX2         196       Hold 1 Isolation Cell (Logic OR)       ISOLORX2         197       Low to High Level Shifter       LSUPX1         198       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX3         199       Low to High Level Shifter       LSUPX3         200       Low to High Level Shifter       LSUPX3	184	Pass Gate	PGX2
Bi-directional Switches           186         Bi-directional Switch w/ Low-Active Enable         BSLEX1           187         Bi-directional Switch w/ Low-Active Enable         BSLEX2           188         Bi-directional Switch w/ Low-Active Enable         BSLEX4           180         Hold 0 Isolation Cells         ISOLANDX1           190         Hold 0 Isolation Cell (Logic AND)         ISOLANDX2           191         Hold 0 Isolation Cell (Logic AND)         ISOLANDX4           192         Hold 0 Isolation Cell (Logic OR)         ISOLANDX4           193         Hold 1 Isolation Cell (Logic OR)         ISOLORX2           194         Hold 1 Isolation Cell (Logic OR)         ISOLORX2           195         Hold 1 Isolation Cell (Logic OR)         ISOLORX4           196         Hold 1 Isolation Cell (Logic OR)         ISOLORX2           197         Low to High Level Shifter         LSUPX2           198         Low to High Level Shifter         LSUPX2           199         Low to High Level Shifter         LSUPX2           199         Low to High Level Shifter         LSUPX4           200         Low to High Level Shifter         LSDNX4           201         High to Low Level Shifter         LSDNX4           202         Low	185	Pass Gate	PGX4
186       Bi-directional Switch w/ Low-Active Enable       BSLEX1         187       Bi-directional Switch w/ Low-Active Enable       BSLEX2         188       Bi-directional Switch w/ Low-Active Enable       BSLEX4         189       Hold 0 Isolation Cell (Logic AND)       ISOLANDX1         190       Hold 0 Isolation Cell (Logic AND)       ISOLANDX2         191       Hold 0 Isolation Cell (Logic AND)       ISOLANDX4         192       Hold 0 Isolation Cell (Logic AND)       ISOLANDX4         193       Hold 1 Isolation Cell (Logic OR)       ISOLORX1         194       Hold 1 Isolation Cell (Logic OR)       ISOLORX2         195       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         196       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         197       Low to High Level Shifter       LSUPX1         198       Low to High Level Shifter       LSUPX2         200       Low to High Level Shifter       LSUPX4         201       High to Low Level Shifter       LSUPX1         202       High to Low Level Shifter       LSDNX4         203       High to Low Level Shifter       LSDNX4         204       High to Low Level Shifter       LSDNX4         205       Low to High Level Shifter / Low-Active Enable </td <td></td> <td>Bi-directional Switches</td> <td></td>		Bi-directional Switches	
187       Bi-directional Switch w/ Low-Active Enable       BSLEX2         188       Bi-directional Switch w/ Low-Active Enable       BSLEX4         1solation Cells       ISOLANDX1         190       Hold 0 Isolation Cell (Logic AND)       ISOLANDX2         191       Hold 0 Isolation Cell (Logic AND)       ISOLANDX4         192       Hold 0 Isolation Cell (Logic AND)       ISOLANDX4         193       Hold 1 Isolation Cell (Logic CR)       ISOLANDX4         194       Hold 1 Isolation Cell (Logic CR)       ISOLORX1         195       Hold 1 Isolation Cell (Logic CR)       ISOLORX2         196       Hold 1 Isolation Cell (Logic CR)       ISOLORX2         197       Low to High Level Shifter       LSUPX1         198       Low to High Level Shifter       LSUPX1         198       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX3         201       High to Low Level Shifter       LSUPX4         202       High to Low Level Shifter       LSDNX2         203       High to Low Level Shifter       LSDNX2         204       High to Low Level Shifter/ Low-Active Enable       LSUPENX2         <	186	Bi-directional Switch w/ Low-Active Enable	BSLEX1
188       Bi-directional Switch w/ Low-Active Enable       BSLEX4         189       Hold 0 Isolation Cell (Logic AND)       ISOLANDX1         190       Hold 0 Isolation Cell (Logic AND)       ISOLANDX2         191       Hold 0 Isolation Cell (Logic AND)       ISOLANDX4         192       Hold 0 Isolation Cell (Logic CR)       ISOLANDX4         193       Hold 1 Isolation Cell (Logic OR)       ISOLANDX3         194       Hold 1 Isolation Cell (Logic OR)       ISOLORX1         195       Hold 1 Isolation Cell (Logic OR)       ISOLORX2         195       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         196       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         197       Low to High Level Shifter       LSUPX1         198       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX3         200       Low to High Level Shifter       LSUPX4         201       High to Low Level Shifter       LSUPX3         202       High to Low Level Shifter       LSDNX2         203       High to Low Level Shifter       LSDNX8         205       Low to High Level Shifter/ Low-Active Enable       LSUPENX2 <td>187</td> <td>Bi-directional Switch w/ Low-Active Enable</td> <td>BSLEX2</td>	187	Bi-directional Switch w/ Low-Active Enable	BSLEX2
Isolation Cells         ISOLANDX1           189         Hold 0 Isolation Cell (Logic AND)         ISOLANDX1           190         Hold 0 Isolation Cell (Logic AND)         ISOLANDX2           191         Hold 0 Isolation Cell (Logic AND)         ISOLANDX4           192         Hold 0 Isolation Cell (Logic AND)         ISOLANDX4           193         Hold 1 Isolation Cell (Logic OR)         ISOLORX1           194         Hold 1 Isolation Cell (Logic OR)         ISOLORX2           195         Hold 1 Isolation Cell (Logic OR)         ISOLORX4           196         Hold 1 Isolation Cell (Logic OR)         ISOLORX4           196         Hold 1 Isolation Cell (Logic OR)         ISOLORX4           196         Hold 1 Isolation Cell (Logic OR)         ISOLORX4           197         Low to High Level Shifter         LSUPX1           198         Low to High Level Shifter         LSUPX2           199         Low to High Level Shifter         LSUPX2           200         Low to High Level Shifter         LSUPX3           201         High to Low Level Shifter         LSDNX1           202         High to Low Level Shifter         LSDNX2           203         High to Low Level Shifter/ Low-Active Enable         LSUPENX4           204 <td>188</td> <td>Bi-directional Switch w/ Low-Active Enable</td> <td>BSLEX4</td>	188	Bi-directional Switch w/ Low-Active Enable	BSLEX4
189       Hold 0 Isolation Cell (Logic AND)       ISOLANDX1         190       Hold 0 Isolation Cell (Logic AND)       ISOLANDX2         191       Hold 0 Isolation Cell (Logic AND)       ISOLANDX4         192       Hold 0 Isolation Cell (Logic AND)       ISOLANDX8         193       Hold 1 Isolation Cell (Logic CR)       ISOLORX1         194       Hold 1 Isolation Cell (Logic OR)       ISOLORX2         195       Hold 1 Isolation Cell (Logic OR)       ISOLORX2         196       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         196       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         196       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         197       Low to High Level Shifter       LSUPX1         198       Low to High Level Shifter       LSUPX1         199       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX3         200       Low to High Level Shifter       LSUPX4         201       High to Low Level Shifter       LSUPX3         202       High to Low Level Shifter       LSDNX4         203       High to Low Level Shifter       LSDNX4         204       High to Low Level Shifter/ Low-Active Enable       LSUPENX4 </td <td></td> <td>Isolation Cells</td> <td></td>		Isolation Cells	
190       Hold 0 Isolation Cell (Logic AND)       ISOLANDX2         191       Hold 0 Isolation Cell (Logic AND)       ISOLANDX4         192       Hold 0 Isolation Cell (Logic AND)       ISOLANDX8         193       Hold 1 Isolation Cell (Logic OR)       ISOLORX1         194       Hold 1 Isolation Cell (Logic OR)       ISOLORX1         195       Hold 1 Isolation Cell (Logic OR)       ISOLORX2         195       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         196       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         197       Low to High Level Shifter       LSUPX1         198       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX2         201       High to Low Level Shifter       LSUPX2         202       High to Low Level Shifter       LSUPX3         203       High to Low Level Shifter       LSUPX4         204       High to Low Level Shifter/ Low-Active Enable       LSUPENX4         205       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         206       Low to High Level Shifter/ Low-Active Enable <t< td=""><td>189</td><td>Hold 0 Isolation Cell (Logic AND)</td><td>ISOLANDX1</td></t<>	189	Hold 0 Isolation Cell (Logic AND)	ISOLANDX1
191       Hold 0 Isolation Cell (Logic AND)       ISOLANDX4         192       Hold 0 Isolation Cell (Logic AND)       ISOLANDX8         193       Hold 1 Isolation Cell (Logic OR)       ISOLORX1         194       Hold 1 Isolation Cell (Logic OR)       ISOLORX2         195       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         196       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         197       Low to High Level Shifter       LSUPX4         198       Low to High Level Shifter       LSUPX1         198       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX4         201       High to Low Level Shifter       LSUPX2         202       High to Low Level Shifter       LSDNX2         203       High to Low Level Shifter       LSDNX8         205       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         204       High to Low Level Shifter/ Low-Active Enable       LSUPENX4         205       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         206       Low to High Level Shifter/ Low-Active Enable       <	190	Hold 0 Isolation Cell (Logic AND)	ISOLANDX2
192       Hold 0 Isolation Cell (Logic AND)       ISOLANDX8         193       Hold 1 Isolation Cell (Logic OR)       ISOLORX1         194       Hold 1 Isolation Cell (Logic OR)       ISOLORX2         195       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         196       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         197       Low to High Level Shifter       LSUPX1         198       Low to High Level Shifter       LSUPX1         199       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX3         201       High to Low Level Shifter       LSUPX4         202       High to Low Level Shifter       LSDNX2         203       High to Low Level Shifter       LSDNX4         204       High Level Shifter/ Low-Active Enable       LSUPENX4         205       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         206       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         207       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         208       Low to High Level Shifter/ Low-Active Enable	191	Hold 0 Isolation Cell (Logic AND)	ISOLANDX4
193       Hold 1 Isolation Cell (Logic OR)       ISOLORX1         194       Hold 1 Isolation Cell (Logic OR)       ISOLORX2         195       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         196       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         197       Low to High Level Shifter       ISOLORX8         Level1Shifters       LSUPX1         197       Low to High Level Shifter       LSUPX1         198       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX4         201       High to Low Level Shifter       LSUPX3         202       High to Low Level Shifter       LSDNX1         203       High to Low Level Shifter       LSDNX2         203       High to Low Level Shifter/       LSDNX4         204       High to Low Level Shifter/       LSUPENX4         205       Low to High Level Shifter/       LSUPENX4         206       Low to High Level Shifter/       LSUPENX4         205       Low to High Level Shifter/       LSUPENX4         206       Low to High Level Shifter/       LSUPENX4         207       Low to High Level Shifter/       LSUPENX4 <td>192</td> <td>Hold 0 Isolation Cell (Logic AND)</td> <td>ISOLANDX8</td>	192	Hold 0 Isolation Cell (Logic AND)	ISOLANDX8
104       Hold 1 Isolation Cell (Logic OR)       ISOLORX2         195       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         196       Hold 1 Isolation Cell (Logic OR)       ISOLORX8         Level1Shifters       ISOLORX8         197       Low to High Level Shifter       LSUPX1         198       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX4         201       High to Low Level Shifter       LSDNX1         202       High to Low Level Shifter       LSDNX2         203       High to Low Level Shifter       LSDNX4         204       High to Low Level Shifter/ Low-Active Enable       LSUPENX1         205       Low to High Level Shifter/ Low-Active Enable       LSUPENX2         207       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         208       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         209       High to Low Level Shifter/ Low-Active Enable       LSUPENX4	193	Hold 1 Isolation Cell (Logic OR)	ISOLORX1
195       Hold 1 Isolation Cell (Logic OR)       ISOLORX4         196       Hold 1 Isolation Cell (Logic OR)       ISOLORX8         197       Low to High Level Shifter       LSUPX1         198       Low to High Level Shifter       LSUPX1         199       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX4         201       High to Level Shifter       LSUPX3         202       High to Low Level Shifter       LSDNX1         203       High to Low Level Shifter       LSDNX2         203       High to Low Level Shifter/ Low-Active Enable       LSUPENX4         204       High to Level Shifter/ Low-Active Enable       LSUPENX4         205       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         206       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         206       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         204       High to Low Level Shifter/ Low-Active Enable       LSUPENX4         205       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         206       Low to High Level Shi	194	Hold 1 Isolation Cell (Logic OR)	ISOLORX2
196       Hold 1 Isolation Cell (Logic OR)       ISOLORX8         197       Level1Shifters       LSUPX1         198       Low to High Level Shifter       LSUPX1         198       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX4         201       High to Low Level Shifter       LSDNX1         202       High to Low Level Shifter       LSDNX1         203       High to Low Level Shifter       LSDNX2         203       High to Low Level Shifter       LSDNX4         204       High to Low Level Shifter/       LSDNX4         205       Low to High Level Shifter/       LSDNX8         205       Low to High Level Shifter/       LSUPENX1         206       Low to High Level Shifter/       LSUPENX2         207       Low to High Level Shifter/       LSUPENX4         208       Low to High Level Shifter/       LSUPENX4         209       High to Low Level Shifter/       LSUPENX4         209       High to Low Level Shifter/       LSUPENX4         209       High to Low Level Shifter/       LSDNENX2	195	Hold 1 Isolation Cell (Logic OR)	ISOLORX4
Level1Shifters       LSUPX1         197       Low to High Level Shifter       LSUPX2         198       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX4         201       High to Low Level Shifter       LSDNX1         202       High to Low Level Shifter       LSDNX1         203       High to Low Level Shifter       LSDNX2         203       High to Low Level Shifter       LSDNX4         204       High to Low Level Shifter/       LSDNX8         205       Low to High Level Shifter/ Low-Active Enable       LSUPENX1         206       Low to High Level Shifter/ Low-Active Enable       LSUPENX2         207       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         208       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         209       High to Low Level Shifter/ Low-Active Enable       LSUPENX4         210       High to Low Level Shifter/ Low-Active Enable       LSDNENX2         211       High to Low Level Shifter/ Low-Active Enable       LSDNENX2 <td>196</td> <td>Hold 1 Isolation Cell (Logic OR)</td> <td>ISOLORX8</td>	196	Hold 1 Isolation Cell (Logic OR)	ISOLORX8
197       Low to High Level Shifter       LSUPX1         198       Low to High Level Shifter       LSUPX2         199       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX4         200       Low to High Level Shifter       LSUPX8         201       High to Low Level Shifter       LSDNX1         202       High to Low Level Shifter       LSDNX2         203       High to Low Level Shifter       LSDNX4         204       High to Low Level Shifter       LSDNX8         205       Low to High Level Shifter/ Low-Active Enable       LSUPENX1         206       Low to High Level Shifter/ Low-Active Enable       LSUPENX2         207       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         208       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         209       High to Low Level Shifter/ Low-Active Enable       LSUPENX4         210       High to Low Level Shifter/ Low-Active Enable       LSDNENX2         211       High to Low Level Shifter/ Low-Active Enable       LSDNENX4         212       High to Low Level Shifter/ Low-Active Enable       LSDNENX4         210       High to Lo		Level1Shifters	_
198Low to High Level ShifterLSUPX2199Low to High Level ShifterLSUPX4200Low to High Level ShifterLSUPX8201High to Low Level ShifterLSDNX1202High to Low Level ShifterLSDNX1203High to Low Level ShifterLSDNX2203High to Low Level ShifterLSDNX4204High to Low Level ShifterLSDNX4205Low to High Level Shifter/ Low-Active EnableLSUPENX1206Low to High Level Shifter/ Low-Active EnableLSUPENX2207Low to High Level Shifter/ Low-Active EnableLSUPENX4208Low to High Level Shifter/ Low-Active EnableLSUPENX4209High to Low Level Shifter/ Low-Active EnableLSUPENX4210High to Low Level Shifter/ Low-Active EnableLSDNENX1210High to Low Level Shifter/ Low-Active EnableLSDNENX4211High to Low Level Shifter/ Low-Active EnableLSDNENX2211High to Low Level Shifter/ Low-Active EnableLSDNENX4212High to Low Level Shifter/ Low-Active EnableLSDNENX4213High to Low Level Shifter/ Low-Active EnableLSDNENX4214High to Low Level Shifter/ Low-Active EnableLSDNENX4215High to Low Level Shifter/ Low-Active EnableLSDNENX4216Retention Flip-Flops and scan Flip-FlopsDEEEX4	197	Low to High Level Shifter	LSUPX1
109Low to High Level ShifterLSUPX4199Low to High Level ShifterLSUPX8200Low to High Level ShifterLSUPX8201High to Low Level ShifterLSDNX1202High to Low Level ShifterLSDNX2203High to Low Level ShifterLSDNX2204High to Low Level ShifterLSDNX8205Low to High Level Shifter/ Low-Active EnableLSUPENX1206Low to High Level Shifter/ Low-Active EnableLSUPENX2207Low to High Level Shifter/ Low-Active EnableLSUPENX4208Low to High Level Shifter/ Low-Active EnableLSUPENX4209High to Low Level Shifter/ Low-Active EnableLSUPENX8209High to Low Level Shifter/ Low-Active EnableLSDNENX1210High to Low Level Shifter/ Low-Active EnableLSDNENX1211High to Low Level Shifter/ Low-Active EnableLSDNENX2211High to Low Level Shifter/ Low-Active EnableLSDNENX4212High to Low Level Shifter/ Low-Active EnableLSDNENX8Retention Flip-Flops and scan Flip-FlopsDEFEX4203RDEFEX4RDEFEX4	198	Low to High Level Shifter	LSUPX2
100Low to High Level ShifterLSUPX8200Low to High Level ShifterLSUPX8201High to Low Level ShifterLSDNX1202High to Low Level ShifterLSDNX2203High to Low Level ShifterLSDNX4204High to Low Level ShifterLSDNX8205Low to High Level Shifter/ Low-Active EnableLSUPENX1206Low to High Level Shifter/ Low-Active EnableLSUPENX2207Low to High Level Shifter/ Low-Active EnableLSUPENX4208Low to High Level Shifter/ Low-Active EnableLSUPENX4209High to Low Level Shifter/ Low-Active EnableLSUPENX8209High to Low Level Shifter/ Low-Active EnableLSDNENX1210High to Low Level Shifter/ Low-Active EnableLSDNENX1211High to Low Level Shifter/ Low-Active EnableLSDNENX2211High to Low Level Shifter/ Low-Active EnableLSDNENX4212High to Low Level Shifter/ Low-Active EnableLSDNENX8213Retention Flip-Flops and scan Flip-FlopsDEEEX4	199	Low to High Level Shifter	LSUPX4
201High to Low Level ShifterLSDNX1202High to Low Level ShifterLSDNX2203High to Low Level ShifterLSDNX4204High to Low Level ShifterLSDNX8205Low to High Level Shifter/ Low-Active EnableLSUPENX1206Low to High Level Shifter/ Low-Active EnableLSUPENX2207Low to High Level Shifter/ Low-Active EnableLSUPENX4208Low to High Level Shifter/ Low-Active EnableLSUPENX4209High to Low Level Shifter/ Low-Active EnableLSUPENX8209High to Low Level Shifter/ Low-Active EnableLSDNENX1210High to Low Level Shifter/ Low-Active EnableLSDNENX1211High to Low Level Shifter/ Low-Active EnableLSDNENX2212High to Low Level Shifter/ Low-Active EnableLSDNENX4212High to Low Level Shifter/ Low-Active EnableLSDNENX4212High to Low Level Shifter/ Low-Active EnableLSDNENX4212High to Low Level Shifter/ Low-Active EnableLSDNENX8Retention Flip-Flops and scan Flip-FlopsDEEEX4	200	Low to High Level Shifter	LSUPX8
201High to Low Level ShifterLSDNX2202High to Low Level ShifterLSDNX4203High to Low Level ShifterLSDNX4204High to Low Level ShifterLSDNX8205Low to High Level Shifter/ Low-Active EnableLSUPENX1206Low to High Level Shifter/ Low-Active EnableLSUPENX2207Low to High Level Shifter/ Low-Active EnableLSUPENX4208Low to High Level Shifter/ Low-Active EnableLSUPENX4209High to Low Level Shifter/ Low-Active EnableLSUPENX8209High to Low Level Shifter/ Low-Active EnableLSDNENX1210High to Low Level Shifter/ Low-Active EnableLSDNENX2211High to Low Level Shifter/ Low-Active EnableLSDNENX4212High to Low Level Shifter/ Low-Active EnableLSDNENX4214High to Low Level Shifter/ Low-Active EnableLSDNENX8Retention Flip-Flops and scan Flip-FlopsPDEEX4	201	High to Low Level Shifter	LSDNX1
203High to Low Level ShifterLSDNX4204High to Low Level ShifterLSDNX8205Low to High Level Shifter/ Low-Active EnableLSUPENX1206Low to High Level Shifter/ Low-Active EnableLSUPENX2207Low to High Level Shifter/ Low-Active EnableLSUPENX4208Low to High Level Shifter/ Low-Active EnableLSUPENX4209High to Low Level Shifter/ Low-Active EnableLSUPENX8209High to Low Level Shifter/ Low-Active EnableLSDNENX1210High to Low Level Shifter/ Low-Active EnableLSDNENX2211High to Low Level Shifter/ Low-Active EnableLSDNENX4212High to Low Level Shifter/ Low-Active EnableLSDNENX4214Page Teles Patenties PEEPEEX4	202	High to Low Level Shifter	LSDNX2
204High to Low Level ShifterLSDNX8205Low to High Level Shifter/ Low-Active EnableLSUPENX1206Low to High Level Shifter/ Low-Active EnableLSUPENX2207Low to High Level Shifter/ Low-Active EnableLSUPENX4208Low to High Level Shifter/ Low-Active EnableLSUPENX4209High to Low Level Shifter/ Low-Active EnableLSUPENX1210High to Low Level Shifter/ Low-Active EnableLSDNENX1211High to Low Level Shifter/ Low-Active EnableLSDNENX2211High to Low Level Shifter/ Low-Active EnableLSDNENX4212High to Low Level Shifter/ Low-Active EnableLSDNENX4213High to Low Level Shifter/ Low-Active EnableLSDNENX4214Page Edge Detection DEFDEF215Data Edge Detection DEFDEF	203	High to Low Level Shifter	LSDNX4
205       Low to High Level Shifter/ Low-Active Enable       LSUPENX1         206       Low to High Level Shifter/ Low-Active Enable       LSUPENX2         207       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         208       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         209       High to Low Level Shifter/ Low-Active Enable       LSUPENX8         209       High to Low Level Shifter/ Low-Active Enable       LSDNENX1         210       High to Low Level Shifter/ Low-Active Enable       LSDNENX2         211       High to Low Level Shifter/ Low-Active Enable       LSDNENX4         212       High to Low Level Shifter/ Low-Active Enable       LSDNENX4         212       High to Low Level Shifter/ Low-Active Enable       LSDNENX8         Retention Flip-Flops and scan Flip-Flops       DEFEX1	204	High to Love Level Shifter	LSDNX8
206       Low to High Level Shifter/ Low-Active Enable       LSUPENX2         207       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         208       Low to High Level Shifter/ Low-Active Enable       LSUPENX8         209       High to Low Level Shifter/ Low-Active Enable       LSUPENX8         210       High to Low Level Shifter/ Low-Active Enable       LSDNENX1         210       High to Low Level Shifter/ Low-Active Enable       LSDNENX2         211       High to Low Level Shifter/ Low-Active Enable       LSDNENX4         212       High to Low Level Shifter/ Low-Active Enable       LSDNENX8         Retention Flip-Flops and scan Flip-Flops       DEEEX1	205	Low to High Level Shifter/ Low-Active Enable	LSUPENX1
200       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         207       Low to High Level Shifter/ Low-Active Enable       LSUPENX4         208       Low to High Level Shifter/ Low-Active Enable       LSUPENX8         209       High to Low Level Shifter/ Low-Active Enable       LSDNENX1         210       High to Low Level Shifter/ Low-Active Enable       LSDNENX2         211       High to Low Level Shifter/ Low-Active Enable       LSDNENX4         212       High to Low Level Shifter/ Low-Active Enable       LSDNENX8         Retention Flip-Flops and scan Flip-Flops       DEFEX1	206	Low to High Level Shifter/ Low-Active Enable	LSUPENX2
208       Low to High Level Shifter/ Low-Active Enable       LSUPENX8         209       High to Low Level Shifter/ Low-Active Enable       LSDNENX1         210       High to Low Level Shifter/ Low-Active Enable       LSDNENX2         211       High to Low Level Shifter/ Low-Active Enable       LSDNENX4         212       High to Low Level Shifter/ Low-Active Enable       LSDNENX4         212       High to Low Level Shifter/ Low-Active Enable       LSDNENX8         Retention Flip-Flops and scan Flip-Flops       DEFEX1	207	Low to High Level Shifter/ Low-Active Enable	LSUPENX4
209       High to Low Level Shifter/ Low-Active Enable       LSDNENX1         210       High to Low Level Shifter/ Low-Active Enable       LSDNENX2         211       High to Low Level Shifter/ Low-Active Enable       LSDNENX4         212       High to Low Level Shifter/ Low-Active Enable       LSDNENX4         212       High to Low Level Shifter/ Low-Active Enable       LSDNENX4         212       High to Low Level Shifter/ Low-Active Enable       LSDNENX8         Retention Flip-Flops and scan Flip-Flops       DEFEX1	208	Low to High Level Shifter/ Low-Active Enable	LSUPENX8
210       High to Low Level Shifter/ Low-Active Enable       LSDNENX2         211       High to Low Level Shifter/ Low-Active Enable       LSDNENX4         212       High to Low Level Shifter/ Low-Active Enable       LSDNENX8         Retention Flip-Flops and scan Flip-Flops       DEFEX1	209	High to Low Level Shifter/ Low-Active Enable	LSDNENX1
211       High to Low Level Shifter/ Low-Active Enable       LSDNENX4         212       High to Low Level Shifter/ Low-Active Enable       LSDNENX8         Retention Flip-Flops and scan Flip-Flops       DEFEX1	210	High to Low Level Shifter/ Low-Active Enable	LSDNENX2
211       High to Low Level Shifter/ Low-Active Enable       LSDNENX8         212       High to Low Level Shifter/ Low-Active Enable       LSDNENX8         Retention Flip-Flops and scan Flip-Flops       DEFEX1	211	High to Low Level Shifter/ Low-Active Enable	I SDNENX4
Retention Flip-Flops     PDEFX1	212	High to Low Level Shifter/ Low-Active Enable	I SDNENX8
Dec Edge Detertion DEE		Retention Flin-Flops and scan Flin-Flops	
1213 POS EDDE RETENTION DEE	213	Pos Edge Retention DEF	RDFFX1

No	Cell Description	Cell Name
214	Pos Edge Retention DFF	RDFFX2
215	Scan Pos Edge Retention DFF	RSDFFX1
216	Scan Pos Edge Retention DFF	RSDFFX2
217	Neg Edge Retention DFF	RDFFNX1
218	Neg Edge Retention DFF	RDFFNX2
219	Scan Neg Edge Retention DFF	RSDFFNX1
220	Scan Neg Edge Retention DFF	RSDFFNX2
	Power Gating Cells	
221	Header Cell	HEADX2
222	Header Cell	HEADX4
223	Header Cell	HEADX8
224	Header Cell	HEADX16
225	Header Cell	HEADX32
	Always on Cells	
226	Always on Inverter	AOINVX1
227	Always on Inverter	AOINVX2
228	Always on Inverter	AOINVX4
229	Always on Non-inverting Buffer	AOBUFX1
230	Always on Non-inverting Buffer	AOBUFX2
231	Always on Non-inverting Buffer	AOBUFX4
232	Always on Pos Edge DFF, w/ Async Low-Active Reset	AODFFARX1
233	Always on Pos Edge DFF, w/ Async Low-Active Reset	AODFFARX2
234	Always on Neg Edge DFF, w/ Async Low-Active Reset	AODFFNARX1
235	Always on Neg Edge DFF, w/ Async Low-Active Reset	AODFFNARX2
	Additional Cells	
236	Bus Keeper	BUSKP
237	P-MOSFET (w=1.12 um, l=0.1um)	PMT1
238	P-MOSFET (w=2.24 um, I=0.1um)	PMT2
239	P-MOSFET (w=4.48 um, I=0.1um)	PMT3
240	N-MOSFET (w=0.48 um, I=0.1um)	NMT1
241	N-MOSFET (w=0.96 um, I=0.1um)	NMT2
242	N-MOSFET (w=1.92 um, I=0.1um)	NMT3
243	Tie High	TIEH
244	Tie Low	TIEL
245	Antenna Diode	ANTENNA
246	Decoupling Capacitance	DCAP
247	Capacitive Load	CLOAD1
	Fillers	
248	Sinale Heiaht Filler Cell 2 grid width	SHFILL2
249	Double Heiaht (hiah-low-high) Filler Cell 2 grid width	DHFILLHLH2
250	Double Height (low-high-low) Filler Cell 2 grid width	DHFILLLHL2
251	Double Height (high-low-high) Level Shifter Filler Cell 11 grid width	DHFILLHLHLS11

Ν	Туре	Description
1	.doc, .txt	Databook / User guide, Layer usage file
2	.sdb, .slib	Symbols
3	.db, .lib	Synthesis
4	.V	Verilog simulation models
5	.vhd	VHDL / Vital simulation models
6	.sp	HSPICE netlists
7	.rcx	Extracted RC netlists for different corners
8	.gds	GDSII layout views
9	.drc, .lvs, .erc	Report files
10	.lef	LEF files
11	.fram, .cel	Fram views, layout views and runset files
12	.plib	Physical compiler views

Table 7.1. Digital Standard Cell Library deliverables

### 8. Physical structure of digital cell

The selection of physical structure of digital cell is aimed at providing maximum cell density in digital designs. It is more important to provide minimal area for the most frequently used cells. In general, these are usually NAND cells with two inputs, and D flip-flops. The width of the power rails has been selected on the basis of acceptable current density given by the design rules, and electromigration. Physical structures, shown in Fig.8.1-8.5, have been used for different cells.



Figure 8.1. Physical structure of single height digital standard cells



Figure 8.2. Physical structure of double height (low-high-low) digital standard cells (for Always on Cells)



Figure 8.3. Physical structure of double height (high-low-high) digital standard cells (for Level-Shifter cells: Low-High



Figure 8.4. Physical structure of single height digital standard cells (for Level-shifter cells: High-Low)



Figure 8.5. Physical structure of single height digital standard cells (for Retention Flip-Flops and scan Flip-Flops)

Parameter	Symbol	Value
Cell height	Н	2.88 um
Power rail width	W <sub>1</sub>	0.16 um
Vertical grid	W <sub>2</sub>	0.32 um
Horizontal grid	W <sub>3</sub>	0.32 um
NWell height	W4	1.68 um
VDDH to VDDL height (Fig. 8.3)	$W_5$	0.72 um

Table 8.1. Physical structure dimensions

 $d_{track}$  is the minimum center-to-center distance for metal2 layers (with VIA12



Minimum center-to-center distance

### 9. Descriptions of Digital Standard Cells

Inverters: INVX0, INVX1, INVX2, INVX4, INVX8, INVX16, INVX32



Figure 9.1. Logic Symbol of Inverting Buffer

#### Table 9.1. Inverter Truth Table

IN	QN
0	1
1	0

#### Table 9.2. Inverter Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
Cell		oad Prop Delay (Avg)	Po	wer	Area
Name Cloa	Cload		Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
INVX1	1 x Csl	38	88	12	6.4512
INVX8	8 x Csl	39	582	78	14.7456
INVX32	32 x Csl	41	2510	358	47.0016

Inverting Buffers: IBUFFX2, IBUFFX4, IBUFFX8, IBUFFX16, IBUFFX32



Figure 9.2. Logic Symbol of Inverting Buffer

Table 9.3. Inverting Buffer Truth Table

IN QN		
0	1	
1	0	

#### Table 9.4. Inverting Buffer Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF				
0.11.11			Pov	wer	Area
Cell Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
IBUFFX2	2 x Csl	98	223	92	10.1376
IBUFFX8	8 x Csl	131	833	339	18.4320
IBUFFX32	32 x Csl	205	3315	2090	56.2176



Figure 9.3. Logic Symbol of Non-inverting Buffer

Table 9.5. Non-inverting Buffer Truth Table



#### Table 9.6. Non-inverting Buffer Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF				
			Power		Area
Cell Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
NBUFFX2	2 x Csl	77	201	79	5.5296
NBUFFX8	8 x Csl	101	742	330	14.7456
NBUFFX32	32 x Csl	168	3125	1284	55.2960

Tri-state Non-inverting Buffer w/ High-Active Enable: TNBUFFX1, TNBUFFX2, TNBUFFX4, TNBUFFX8, TNBUFFX16, TNBUFFX32



Figure 9.4. Logic Symbol of Tri-state Non-inverting Buffer w/ High-Active Enable

Table 9.7. Tri-state Non-inverting Buffer w/ High-Active Enable Truth Table

ENB	IN	Q
0	0	Ζ
0	1	Z
1	0	0
1	1	1

**SALIGHZAZ** 

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF						
0.11.11			wer	Area			
Cell Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic			
		ps	nW	nW/MHz	(um²)		
TNBUFFX1	1 x Csl	101	450	63	13.8240		
TNBUFFX8	8 x Csl	141	1110	337	23.9616		
TNBUFFX32	32 x Csl	138	4100	3672	68.1984		

Table 9.8. Tri-state Non-inverting Buffer w/ High-Active Enable Electrical Parameters and Areas

#### AND: AND2X1, AND2X2, AND2X4, AND3X1, AND3X2, AND3X4, AND4X1, AND4X2, AND4X4



Figure 9.5. Logic Symbol of AND

#### Table 9.9. AND Truth Table (n=2,3,4)

IN1	IN2		INn	Q
0	Х		Х	0
Х	0		Х	0
				0
Х	Х		0	0
1	1	1	1	1

#### Table 9.10. AND Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
			Pov	wer	Area
Cen name	Cload	Prop Delay (Avg)	Delay (Avg) (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
AND2X1	1 x Csl	85	298	19	7.3728
AND2X2	2 x Csl	96	568	36	8.2944
AND3X1	1 x Csl	119	297	34	8.2944
AND3X2	2 x Csl	135	562	55	10.1376
AND4X1	1 x Csl	129	299	42	10.1376
AND4X2	2 x Csl	147	574	75	11.9808

NAND: NAND2X0, NAND2X1, NAND2X2, NAND2X4, NAND3X0, NAND3X1, NAND3X2, NAND3X4, NAND4X0, NAND4X1



Figure 9.6. Logic Symbol of NAND

#### Table 9.11. NAND Truth Table (n=2,3,4)

IN1	IN2		INn	QN
0	Х		Х	1
Х	0		Х	1
				1
Х	Х		0	1
1	1	1	1	0

#### Table 9.12. NAND Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
			Pov	wer	Area
Cell Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
NAND2X1	1 x Csl	51	336	15	5.5296
NAND2X2	2 x Csl	51	673	28	9.2160
NAND3X1	1 x Csl	130	492	38	11.9808
NAND3X2	2 x Csl	142	770	59	12.9024
NAND4X0	0.5 x Csl	66	400	22	8.2944
NAND4X1	1 x Csl	127	716	57	12.9024

OR: OR2X1, OR2X2, OR2X4, OR3X1, OR3X2, OR3X4, OR4X1, OR4X2, OR4X4



Figure 9.7. Logic Symbol of OR

IN1	IN2		INn	Q
0	0		0	0
1	X		X	1
				1
Х	1		X	1
Х	X	Х	1	1

#### Table 9.13. OR Truth Table (n=2,3,4)

### Table 9.14. OR Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
			Pov	wer	Area
Cell Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
OR2X1	1 x Csl	85	226	23	7.3728
OR2X2	2 x Csl	94	409	37	9.2160
OR3X1	1 x Csl	114	250	39	9.2160
OR3X2	2 x Csl	121	435	62	11.0592
OR4X1	1 x Csl	137	261	56	10.1376
OR4X2	2 x Csl	153	449	93	11.9808

NOR: NOR2X0, NOR2X1, NOR2X2, NOR2X4, NOR3X0, NOR3X1, NOR3X2, NOR3X4, NOR4X0, NOR4X1



Figure 9.8. Logic Symbol of NOR

Table 9.15. NOR Truth Table (n=2,3,4)

IN1	IN2		INn	QN
0	0		0	1
1	Х		Х	0
				0
Х	1		Х	0
Х	Х	Х	1	0

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF				
	Cload	Prop Delay (Avg)	Power		Area
			Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
NOR2X1	1 x Csl	64	170	15	6.4512
NOR2X2	2 x Csl	66	340	29	9.2160
NOR3X1	1 x Csl	136	374	45	11.9808
NOR3X2	2 x Csl	147	558	67	13.8240
NOR4X0	0.5 x Csl	95	168	27	9.2160
NOR4X1	1 x Csl	124	414	50	15.6672

### Table 9.16. NOR Electrical Parameters and Areas

#### XOR: XOR2X1, XOR2X2, XOR3X1, XOR3X2



Figure 9.9. Logic Symbol of XOR

### Table 9.17. XOR Truth Table (n=2,3)

IN1	IN2		INn	Q
0	0		0	0
Odd number of 1's				1
Even number of 1's			0	

#### Table 9.18. XOR Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
			Power		Area
	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
XOR2X1	1 x Csl	133	454	26	13.8240
XOR2X2	2 x Csl	144	723	37	15.6672
XOR3X1	1 x Csl	218	852	77	22.1184
XOR3X2	2 x Csl	253	1154	127	23.9616
# XNOR: XNOR2X1, XNOR2X2, XNOR3X1, XNOR3X2



Figure 9.10. Logic Symbol of XNOR

# Table 9.19. XNOR Truth Table (n=2,3)

IN1	IN2		INn	QN
0	1			
Oc	0			
Eve	1			

#### Table 9.20. XNOR Electrical Parameters and Areas

	Operating Condition Operating Frequent Capacitive Standar	Dperating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Dperating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
			Po	wer	Area	
Cell Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	nW/MHz	(um²)	
XNOR2X1	1 x Csl	136	933	25	13.8240	
XNOR2X2	2 x Csl	151	706	9	15.6672	
XNOR3X1	1 x Csl	229	909	81	22.1184	
XNOR3X2	2 x Csl	252	1196	94	23.9616	

## AND-OR: AO21X1, AO21X2 Q=(1&2)|3



Figure 9.11. Logic Symbol of AND-OR 2/1

#### Table 9.21. AND-OR 2/1 Truth Table

IN1	IN2	IN3	Q
1	1	Х	1
Х	Х	1	1
0	Х	0	0
Х	0	0	0

Table 9.22. AND-OR 2/1 Electrical Parameters and Areas						
Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF						
Cell		Power				
Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	nW/MHz	(um²)	
AO21X1	1 x Csl	109	322	35	10.1376	
AO21X2	2 x Csl	131	595	67	11.9808	

## AND-OR: AO22X1, AO22X2 Q=(1&2)|(3&4)



Figure 9.12. Logic Symbol of AND-OR 2/2

|--|

IN1	IN2	IN3	IN4	Q
Х	Х	1	1	1
1	1	Х	Х	1
0	Х	0	Х	0
Х	0	0	Х	0
0	Х	Х	0	0
Х	0	Х	0	0

# Table 9.24. AND-OR 2/2 Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
Cell			Area		
Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
AO22X1	1 x Csl	119	333	42	11.9808
AO22X2	2 x Csl	141	608	80	12.9024

AND-OR: AO221X1, AO221X2 Q=(1&2)|(3&4)|5



Figure 9.13.	Logic Symbol of AND-OR 2/2/1
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	Table 9.25.	AND-OR	2/2/1	Truth	Table
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IN1	IN2	IN3	IN4	IN5	Q
1	1	Х	Х	Х	1
Х	Х	1	1	Х	1
Х	Х	Х	Х	1	1
0	Х	0	Х	0	0
Х	0	0	Х	0	0
0	Х	Х	0	0	0
Х	0	Х	0	0	0

#### Table 9.26. AND-OR 2/2/1 Electrical Parameters and Areas

Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					
Cell			Pov	wer	Area
Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
AO221X1	1 x Csl	150	353	53	12.9024
AO221X2	2 x Csl	168	629	89	14.7456

AND-OR: AO222X1, AO222X2 Q=(1&2)|(3&4)|(5&6)



Figure 9.14. Logic Symbol of AND-OR 2/2/2

#### Table 9.27. AND-OR 2/2/2 Truth Table

IN1	IN2	IN3	IN4	IN5	IN6	Q
1	1	Х	Х	Х	Х	1
Х	Х	1	1	Х	Х	1
Х	Х	Х	Х	1	1	1
0	0	0	0	0	0	0

#### Table 9.28. AND-OR 2/2/2 Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
Cell			Pov	wer	Area
Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
AO222X1	1 x Csl	162	365	53	14.7456
AO222X2	2 x Csl	176	642	85	15.6672

## AND-OR-Invert: AOI21X1, AOI21X2 QN=!((1&2)|3)



Figure 9.15. Logic Symbol of AND-OR-Invert 2/1

IN1	IN2	IN3	QN
1	1	Х	0
Х	Х	1	0
0	Х	0	1
X	0	0	1

# Table 9.29. AND-OR-Invert 2/1 Truth Table

# Table 9.30. AND-OR-Invert 2/1 Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
Cell			Pov	wer	Area
Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
AOI21X1	1 x Csl	136	437	47	11.9808
AOI21X2	2 x Csl	146	708	72	12.9024

#### AND-OR-Invert: AOI22X1, AOI22X2 QN=!((1&2)|(3&4))



Figure 9.16. Logic Symbol of AND-OR-Invert 2/2

#### Table 9.31. AND-OR-Invert 2/2 Truth Table

IN1	IN2	IN3	IN4	QN
Х	Х	1	1	0
1	1	Х	Х	0
0	Х	0	Х	1
Х	0	0	Х	1
0	Х	Х	0	1
Х	0	Х	0	1

Table 9.32. AND-OR-Invert 2/2 Electrical Parameters and Areas							
	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF						
Cell	Cload	Prop Delay (Avg)	Power		Area		
Name			Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic			
		ps	nW	nW/MHz	(um²)		
AOI22X1	1 x Csl	154	435	45	12.9024		
AOI22X2	2 x Csl	175	708	71	14.7456		

AND-OR-Invert: AOI221X1, AOI221X2 QN=!((1&2)|(3&4)|5)





IN1	IN2	IN3	IN4	IN5	QN
1	1	Х	Х	Х	0
Х	Х	1	1	Х	0
Х	Х	Х	Х	1	0
0	Х	0	Х	0	1
Х	0	0	Х	0	1
0	Х	Х	0	0	1
Х	0	Х	0	0	1

Table 9.33.	AND-OR-Invert 2/2/1	Truth	Table
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Table 9.34. AND-OR-Invert 2/2/1 Electrical Parameters and Areas							
	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF						
Cell Name	Cload	Prop Delay (Avg)	Power		Area		
			Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic			
		ps	nW	nW/MHz	(um²)		
AOI221X1	1 x Csl	183	507	57	14.7456		
AOI221X2	2 x Csl	192	779	81	15.6672		

AND-OR-Invert: AOI222X1, AOI222X2 QN=!((1&2)|(3&4)|(5&6))



Figure 9.18. Logic Symbol of AND-OR-Invert 2/2/2

IN1	IN2	IN3	IN4	IN5	IN6	QN
1	1	Х	Х	Х	Х	0
Х	Х	1	1	Х	Х	0
Х	Х	Х	Х	1	1	0
0	0	0	0	0	0	1

#### Table 9.35. AND-OR-Invert 2/2/2 Truth Table

#### Table 9.36. AND-OR-Invert 2/2/2 Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
Cell			Pov	wer	Area
Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
AOI222X1	1 x Csl	182	527	57	15.6672
AOI222X2	2 x Csl	199	799	79	17.5104

OR-AND: OA21X1, OA21X2 Q=(1|2)&3



Figure 9.19. Logic Symbol of OR-AND 2/1

Table 9.37. OR-AND 2/1 Truth Table

IN1	IN2	IN3	Q
0	0	Х	0
Х	Х	0	0
1	Х	1	1
Х	1	1	1

Table 9.38. OR-AND 2/1 Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
Cell			Pov	wer	Area
Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um <sup>2</sup> )
OA21X1	1 x Csl	118	302	34	9.2160
OA21X2	2 x Csl	120	584	62	11.0592

OR-AND: OA22X1, OA22X2 Q=(1|2)&(3|4)



Figure 9.20. Logic Symbol of OR-AND 2/2

IN1	IN2	IN3	IN4	Q
0	0	Х	Х	0
Х	Х	0	0	0
1	Х	1	Х	1
Х	1	1	Х	1
1	Х	Х	1	1
Х	1	Х	1	1

# Table 9.39. OR-AND 2/2 Truth Table

#### Table 9.40. OR-AND 2/2 Electrical Parameters and Areas

Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					
Cell			Pov	wer	Area
Name Cload	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
OA22X1	1 x Csl	115	332	45	11.0592
OA22X2	2 x Csl	130	606	74	12.9024

#### OR-AND: OA221X1, OA221X2 Q=(1|2)&(3|4)&5



Figure 9.21. Logic Symbol of OR-AND 2/2/1

IN1	IN2	IN3	IN4	IN5	Q
0	0	Х	Х	Х	0
Х	Х	0	0	Х	0
Х	Х	Х	Х	0	0
1	Х	1	Х	1	1
Х	1	1	Х	1	1
1	Х	Х	1	1	1
Х	1	Х	1	1	1

#### Table 9.41. OR-AND 2/2/1 Truth Table

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					
Cell Name Cload		Pov Leakage	wer	Area		
	Cload	Prop Delay (Avg)	(VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	nW/MHz	(um²)	
OA221X1	1 x Csl	145	350	53	12.9024	
OA221X2	2 x Csl	164	590	90	14.7456	

Table 9.42. OR-AND 2/2/1 Electrical Parameters and Areas

OR-AND: OA222X1, OA222X2 Q=(1|2)&(3|4)&(5|6)



Figure 9.22. Logic Symbol of OR-AND 2/2/2

## Table 9.43. OR-AND 2/2/2 Truth Table

IN1	IN2	IN3	IN4	IN5	IN6	Q
0	0	Х	Х	Х	Х	0
Х	Х	0	0	Х	Х	0
Х	Х	Х	Х	0	0	0
1	Х	1	Х	1	Х	1
1	Х	1	Х	Х	1	1
1	Х	Х	1	1	Х	1
1	Х	Х	1	Х	1	1
Х	1	1	Х	1	Х	1
Х	1	1	Х	Х	1	1
Х	1	Х	1	1	Х	1
Х	1	Х	1	Х	1	1

Cable 9.44. OR-AND 2/2/2 Electrical Parameters and Areas							
Cell Name			Pov	wer	Area		
	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic			
		ps	nW	nW/MHz	(um²)		
OA222X1	1 x Csl	168	375	59	14.7456		
OA222X2	2 x Csl	192	608	102	15.6672		

OR-AND-Invert: OAI21X1, OAI21X2 QN=!((1|2)&3)



Figure 9.23. Logic Symbol of OR-AND-INVERT 2/1

#### Table 9.45. OR-AND-INVERT 2/1 Truth Table

IN1	IN2	IN3	QN
0	0	Х	1
Х	Х	0	1
1	Х	1	0
Х	1	1	0

## Table 9.46. OR-AND-INVERT 2/1 Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
Cell			Pov	wer	Area	
Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	nW/MHz	(um²)	
OAI21X1	1 x Csl	138	443	48	11.0592	
OAI21X2	2 x Csl	148	715	72	11.9808	

OR-AND-Invert: OAI22X1, OAI22X2 QN=!((1|2)&(3|4))



Figure 9.24. Logic Symbol of OR-AND-INVERT 2/2

#### Table 9.47. OR-AND-INVERT 2/2 Truth Table

IN1	IN2	IN3	IN4	QN
0	0	Х	Х	1
Х	Х	0	0	1
1	Х	1	Х	0
Х	1	1	Х	0
1	Х	Х	1	0
Х	1	Х	1	0

#### Table 9.48. OR-AND-INVERT 2/2 Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					
Cell Name			Pov	wer	Area	
	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	nW/MHz	(um²)	
OAI22X1	1 x Csl	159	498	50	12.9024	
OAI22X2	2 x Csl	169	770	77	13.8240	

#### OR-AND-Invert: OAI221X1, OAI221X2 QN=!((1|2)&(3|4)&5)



Figure 9.25. Logic Symbol of OR-AND-INVERT 2/2/1

IN1	IN2	IN3	IN4	IN5	QN
0	0	Х	Х	Х	1
Х	Х	0	0	Х	1
Х	Х	Х	Х	0	1
1	Х	1	Х	1	0
Х	1	1	Х	1	0
1	Х	Х	1	1	0
Х	1	Х	1	1	0

# Table 9.49. OR-AND-INVERT 2/2/1 Truth Table

## Table 9.50. OR-AND-INVERT 2/2/1 Electrical Parameters and Areas

Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
Cell			Pov	wer	Area
Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
OAI221X1	1 x Csl	194	499	57	14.7456
OAI221X2	2 x Csl	210	771	88	15.6672

#### OR-AND-Invert: OAI222X1, OAI222X2 QN=!((1|2)&(3|4)&(5|6))



Figure 9.26. Logic Symbol of OR-AND-INVERT 2/2/2

IN1	IN2	IN3	IN4	IN5	IN6	QN
0	0	Х	Х	Х	Х	1
Х	Х	0	0	Х	Х	1
Х	Х	Х	Х	0	0	1
1	Х	1	Х	1	Х	0
1	Х	1	Х	Х	1	0
1	Х	Х	1	1	Х	0
1	Х	Х	1	Х	1	0
Х	1	1	Х	1	Х	0
Х	1	1	Х	Х	1	0
Х	1	Х	1	1	Х	0
Х	1	Х	1	Х	1	0

# Table 9.51. OR-AND-INVERT 2/2/2 Truth Table

#### Table 9.52. OR-AND-INVERT 2/2/2 Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
Cell			Ρον	wer	Area	
Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	nW/MHz	(um²)	
OAI222X1	1 x Csl	235	475	62	15.6672	
OAI222X2	2 x Csl	252	737	93	17.5104	

#### Multiplexer 2 to 1: MUX21X1, MUX21X2



Figure 9.27. Logic Symbol of Multiplexer 2 to 1

Table 9.53. Multiplexer 2 to 1 Truth Table

S	Q
0	IN1
1	IN2

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	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
Cell	Cell Name Cload		Pov	wer	Area	
Name Cload		Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	nW/MHz	(um²)	
MUX21X1	1 x Csl	107	815	43	11.0592	
MUX21X2	2 x Csl	120	881	70	12.9024	

Table 9.54. Multiplexer 2 to 1 Electrical Parameters and Areas

Multiplexer 4 to 1: MUX41X1, MUX41X2



Figure 9.28. Logic Symbol of Multiplexer 4 to 1

Table 9.55. Multiplexer 4 to 1 Truth Table

S1	S0	Q
0	0	IN1
0	1	IN2
1	0	IN3
1	1	IN4

## Table 9.56. Multiplexer 4 to 1 Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
Cell			Pov	wer	Area	
Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	nW/MHz	(um²)	
MUX41X1	1 x Csl	168	827	58	23.0400	
MUX41X2	2 x Csl	189	1138	98	24.8832	

### Decoder 2 to 4: DEC24X1, DEC24X2



Figure 9.29. Logic Symbol of Decoder 2 to 4

#### Table 9.57. Decoder 2 to 4 Truth Table

IN2	IN1	Q0	Q1	Q2	Q3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

### Table 9.58. Decoder 2 to 4 Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
Oall Marris				Pow	er	Area
Cell Name	Cload	Output	Prop Delay (Avg) Clk to OUT	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um²)
		Q0	119			
	1 v Cal	Q1	119	1000	66	20 4012
DEC24X1	1 X 0 51	Q2	83	1230	00	29.4912
		Q3	79			
		Q0	156			
		Q1	154	2112	161	36 8640
	2 X 051	Q2	117	2112	101	30.0040
		Q3	115			

Half Adder 1-Bit: HADDX1, HADDX2



Figure 9.30. Logic Symbol of Half Adder 1-Bit

A0	B0	S0 (sum)	C1 (carry)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

# Table 9.59. Half Adder 1-Bit Truth Table

#### Table 9.60. Half Adder 1-Bit Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					
<b>A H N H</b>				Pow	er	Area
Cell Name	Cload	Output	Prop Delay (Avg) Clk to OUT (S0, C1)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um²)
	1 x Csl	S0	98	0.45	65	45.0070
HADDX1		C1	125	645	65	15.6672
	2 x Csl	S0	107	1100	106	19 4220
ΠΑΟΟΛΖ		C1	130	1100		10.4320

Full Adder 1-Bit: FADDX1, FADDX2



Figure 9.31. Logic Symbol of Full Adder 1-Bit

#### Table 9.61. Full Adder 1-Bit Truth Table

А	В	CI	S (sum)	CO (carry)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					
				Pow	ver	Area
Cell Name	Cload	Output Clk t	Prop Delay (Avg) Clk to OUT (S, CO)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um²)
FADDX1	1 x Csl	S CO	166 125	31	105	29.4912
	2 x Csl	S	185	- 56	165	24.2244
FADDXZ		CO	138			31.3344

Table 9.62. Full Adder 1-Bit Electrical Parameters and Areas

Pos Edge DFF: DFFX1, DFFX2



Figure 9.32. Logic Symbol of Pos Edge DFF

#### Table 9.63. Pos Edge DFF Transition Table

D	CLK	Q	QN
Х	Inactive	No change	No change
1	Rise	1	0
0	Rise	0	1

## Table 9.64. Pos Edge DFF Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF						
				Pow	ver	Area	
Cell Name	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW	nW/MHz	(um²)	
DEEVA	1 ··· Oal	Q	213	070	470	04.0000	
DFFX1	1 x CSI	QN	167	670	170	24.8832	
DEEV2	FFX2 2 x Csl	2 x Csl Q QN	253	1040	330	21 2244	
υγγλα			179			31.3344	

Pos Edge DFF w/Async Low-Active Set: DFFASX1, DFFASX2



Figure 9.33. Logic Symbol of Pos Edge DFF w/Async Low-Active Set

Table 9.65. Pos Edge DFF w/Async Low-Active Set Transition Table

D	SETB	CLK	Q	QN
Х	0	Х	1	0
Х	1	Inactive	No change	No change
1	1	Rise	1	0
0	1	Rise	0	1

Table 9.66. Pos Edge DFF w/Async Low-Active Set Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF						
				Pow	er	Area	
Cell Name	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW	nW/MHz	(um²)	
	1 v Cal	Q	253	000	400	24.2244	
DFFASX1	1 X CSI	QN	204	680	120	31.3344	
	2 x Csl	Q	281	- 1040	160	24 0002	
DEFRONZ		QN	204		160	34.0992	

Pos Edge DFF w/Async Low-Active Reset: DFFARX1, DFFARX2



Figure 9.34. Logic Symbol of Pos Edge DFF w/Async Low-Active Reset



D	RSTB	CLK	Q	QN
Х	0	Х	0	1
Х	1	Inactive	No change	No change
1	1	Rise	1	0
0	1	Rise	0	1

Table 9.67. Pos Edge DFF w/Async Low-Active Reset Transition Table

# Table 9.68. Pos Edge DFF w/Async Low-Active Reset Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF						
				Pow	er	Area	
Cell Name	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW	nW/MHz	(um²)	
DFFARX1	1 x Csl	Q QN	217 162	620	100	32.2560	
DFFARX2	2 x Csl	Q QN	264 179	970	130	34.0992	

Pos Edge DFF w/Async Low-Active Set & Reset: DFFASRX1, DFFASRX2



Figure 9.35. Logic Symbol of Pos Edge DFF w/Async Low-Active Set & Reset

Table 9.69. Pos Edge DFF w/Async Low-Active Set & Reset Transition Table
--

D	SETB	RSTB	CLK	Q	QN	Notes
Х	0	0	Х	Х	Х	Not Allowed
Х	0	1	Х	1	0	
Х	1	0	Х	0	1	
Х	1	1	Inactive	No change	No change	
1	1	1	Rise	1	0	
0	1	1	Rise	0	1	

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF						
0.11.11				Pow	er	Area	
Cell Name	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW	nW/MHz	(um²)	
DFFASRX1	1 x Csl	Q QN	251 190	680	80	35.0208	
DFFASRX2	2 x Csl	Q QN	302 215	1030	110	36.8640	

Table 9.70. Pos Edge DFF w/Async Low-Active Set & Reset Electrical Parameters and Areas

Pos Edge DFF w/ Sync Low-Active Set & Reset: DFFSSRX1, DFFSSRX2



Figure 9.36. Logic Symbol of Pos Edge DFF w/ Sync Low-Active Set & Reset

Table	Table 9.71. FOS Edge DIT W/ Sync Low-Active Set & Reset Transition Table								
D	SETB	RSTB	CLK	Q	QN	Notes			
Х	Х	Х	Inactive	No change	No change				
0	1	1	Rise	0	1				
1	1	1	Rise	1	0				
Х	0	1	Rise	1	0				
Х	1	0	Rise	0	1				

Х

Table 9.71. Pos Edge DFF w/ Sync Low-Active Set & Reset Transition Table

0

0

Rise

Х

Not Allowed

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able 9.72. Fos Edge DFF W/ Sync Low-Active Set & Reset Electrical Parameters and Areas							
	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF						
<b>A 1 N</b>				Pow	ver	Area	
Cell Name	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW	nW/MHz	(um²)	
DFFSSRX1	1 x Csl	Q	208	950	238	33.1776	
		QN	166				
DFFSSRX2	2 x Csl	Q QN	257 191	1300	396	37.7856	

Table 9.72. Pos Edge DFF w/ Sync Low-Active Set & Reset Electrical Parameters and Ar

Neg Edge DFF: DFFNX1, DFFNX2



Figure 9.37. Logic Symbol of Neg Edge DFF

#### Table 9.73. Neg Edge DFF Transition Table

D	CLK Q		QN
Х	Inactive	No change	No change
1	Fall	1	0
0	Fall	0	1

#### Table 9.74. Neg Edge DFF Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
				Pow	er	Area
Cell Name	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um²)
	1 v Cal	Q	233	005	00	28 5000
DFFNX1	1 x Csi	QN	189	805	96	28.5696
		Q	296	1742	154	21 2244
DEFINAZ	2 X USI	QN	223			51.3344

Neg Edge DFF w/Async Low-Active Set: DFFNASX1, DFFNASX2



Figure 9.38. Logic Symbol of Neg Edge DFF w/Async Low-Active Set

Table 9.75. Neg Edge	DFF w/Async Low-Act	tive Set Transition Table
5 5	,	

D	SETB	CLK	Q	QN
Х	0	Х	1	0
Х	1	Inactive	No change	No change
1	1	Fall	1	0
0	1	Fall	0	1

Table 9.76. Neg Edge DFF w/Async Low-Active Set Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
<b>A H N H</b>				Pow	er	Area
Cell Name	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um²)
	1 · · · Oal	l al Q	298	640	0.0	20,4400
DFFNASX1	1 X CSI	QN	245		90	30.4128
DFFNASX2	2 x Csl	Q	340	1010	150	24 0002
		QN	256			34.0992

Neg Edge DFF w/Async Low-Active Reset: DFFNARX1, DFFNARX2



Figure 9.39. Logic Symbol of Neg Edge DFF w/Async Low-Active Reset



D	RSTB	CLK	Q	QN
Х	0	Х	0	1
Х	1	Inactive	No change	No change
1	1	Fall	1	0
0	1	Fall	0	1

# Table 9.77. Neg Edge DFF w/Async Low-Active Reset Transition Table

Table 9.78. Neg Edge DFF w/Async Low-Active Reset Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					
				Pow	ver	Area
Cell Name	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um²)
	4	Q	268	000	404	20.0500
DFFNARX1	1 X CSI	QN	206	626	101	32.2560
		Q	306	999	145	24 0002
DEFINARAZ	2 X USI	QN	208			34.0992

Neg Edge DFF w/Async Low-Active Set & Reset: DFFNASRX1, DFFNASRX2



Figure 9.40. Logic Symbol of Neg Edge DFF w/Async Low-Active Set & Reset

Table 9.79. Neg Edge DFF w/Async Low-Active Set & Reset Transition Table
--

D	SETB	RSTB	CLK	Q	QN	Notes
Х	0	0	Х	Х	Х	Not Allowed
Х	0	1	Х	1	0	
Х	1	0	Х	0	1	
Х	1	1	Inactive	No change	No change	
1	1	1	Fall	1	0	
0	1	1	Fall	0	1	

Table 9.80. Neg Edge DFF w/Async Low-Active Set & Reset Electrical Parameters and Areas								
	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF							
				Pow	er	Area		
Cell Name	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic			
			ps	nW	nW/MHz	(um²)		
	1 v Col	Q	314	620	102	25.0209		
DFFNASRX1	T X USI	QN	248	620	103	35.0206		
	2 x Csl	Q	344	1040	162	36 8640		
	2 × 03	QN	253	1040		00.0040		

Neg Edge DFF w/Async Low-Active Set & Reset, Only Q out: DFFNASRQX1, DFFNASRQX2



Figure 9.41. Logic Symbol of Neg Edge DFF w/Async Low-Active Set & Reset, Only Q out

D	SETB	RSTB	CLK	Q	Notes
Х	0	0	Х	Х	Not Allowed
Х	0	1	Х	1	
Х	1	0	Х	0	
Х	1	1	Inactive	No change	
0	1	1	Fall	0	
1	1	1	Fall	1	

Table 9.81. Neg Edge DFF w/Async Low-Active Set & Reset, Only Q out Transition Table

Table 9.82. Neg Edge DFF w/Async Low-Active Set & Reset, Only Q out Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
				Pow	ver	Area
Cell Name	Cload	Output	Prop Delay (Avg) Clk to OUT (Q)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um²)
DFFNASRQX1	1 x Csl	Q	289	110	67	32.2560
DFFNASRQX2	2 x Csl	Q	256	400	110	34.0992

Neg Edge DFF w/Async Low-Active Set & Reset, Only QN out: DFFNASRNX1, DFFNASRNX2



Figure 9.42. Logic Symbol of Neg Edge DFF w/Async Low-Active Set & Reset, Only QN out

D	SETB	RSTB	CLK	QN	Notes
Х	0	0	Х	Х	Not Allowed
Х	0	1	Х	0	
Х	1	0	Х	1	
Х	1	1	Inactive	No change	
0	1	1	Fall	1	
1	1	1	Fall	0	

Table 5.00. Neg Euge DTT W// Syno Eow / Kenve Oct & Reset, Only QN out Transition Table
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Table 9.84. Neg Edge DFF w/Async Low-Active Set & Reset, Only QN out Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF						
				Pow	ver	Area	
	Cload	Output	Prop Delay (Avg) Clk to OUT (QN)	Leakage (VDD=1.32 V DC, Dynamic Temp=25 Dec.C)			
			ps	nW	nW/MHz	(um²)	
DFFNASRNX1	1 x Csl	QN	229	430	98	32.2560	
DFFNASRNX2	2 x Csl	QN	230	34.0992			

Scan Pos Edge DFF: SDFFX1, SDFFX2



Figure 9.43. Logic Symbol of Scan Pos Edge DFF

#### Table 9.85. Scan Pos Edge DFF Transition Table

D	SI	SE	CLK	Q	QN
Х	Х	Х	Inactive	No change	No change
1	Х	0	Rise	1	0
0	Х	0	Rise	0	1
Х	1	1	Rise	1	0
Х	0	1	Rise	0	1

## Table 9.86. Scan Pos Edge DFF Electrical Parameters and Areas

Cell Name	Operating Operating Capacitive					
				Pow	ver	Area
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um²)
	1 · · · Oal	Q	209	700	400	00.4400
SUFFX1	1 X CSI	QN	166	720	160	30.4128
	2 x Csl	Q	248	1100	260	22 1776
SUFFAZ		QN	179	1100	200	33.1770

Scan Pos Edge DFF w/Async Low-Active Set: SDFFASX1, SDFFASX2



Figure 9.44. Logic Symbol of Scan Pos Edge DFF w/Async Low-Active Set

Table 9.87. Scan	Pos Edge DFF	w/Async Low-A	ctive Set	Transition	Table
------------------	--------------	---------------	-----------	------------	-------

D	SI	SE	SETB	CLK	Q	QN
Х	Х	Х	0	Х	1	0
Х	Х	Х	1	Inactive	No change	No change
1	Х	0	1	Rise	1	0
0	Х	0	1	Rise	0	1
Х	1	1	1	Rise	1	0
Х	0	1	1	Rise	0	1

Table 9.88. Scan Pos Edge DFF w/Async Low-Active Set Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF						
				Pow	er Area		
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW	nW/MHz	Area (um <sup>2</sup> ) 36.8640 39.6288	
	1 v Col	Q	232	500	100	20.0040	
SUFFASAT	T X USI	QN	186	580	100	36.8640	
		Q	282	1000	140	20 6299	
SUFFASAZ	2 x CSI	QN	203	1090 140		39.0200	

Scan Pos Edge DFF w/Async Low-Active Reset: SDFFARX1, SDFFARX2



Figure 9.45. Logic Symbol of Scan Pos Edge DFF w/Async Low-Active Reset

D	SI	SE	RSTB	CLK	Q	QN
Х	Х	Х	0	Х	0	1
Х	Х	Х	1	Inactive	No change	No change
1	Х	0	1	Rise	1	0
0	Х	0	1	Rise	0	1
Х	1	1	1	Rise	1	0
Х	0	1	1	Rise	0	1

#### Table 9.89. Scan Pos Edge DFF w/Async Low-Active Reset Transition Table

#### Table 9.90. Scan Pos Edge DFF w/Async Low-Active Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF							
				Pow	er	Area (um <sup>2</sup> ) 37.7856		
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic			
			ps	nW	nW/MHz	(um²)		
	4 0.1	Q	216	000	00	07 7050		
SDFFARX1	1 X CSI	QN	161	660	90	37.7856		
		Q	263	050	400	20 6200		
SUFFARAZ		QN	180	950	120	39.0200		

Scan Pos Edge DFF w/Async Low-Active Set & Reset: SDFFASRX1, SDFFASRX2



Figure 9.46. Logic Symbol of Scan Pos Edge DFF w/Async Low-Active Set & Reset

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D	SI	SE	SETB	RSTB	CLK	Q	QN	Notes
Х	Х	Х	0	0	Х	Х	Х	Not Allowed
Х	Х	Х	0	1	Х	1	0	
Х	Х	Х	1	0	Х	0	1	
Х	Х	Х	1	1	Inactive	No change	No change	
1	Х	0	1	1	Rise	1	0	
0	Х	0	1	1	Rise	0	1	
Х	1	1	1	1	Rise	Х	1	
Х	0	1	1	1	Rise	Х	0	

Table 9.91. Scan Pos Edge DFF w/Async Low-Active Set & Reset Transition Table

# Table 9.92. Scan Pos Edge DFF w/Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF						
				Pow	er	Area	
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
			ps nW nW/MH	nW/MHz	(um²)		
	404	Q	258	700	00	40 5504	
SUFFASRAT	T X USI	QN	197	730	90	40.5504	
		Q	313	1000	100	12 2026	
SDFFASKAZ	2 X 051	QN	225	1090	120	42.3930	

Scan Pos Edge DFF w/Async Low-Active Set & Reset, Q, QN & S0 outs: SDFFASRSX1, SDFFASRSX2



Figure 9.47. Logic Symbol of Scan Pos Edge DFF w/Async Low-Active Set & Reset, Q, QN & S0 outs

Table 9.93. Scan Pos Edge DFF w/Async Low-Active Set & Reset, Q, QN & S0 outs Transition Table

D	SI	SE	SETB	RSTB	CLK	Q	QN	S0	Notes
Х	Х	Х	0	0	Х	Х	Х	Х	Not Allowed
Х	Х	Х	0	1	Х	1	0	1	
Х	Х	Х	1	0	Х	0	1	0	
Х	Х	Х	1	1	Inactive	No change	No change	No change	
1	Х	0	1	1	Rise	1	0	1	
0	Х	0	1	1	Rise	0	1	0	
Х	1	1	1	1	Rise	1	0	1	
Х	0	1	1	1	Rise	0	1	0	

#### Table 9.94. Scan Pos Edge DFF w/Async Low-Active Set & Reset, Q, QN & S0 outs Electrical Parameters and Areas

	Operating Operating Capacitive					
				Pow	ver	<b>A</b> # <b>a a</b>
Cell Name	Cload	Cload Output	Prop Delay (Avg) Clk to OUT (Q, QN, S0)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	Area
			ps	nW	nW/MHz	(um²)
		Q	275			
SDFFASRSX1	1 x Csl	QN	194	860	110	42.3936
		S0	279			
	2 x Csl	Q	360			
SDFFASRSX2		QN	222	1260	170	45.1584
		S0	361			

Scan Pos Edge DFF w/ Sync Low-Active Set & Reset: SDFFSSRX1, SDFFSSRX2



Figure 9.48. Logic Symbol of Scan Pos Edge DFF w/Async Low-Active Set & Reset

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			0		,			
D	SI	SE	SETB	RSTB	CLK	Q	QN	Notes
Х	Х	0	0	0	Rise	Х	Х	Not Allowed
Х	Х	0	0	1	Rise	1	0	
Х	Х	0	1	0	Rise	0	1	
Х	Х	Х	Х	Х	Inactive	No change	No change	
1	Х	0	1	1	Rise	1	0	
0	Х	0	1	1	Rise	0	1	
Х	1	1	1	1	Rise	1	0	
Х	0	1	1	1	Rise	0	1	

Table 9.95. Scan Pos Edge DFF w/ Sync Low-Active Set & Reset Transition Table

# Table 9.96. Scan Pos Edge DFF w/ Sync Low-Active Set & Reset Electrical Parameters and Areas

	Operating Operating Capacitive					
				Pow	er	Area
Cell Name	Cload		Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um²)
	1 v Cal	Q	208	1120	404	20,6289
SDLLSSKYI	I X USI	QN	190	1120	404	39.0200
	2 x Csl	Q	255	1480	E 4 C	13 3152
JUFF JORAZ		QN	190	1400	540	43.3152

## Scan Neg Edge DFF: SDFFNX1, SDFFNX2



Figure 9.49. Logic Symbol of Scan Neg Edge DFF

#### Table 9.97. Scan Neg Edge DFF Transition Table

D	SI	SE	CLK	Q	QN
Х	Х	Х	Inactive	No change	No change
1	Х	0	Fall	1	0
0	Х	0	Fall	0	1
Х	1	1	Fall	1	0
Х	0	1	Fall	0	1

	Operating Operating Capacitive	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
Cell Name Cload				Pow	er	Area	
	Output Prop Delay (Avg) Clk to OUT (Q, QN	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic			
			ps	nW	nW/MHz	(um²)	
SDFFNX1	1 x Csl	Q QN	239 192	730	98	34.0992	
SDFFNX2	2 x Csl	Q QN	286 227	1138	150	36.8640	

Table 9.98. Scan Neg Edge DFF Electrical Parameters and Areas

Scan Neg Edge DFF w/Async Low-Active Set: SDFFNASX1, SDFFNASX2



Figure 9.50. Logic Symbol of Scan Neg Edge DFF w/Async Low-Active Set

D	SI	SE	SETB	CLK	Q	QN
Х	Х	Х	0	Х	1	0
Х	Х	Х	1	Inactive	No change	No change
1	Х	0	1	Fall	1	0
0	Х	0	1	Fall	0	1
Х	1	1	1	Fall	1	0
Х	0	1	1	Fall	0	1

Table 9.99. S	Scan Neg Edge	DFF w/Async L	_ow-Active Set	Transition Table
	0 0	<u> </u>		

	Operating Operating Capacitive								
Cell Name Cload				Pow	er	Area			
	Cload	d Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic				
			ps	nW	nW/MHz	(um²)			
SDFFNASX1	1 x Csl	Q QN	263 223	690	110	36.8640			
SDFFNASX2	2 x Csl	Q QN	233 189	1100	140	39.6288			

Table 9.100. Scan Neg Edge DFF w/Async Low-Active Set Electrical Parameters and Areas

Scan Neg Edge DFF w/Async Low-Active Reset: SDFFNARX1, SDFFNARX2



Figure 9.51. Logic Symbol of Scan Neg Edge DFF w/Async Low-Active Reset

1		<u> </u>	-	-		
D	SI	SE	RSTB	CLK	Q	QN
Х	Х	Х	0	Х	0	1
Х	Х	Х	1	Inactive	No change	No change
1	Х	0	1	Fall	1	0
0	Х	0	1	Fall	0	1
Х	1	1	1	Fall	1	0
Х	0	1	1	Fall	0	1

Table 9.101. Scan Neg Edge DFF w/Async Low-Active Reset Transition Table

	Operating Operating Capacitive							
Cell Name Cload				Pow	er	Area		
	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic				
			ps	nW	nW/MHz	(um <sup>2</sup> )		
SDFFNARX1	1 x Csl	Q QN	273 210	706	107	37.7856		
SDFFNARX2	2 x Csl	Q QN	306 235	1185	153	39.6288		

Table 9.102. Scan Neg Edge DFF w/Async Low-Active Reset Electrical Parameters and Areas

Scan Neg Edge DFF w/Async Low-Active Set & Reset: SDFFNASRX1, SDFFNASRX2



Figure 9.52. Logic Symbol of Scan Neg Edge DFF w/Async Low-Active Set & Reset

Table 9.103. \$	Scan Neg E	dge DFF w/Asyn	c Low-Active Set	& Reset Transition Tab	ole
-----------------	------------	----------------	------------------	------------------------	-----

D	SI	SE	SETB	RSTB	CLK	Q	QN	Notes
Х	Х	Х	0	0	Х	Х	Х	Not Allowed
Х	Х	Х	0	1	Х	1	0	
Х	Х	Х	1	0	Х	0	1	
Х	Х	Х	1	1	Inactive	No change	No change	
1	Х	0	1	1	Fall	1	0	
0	Х	0	1	1	Fall	0	1	
Х	1	1	1	1	Fall	Х	1	
Х	0	1	1	1	Fall	Х	0	

Table 9.104. Scan Neg Edge DFF w/Async Low-Active Set & Reset Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		Area
				Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um²)
SDFFNASRX1	1 x Csl	Q	308	860	160	40 5504
		QN	239			40.5504
SDFFNASRX2	2 x Csl	Q	337	1130	373	12 3036
		QN	276	525	42.3930	

#### RS-NAND Latch: LNANDX1, LNANDX2



Figure 9.53. Logic Symbol of RS-NAND Latch

#### Table 9.105. RS-NAND Latch Transition Table

RIN	SIN	Q	QN	
0	0	Х	Х	
0	1	1	0	
1	0	0	1	
1	1	No change	No change	

#### Table 9.106. RS-NAND Latch Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Power		Area
				Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um²)
LNANDX1	1 x Csl	Q	122	257	11	40.4070
		QN	122			10.1376
LNANDX2	2 x Csl	Q	121	517	21	19 4220
		QN	121			10.4320


# High-Active Latch: LATCHX1, LATCHX2



Figure 9.54. Logic Symbol of High-Active Latch

Table 9.107. High-Active Latch Transition Table

D	CLK	Q	QN
Х	0	No change	No change
0	1	0	1
1	1	1	0

Table 9.108. High-Active Latch Electrical Parameters and Areas

Cell Name	Operating Operating Capacitive					
	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Pow Leakage (VDD=1.32 V DC, Temp=25 Dec C)	Dynamic	Area
			ps	nW	nW/MHz	(um <sup>2</sup> )
LATCHX1	1 x Csl	Q QN	123 166	813	158	22.1184
LATCHX1	2 x Csl	Q QN	142 206	1125	201	25.8048

High-Active Latch w/ Async Low-Active Set: LASX1, LASX2



Figure 9.55. Logic Symbol of High-Active Latch w/ Async Low-Active Set

D	SETB	CLK	Q	QN
Х	1	0	No change	No change
Х	0	Х	1	0
1	1	1	1	0
0	1	1	0	1

Table 9.109. High-Active Latch w/ Async Low-Active Set Transition Table

#### Table 9.110. High-Active Latch w/ Async Low-Active Set Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					
				Pow	er	Area
Cell Name	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um²)
LASX1	1 x Csl	Q QN	228 178	713	66	24.8832
LASX2	2 x Csl	Q QN	254 184	1139	129	29.5696

High-Active Latch w/ Async Low-Active Reset: LARX1, LARX2



Figure 9.56. Logic Symbol of High-Active Latch w/ Async Low-Active Reset

Table 9.111. High-Active Latch w/ Async Low-Active Reset Transition Table

D	RSTB	CLK	Q	QN
Х	1	0	No change	No change
Х	0	Х	0	1
1	1	1	1	0
0	1	1	0	1

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	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF						
<b>A 1 N</b>	-			Pow	er	Area	
Cell Name	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
			ps	nW	nW/MHz	(um²)	
LARX1	1 x Csl	Q QN	232 159	790	68	25.8048	
LARX2	2 x Csl	Q QN	275 178	1150	116	29.4912	

Table 9.112. High-Active Latch w/ Async Low-Active Reset Electrical Parameters and Areas

High-Active Latch w/ Async Low-Active Set & Reset: LASRX1, LASRX2



Figure 9.57. Logic Symbol of High-Active Latch w/ Async Low-Active Set & Reset

Table 9.113. High-Active Latch w/	Async Low-Active Set 8	Reset Transition Table
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D	SETB	RSTB	CLK	Q	QN	Notes
Х	1	1	Х	Х	Х	Not Allowed
Х	0	1	Х	1	0	
Х	1	0	Х	0	1	
Х	1	1	0	No change	No change	
1	1	1	1	1	0	
0	1	1	1	0	1	

Table 9.114. High-Active Latch w/ Async Low-Active Set & Reset Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					
O all Nama				Pow	ver	Area
Cell Name	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um²)
LASRX1	1 x Csl	Q	254	554	73	26.7264
LASRX2	2 x Csl		201	980		
		QN	197		125	31.3344

High-Active Latch w/ Async Low-Active Set & Reset only Q out: LASRQX1, LASRQX2



Figure 9.58. Logic Symbol of High-Active Latch w/ Async Low-Active Set & Reset only Q out

Table 9.115. High-Active	e Latch w/ Async	Low-Active Set &	Reset only	Q out T	ransition Table
0	,		,		

D	SETB	RSTB	CLK	Q	Notes
Х	0	0	Х	Х	Not Allowed
Х	0	1	Х	1	
Х	1	0	Х	0	
Х	1	1	0	No change	
1	1	1	1	1	
0	1	1	1	0	

Table 9.116. High-Active Latch w/ Async Low-Active Set & Reset only Q out Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					
0.11.11			Pov	wer	Area	
Cell Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	nW/MHz	(um²)	
LASRQX1	1 x Csl	227	428	62	25.8048	
LASRQX2	2 x Csl	246	517	97	26.7264	

High-Active Latch w/ Async Low-Active Set & Reset only QN out: LASRNX1, LASRNX2



Figure 9.59. Logic Symbol of High-Active Latch w/ Async Low-Active Set & Reset only QN out

D	SETB	RSTB	CLK	QN	Notes
Х	0	0	Х	Х	Not Allowed
Х	0	1	Х	0	
Х	1	0	Х	1	
Х	1	1	0	No change	
1	1	1	1	0	
0	1	1	1	1	

Table 9.117. High-Active Latch w/ Async Low-Active Set & Reset only QN out Transition Table



Table 9.118. High-Active Latch w/ Async Low-Active Set & Reset only QN out Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
Cell Name			Pov	wer	Area
	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um <sup>2</sup> )
LASRNX1	1 x Csl	176	345	44	25.8048
LASRNX2	2 x Csl	198	418	51	27.6480

Clock Gating cell w/ Latched Pos Edge Control Post: CGLPPSX2, CGLPPSX4, CGLPPSX8, CGLPPSX16



Figure 9.60. Logic Symbol of Clock Gating cell w/ Latched Pos Edge Control Post

Table 9.119. Clock Gating cell w/ Latched Pos Edge Control Post Truth Table

SE	EN	CLK	GCLK
1	Х	0	0
1	Х	1	1
0	0	0	0
0	0	1	OBS
0	1	0	0
0	1	1	1

Table 9.120. Clock Gating cell w/ Latched Pos Edge Control Post Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz,				
	Capacitive Standard Load: Csl=13 fF Power				
Cell Name	Cload Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	nW/MHz	(um²)
CGLPPSX2	2 x Csl	181	1073	66	25.8048
CGLPPSX8	8 x Csl	200	2889	185	33.1776
CGLPPSX16	16 x Csl	118	5346	397	47.0016

Clock Gating cell w/ Latched Neg Edge Control Post: CGLNPSX2, CGLNPSX4, CGLNPSX8, CGLNPSX16



Figure 9.61. Logic Symbol of Clock Gating cell w/ Latched Neg Edge Control Post

Table 9.121. Clock Gating cell w/ Latched Neg Edge Control Post Truth Table

SE	EN	CLK	GCLK
1	Х	0	0
1	Х	1	1
0	0	0	!OBS
0	0	1	1
0	1	0	0
0	1	1	1

Table 9.122. Clock Gating cell w/ Latched Neg Edge Control Post Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
Cell Name			Pov	wer	Area
	Cload Prop Dela	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
CGLNPSX2	2 x Csl	185	915	79	23.0400
CGLNPSX8	8 x Csl	267	2697	304	31.3344
CGLNPSX16	16 x Csl	246	5049	488	44.2368

Clock Gating cell w/ Latched Pos Edge Control Pre: CGLPPRX2, CGLPPRX8



Figure 9.62. Logic Symbol of Clock Gating cell w/ Latched Pos Edge Control Pre

Table 9.123. Clock Gating cell w/ Latched Pos Edge Control Pre Truth Table

SE	EN	CLK	ENL
1	Х	0	1
Х	1	0	1
0	0	0	1
Х	Х	1	No change

ENL	CLK	GCLK
0	0	0
0	1	0
1	0	0
1	1	1

Table 9.124. Clock Gating cell w/ Latched Pos Edge Control Pre Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
			Pov	wer	Area
Cell Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um <sup>2</sup> )
CGLPPRX2	2 x Csl	185	919	66	21.1968
CGLPPRX8	8 x Csl	205	2668	185	29.4912

Clock Gating cell w/ Latched Neg Edge Control Pre: CGLNPRX2, CGLNPRX8



Figure 9.63. Logic Symbol of Clock Gating cell w/ Latched Neg Edge Control Pre

Table 9.125. Clock Gating cell w/ Latched Neg Edge Control Pre Truth Table

SE	EN	CLK	ENL
1	Х	1	1
Х	1	1	1
0	0	1	1
Х	Х	0	No change

ENL	CLK	GCLK
0	0	1
0	1	1
1	0	0
1	1	1

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Table 9.126. Clock Gating cell w/ Latched Neg Edge Control Pre Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF				
Cell Name				ver	Area
	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
CGLNPRX2	2 x Csl	178	714	66	23.0400
CGLNPRX8	8 x Csl	220	1350	198	32.2560

Non-Inverting Delay Line: DELLN1X2, DELLN2X2, DELLN3X2



Figure 9.64. Logic Symbol of Non-Inverting Delay Line

Table 9.127. Non-Inverting Delay Line Truth Table



Table 9.128. Non-Inverting Delay Line Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
0 11 11			Pov	wer	Area
Cell Name	Cload Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
	ps	nW	nW/MHz	(um <sup>2</sup> )	
DELLN1X2	2 x Csl	254	385	125	14.7456
DELLN2X2	2 x Csl	509	445	135	15.6672
DELLN3X2	2 x Csl	754	668	156	22.1184

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Pass Gate: PGX1, PGX2, PGX4



Figure 9.65. Logic Symbol of Pass Gate

Table 9.129. Pass Gate Truth	Table
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INQ1	INN	INP	INQ2	Notes
Х	0	1	Z	
Х	Х	0	Х	Not Allowed
Х	1	Х	Х	Not Allowed
X	1	0	INQ1	

### Table 9.130. Pass Gate Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
			Pov	wer	Area
Cell Name	Cload Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	nW/MHz	(um <sup>2</sup> )
PGX1	1 x Csl	35	160	11	7.3728
PGX2	2 x Csl	37	325	20	8.2944
PGX4	4 x Csl	39	618	38	10.1376

Bi-directional Switch w/ Active Low Enable: BSLEX1, BSLEX2, BSLEX4



Figure 9.66. Logic Symbol of Bi-directional Switch w/ Active Low Enable

Table 9.131. Bi-directional Switch w/ Active Low Enable Truth Table

INOUT1	ENB	INOUT2
Х	0	INOUT1
Х	1	Z

Table 9.132. Bi-directional Switch w/ Active Low Enable Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
0			Pov	wer	Area
Cell Name	Cload Prop Del	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um²)
BSLEX1	1 x Csl	36	315	10	7.3728
BSLEX2	2 x Csl	38	610	19	10.1376
BSLEX4	4 x Csl	40	1150	39	12.9024

Hold 0 Isolation Cell (Logic AND): ISOLANDX1, ISOLANDX2, ISOLANDX4, ISOLANDX8



Figure 9.67. Logic Symbol of Hold 1 Isolation Cell (Logic AND)

Table 9.133. Hold 0 Isolation Cell (Logic AND) Truth Table

D	ISO	Q
0	Х	0
Х	0	0
1	1	1

Table 9.134. Hold 0 Isolation Cell (Logic AND) Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
0				wer	Area
Cell Name	Cload Prop Delay (Avg)	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		nW	nW/MHz	(um²)	
ISOLANDX1	1 x Csl	111	366	20	7.3728
ISOLANDX2	2 x Csl	129	644	26	9.2016
ISOLANDX8	8 x Csl	165	2354	50	18.4320

Hold 1 Isolation Cell (Logic OR): ISOLORX1, ISOLORX2, ISOLORX4, ISOLORX8



Figure 9.68. Logic Symbol of Hold 0 Isolation Cell (Logic OR)

Table 9.135. Hold 1 Isolation Cell (Logic OR) Truth Table

ISO	Q
0	0
1	1
Х	1
	0 1 X

Table 9.136. Hold 1 Isolation Cell (Logic OR) Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				
			Pov	wer	Area
Cell Name	Cload Prop Delay (Avg)	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		nW	nW/MHz	(um²)	
ISOLORX1	1 x Csl	84	330	45	7.3728
ISOLORX2	2 x Csl	82	611	76	9.2160
ISOLORX8	8 x Csl	162	2305	326	17.5104

Low to High Level Shifter: LSUPX1, LSUPX2, LSUPX4, LSUPX8



Figure 9.69. Logic Symbol of Low to High Level Shifter

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Table 9.137. Low to High Level Shifter Truth Table

D	Q	
0	0	
Х	1	
1	1	

Table 9.138. Low to High Level Shifter Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF				
			Pov	wer	Area
Cell Name	Cload Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	nW/MHz	(um²)
LSUPX1	1 x Csl	262	450	112	22.1184
LSUPX2	2 x Csl	301	733	158	22.1184
LSUPX8	8 x Csl	500	2376	465	36.8640

High to Low Level Shifter: LSDNX1, LSDNX2, LSDNX4, LSDNX8





Table 9.139. High to Low Level Shifter

D	Q
0	0
Х	1
1	1

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	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					
			Pov	wer	Area	
Cell Name	Cload	Cload Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	nW/MHz	(um <sup>2</sup> )	
LSDNX1	1 x Csl	69	306	31	5.5296	
LSDNX2	2 x Csl	78	585	58	7.3728	
LSDNX8	8 x Csl 143 2639 231				23.0400	

Table 9.140. High to Low Level Shifter Electrical Parameters and Areas

Low to High Level Shifter/ Active Low Enable: LSUPENX1, LSUPENX2, LSUPENX4, LSUPENX8





Table 9.141. Low to High Level Shifter /Active Low Enable Truth Table

D	ENB	Q
Х	0	1
0	1	0
1	1	1

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Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF						
			Pov	wer	Area	
Cell Name	Cload	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um <sup>2</sup> )	
		200	707	450	27 2000	
LSUPENAI	I X USI	280	/8/	450	27.3000	
LSUPENX2	2 x Csl	285	923	975	31.1328	
LSUPENX8	8 x Csl	608	3125	1680	42.9410	

High to Low Level Shifter/ Active Low Enable: LSDNENX1, LSDNENX2, LSDNENX4, LSDNENX8



Figure 9.72. Logic Symbol of High to Low Level Shifter/Active Low Enable

Table 9.143. High to Low Level Shifter / Active Low Enable Truth Table

D	ENB	Q
Х	0	1
0	1	0
1	1	1

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Table 5.144. High to Low Level Officer/ Notive Low Enable Elevendar and Areas						
Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF						
			Pov	ver	Area	
Cell Name	Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	nW/MHz	(um²)	
LSDNENX1	1 x Csl	69	28	200	10.9250	
LSDNENX2	2 x Csl	82	30	220	18.4000	
LSDNENX8	8 x Csl	8 x Csl 218 457 800				

Table 9.144. High to Low Level Shifter/ Active Low Enable Electrical Parameters and Areas

Pos Edge Retention DFF: RDFFX1, RDFFX2



Figure 9.73. Logic Symbol of Pos Edge Retention DFF

Table 9.145. F	Pos Edge	Retention DFI	- Transition Table
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RETN	D	CLK	Q[n+1]	QN[n+1]	Mode
1	0	Rise	0	1	Normal mode write 0
1	1	Rise	1	0	Normal mode write 1
1	Х	Fall	Q[n]	QN[n]	Normal mode latch state
0	Х	Х	Х	Х	Retention mode
Rise	Х	0	Q[n]	QN[n]	Restore mode
Х	Х	Х	Х	Х	Power down no retention

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
				Pow	ver	Area
Cell Name	Cload	d Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um²)
RDFFX1	1 x Csl	Q QN	173 251	1056	134	58.0608
RDFFX2	2 x Csl	Q QN	195 293	1188	246	58.9824

Table 9.146. Pos Edge Retention DFF Electrical Parameters and Areas

Scan Pos Edge Retention DFF: RSDFFX1, RSDFFX2



Figure 9.74. Logic Symbol of Scan Pos Edge Retention DFF

Table 9.147. Scan Pos Edge Retention DFF Transition Tabl	le
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RETN	D	CLK	SI	SE	Q[n+1]	QN[n+1]	Mode
1	Х	Х	Х	Х	0	1	Normal mode reset
1	0	Rise	Х	0	0	1	Normal mode write 0
1	Х	Rise	0	1	0	1	Scan mode write 0
1	Х	Rise	1	1	1	0	Scan mode write 1
1	1	Rise	Х	0	1	0	Normal mode write 1
1	Х	Fall	Х	Х	Q[n]	QN[n]	Normal mode latch state
0	Х	Х	Х	Х	Х	Х	Retention mode
Rise	Х	0	0	0	Q[n]	QN[n]	Restore mode
Х	Х	Х	Х	Х	Х	Х	Power down no retention

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
0 11 11	-			Pow	er	Area
Cell Name Cload	Cload	d Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um²)
RSDFFX1	1 x Csl	Q QN	177 255	1258	110	66.3552
RSDFFX2	2 x Csl	Q QN	194 290	1374	185	68.1984

Table 9.148. Scan Pos Edge Retention DFF Electrical Parameters and Areas

Neg Edge Retention DFF: RDFFNX1, RDFFNX2



Figure 9.75. Logic Symbol of Pos Edge Retention DFF

Table 9.149. Neg Edge Retention [	DFF Transition Table
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RETN	D	CLK	Q[n+1]	QN[n+1]	Mode
1	0	Fall	0	1	Normal mode write 0
1	1	Fall	1	0	Normal mode write 1
1	Х	Rise	Q[n]	QN[n]	Normal mode latch state
0	Х	Х	Х	Х	Retention mode
Rise	Х	0	Q[n]	QN[n]	Restore mode
Х	Х	Х	Х	Х	Power down no retention

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
<b>A</b>				Pow	er	Area
Cell Name Cload	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um²)
RDFFNX1	1 x Csl	Q QN	202 297	1168	110	57.1392
RDFFNX2	2 x Csl	Q QN	214 310	1536	195	58.9824

Table 9.150. Neg Edge Retention DFF Electrical Parameters and Areas

Scan Neg Edge Retention DFF: RSDFFNX1, RSDFFNX2



Figure 9.76. Logic Symbol of Scan Neg Edge Retention DFF

Table 9.151. Scan Neg	Edge F	Retention DF	FF Transition	Table
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RETN	D	CLK	SI	SE	Q[n+1]	QN[n+1]	Mode
1	Х	Х	Х	Х	0	1	Normal mode reset
1	0	Fall	Х	0	0	1	Normal mode write 0
1	Х	Fall	0	1	0	1	Scan mode write 0
1	Х	Fall	1	1	1	0	Scan mode write 1
1	1	Fall	Х	0	1	0	Normal mode write 1
1	Х	Rise	Х	Х	Q[n]	QN[n]	Normal mode latch state
0	Х	Х	Х	Х	Х	Х	Retention mode
Rise	Х	0	0	0	Q[n]	QN[n]	Restore mode
Х	Х	Х	Х	Х	Х	Х	Power down no retention

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
<b>A H N H</b>				Pow	ver	Area
Cell Name Cloa	Cload	Output	Prop Delay (Avg) Clk to OUT (Q, QN)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	fW/MHz	(um²)
RSDFFNX1	1 x Csl	Q QN	206 301	1374	127	66.3552
RSDFFNX2	2 x Csl	Q QN	212 310	1742	241	68.1984

Table 9.152. Scan Neg Edge Retention DFF Electrical Parameters and Areas

Header Cell: HEADX2, HEADX4, HEADX8, HEADX16, HEADX32



Figure 9.77. Logic Symbol of Header Cell

# Table 9.153. Header Cell Truth Table

SLEEP	VDDG	VDD	SLEEPQ
0	1	1	0
1	1	hi-z	1

# Table 9.154. Header Cell Electrical Parameters and Areas

	Operating Condition Operating Frequent Capacitive Standard	emp=25 Deg.C,			
0 11 11			Pov	wer	Area
Cell Name Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	nW/MHz	(um²)
HEADX2	2 x Csl	-	0.74	0.312	27.6480
HEADX8	8 x Csl	-	3	1.6	44.2368
HEADX32	32 x Csl	-	13.2	7.2	112.4352



Figure 9.78. Logic Symbol of Always on Non-inverting Buffer

Table 9.14155. Always on Non-inverting Buffer Truth Table

IN	VDDG	VSS	Q
0	1	0	0
1	1	0	1

Table 9.156. Always on Non-inverting Buffer Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					
			Pov	wer	Area	
Cell Name Cload	Prop Delay (Avg)	Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic			
		ps	nW	nW/MHz	(um²)	
AOINVX1	1 x Csl	66	306	28	22.1184	
AOINVX2	2 x Csl	76	585	60	22.1184	
AOINVX4	4 x Csl	98	1071	112	27.6480	

Always on Non-inverting Buffer: AOBUFX1, AOBUFX2, AOBUFX4



Figure 9.79. Logic Symbol of Always on Non-inverting Buffer

SAUDERAR



#### Table 9.157142. Always on Non-inverting Buffer Truth Table

IN	VDDG	VSS	Q
0	1	0	0
1	1	0	1

# Table 9.158. Always on Non-inverting Buffer Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF					
Cell Name		Prop Delay (Avg)	Power		Area	
	Cload		Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic		
		ps	nW	nW/MHz	(um²)	
AOBUFX1	1 x Csl	66	306	28	22.1184	
AOBUFX2	2 x Csl	76	585	60	22.1184	
AOBUFX4	4 x Csl	98	1071	112	27.6480	

Always on Pos Edge DFF, w/ Async Low-Active Reset: AODFFARX1, AODFFARX2



Figure 9.80. Logic Symbol of Always on Pos Edge DFF, w/ Async Low-Active Reset

Table 9.159. Always on Pos Edge DFF, w/ Async Low-Active Reset Transition Table

RSTB	CLK	D	Q	QN
0	Х	Х	0	1
1	Rise	0	0	1
1	Rise	1	1	0
1	0	Х	Q	QN
1	1	Х	Q	QN

Table 9.160. Always on Pos Edge DFF, w/ Async Low-Active Reset Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
			Prop Delay (Avg) Clk to OUT (Q, QN)	Power		Area
	Cload	Output		Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um²)
AODFFARX1	1 x Csl	Q	255	070	96	46.0800
		QN	186	970		40.0000
AODFFARX2	2 x Csl	Q	290	1120	122	49 7664
		QN	197			43.7004

Always on Neg Edge DFF, w/ Async Low-Active Reset: AODFFNARX1, AODFFNARX2



Figure 9.81. Logic Symbol of Always on Neg Edge DFF, w/ Async Low-Active Reset

Table 9.161. Always on Neg Edge DFF, w/ Async Low-Active Reset Transition Table

RSTB	CLK	D	Q	QN
0	Х	Х	0	1
1	Fall	0	0	1
1	Fall	1	1	0
1	0	Х	Q	QN
1	1	Х	Q	QN

Table 9.162. Always on Neg Edge DFF, w/ Async Low-Active Reset Electrical Parameters and Areas

	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: CsI=13 fF					
			Prop Delay (Avg) Clk to OUT (Q, QN)	Power		Area
Cell Name	Cload	Output		Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
			ps	nW	nW/MHz	(um²)
AODFFNARX1	1 x Csl	Q QN	287 213	620	100	47.9232
AODFFNARX2	2 x Csl	Q QN	322 227	970	132	47.9232

Bus Keeper: BUSKP



Figure 9.82. Logic Symbol of Bus Keeper

Table 9.163. Bus Keeper Truth Table



P-MOSFET: PMT1, PMT2, PMT3



Figure 9.83. Logic Symbol of P-MOSFET

Table 9.164. P-MOSFET Truth Table



# N-MOSFET: NMT1, NMT2, NMT3



Figure 9.84. Logic Symbol of N-MOSFET

Table 9.165. N-MOSFET Truth Table



Tie High: TIEH



Figure 9.85. Logic Symbol of Tie High

Table 9.166. Tie High Truth Table



Tie Low: TIEL



Figure 9.86. Logic Symbol of Tie Low

Table 9.167. Tie Low Truth Table



SYNUPSYS

# Antenna Diode: ANTENNA



Figure 9.87. Logic Symbol of Antenna Diode

Table 9.168. Antenna Diode Truth Table



Decoupling Capacitance: DCAP



Figure 9.88. Logic Symbol of DCAP Decoupling Capacitance

Capacitive Load: CLOAD1



Figure 9.89. Logic Symbol of Capasitive Load

# 10. Revision history

Table 1	0.1. Re	vision	history
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Revision	Date	Change
A.1	06/01/2007	Initial release
A1.1	06/11/2007	<ul> <li>Capacitive Load cell has been added</li> </ul>
		<ul> <li>Filler cells have been updated</li> </ul>
		<ul> <li>Physical structure of double height (high-low-high) digital</li> </ul>
		standard cells (for Level-Shifter cells: Low-High) has been
		<ul> <li>Symbols have been updated</li> </ul>
		<ul> <li>Electrical parameters and areas of cells have been updated</li> </ul>
A1.2	06/06/2008	<ul> <li>Inverting Buffer cells have been updated</li> </ul>
		<ul> <li>Scan Latches cells have been removed</li> </ul>
		<ul> <li>Async cells in Retenetion Flip-Flops and scan Flip-Flops cells</li> </ul>
		have been removed
		<ul> <li>Digital Standard Cell Library deliverables have been updated</li> </ul>
A.1.3	11/12/2008	<ul> <li>The following cells have been added:Low to High Level Shifters/</li> </ul>
		Active Low Enable, High to Low Level Shifters/ Active Low
		Enable
		<ul> <li>2 new corners have been added for characterization</li> </ul>
		-
A.1.4	27/12/2008	<ul> <li>The table of characterization cormers has been updated</li> </ul>
		<ul> <li>The table of characterization cormers for Low to High Level</li> </ul>
		Shifters has been removed