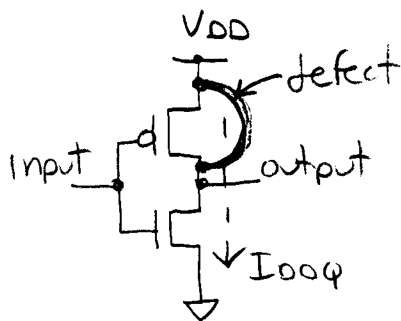
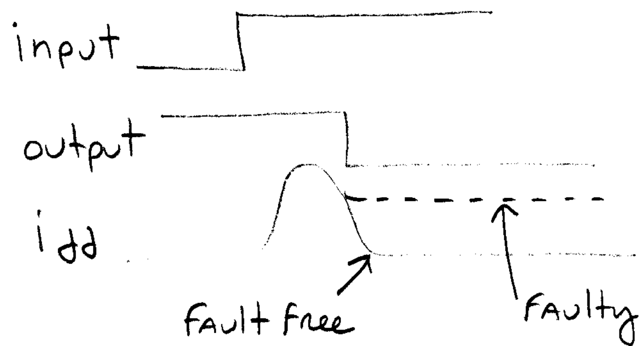
I_{DDQ} Testing of CMOS chips

Under steady state conditions, CMOS gates do not consume power (ideally).

Some current does flow in steady state conditions that is called leakage current, denoted as I_{DDQ}.

By measuring elevated leakage current, a defective chip may be detected.





A defect that causes a high I_{DDQ} when excited is called a <u>pattern dependent defect</u>. A defect that causes a high I_{DDQ} independent of input pattern is called a <u>passive defect</u>.

Advantages of IDDQ Testing

Since IDDQ test uses power lines for fault propagation, 100% observability is possible.

Only a relatively few vectors are required to excite all possible defect sites.

Defects detected by IDDQ testing also lead to reduced reliability.

- metal slivers, electromigration damage
- hot carrier injection damage

IDDQ tests are very useful to screen devices used in high reliability applications.

IDDQ testing of DSM CMOS

Current Signature

Run many vector sets into chip and note any large jumps in IDDQ over background current.

Delta IDDQ

Measure difference between minimum IDDQ vector and maximum IDDQ vector; reject if difference is large.

Wafer-level spatial correlation

Neighboring chips on wafer have fault-free IDDQ characteristics. Reject those neighbors outside the norm.

Challenges to IDDQ Testing

Static threshold method traditionally used
- if IDDQ exceeds a threshold, the chip is rejected.

As feature sizes decrease, static threshold methods no longer work.

$$I_{DDQ} \approx \left(\frac{W X_c}{L_{eff}}\right) e^{-\frac{K V_T}{T}}$$

K = Boltzman const.
$W \cdot X_c$ = channel cross sectional current flow area
W = channel width
L_{eff} = effective channel length
V_T = device threshold voltage
T = device temperature

To operate with much thinner gate oxides, V_T must be reduced. This causes an exponential increase in leakage current.

For current high performance DSM technology, leakage currents are on the order of a few hundred mA.

Future technologies will produce leakage currents in the 10's of Amperes. (8 to 20 A by 2014)

IDDQ testing is <u>slow</u>. 10 - 100 m$ per measurement