Integrated Circuit Packaging

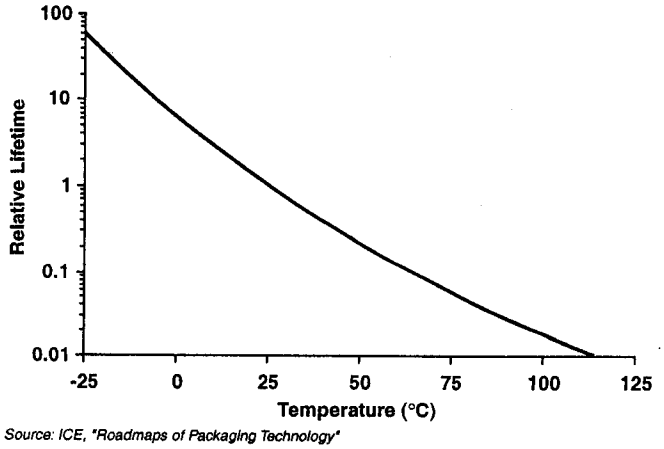
Packaging Provides:
- -physical support and environmental protection
- -connection from I/O pads to board
- -heat dissipation
- -delivery of power to chip

Package strongly effects.....

Cost
- -some analyists forcast that packaging costs will soon dominate total cost for both low and high end ICss
- -a $300 IC with a $100 package not too unusual

Performance
- -approxiately 60% of total system delay comes from the time it takes for a signal to travel from one chip to another
- -By 2010 this will increase to 80% unless a breakthrough is reached. (Hypertransport? 200-80Mhz, 1.2LVDS, differential)
- -every 10 degC increase in temperature, switching delay for CMOS gate increases by 2%

Reliability
- -every 10 degC increase in junction temperature cuts the lifetime of a device roughly in half.
- -without a correctly designed i/o connection offchip, a system may suffer failures from transmission line effects.

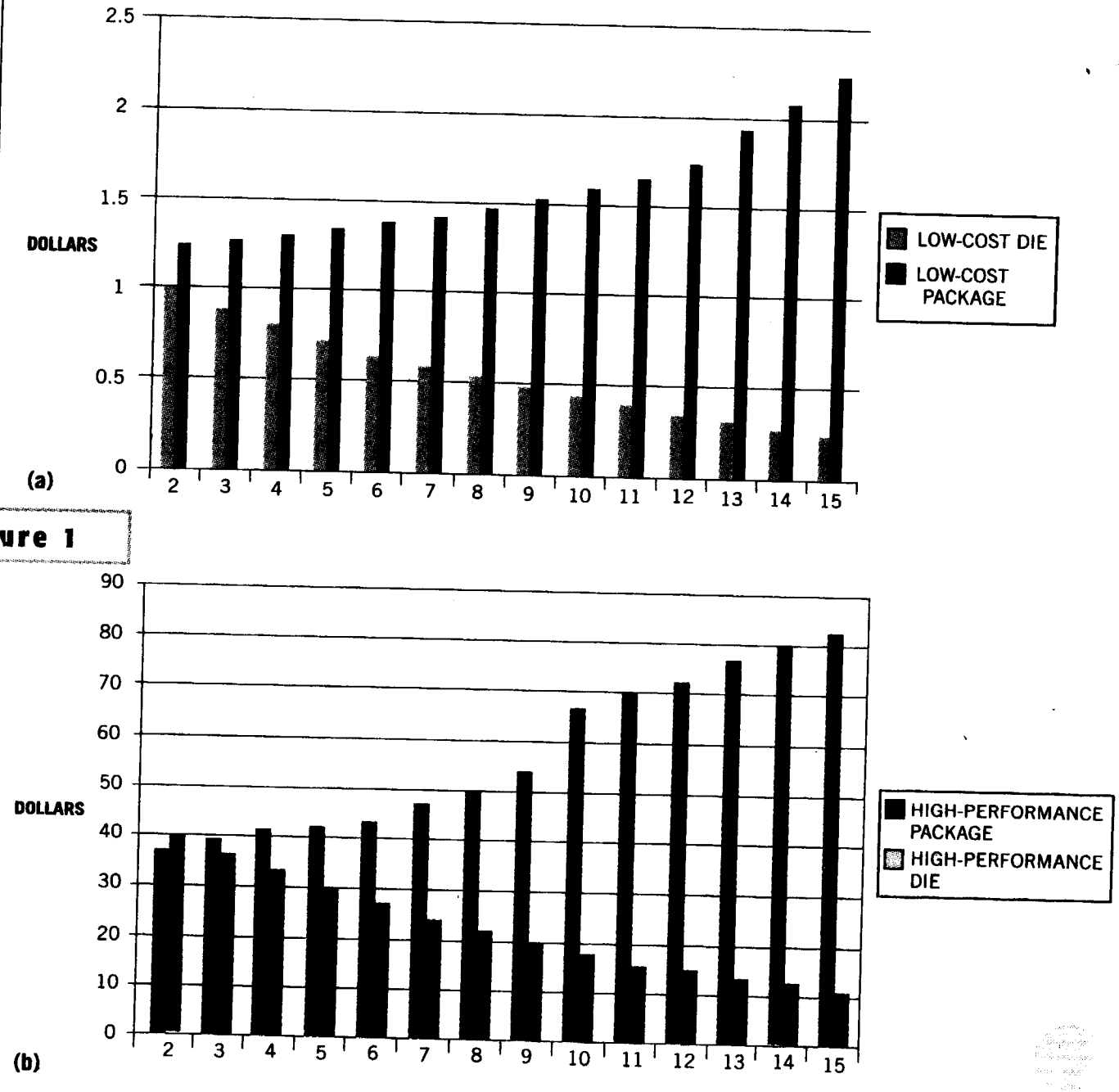


Relative MTBF with Activation Energy of 0.5eV

device level may not be one of them.

often unnecessary to route signal traces between the QFP leads. Instead, you can bring signals to the top of the board using vias within the bare cavity that the pinout boundary defines and then fan

space-sensitive applications. Low-impedance BGA sockets, often employing elastomeric connections, come from companies such as Ironwood Electronics. As an alternative to BGAs, companies such as Advanced Interconnect Technologies are advocating next-generation boundary packages, such as the no-lead



Industry projections suggest that packaging costs soon will outweigh silicon-die costs for both low- (a) and high-complexity (b) devices (courtesy *IEEE International Technology Roadmap for Semiconductors*).

A perfect package:

Speed
- -short chip to chip delay
- -high bandwidth

Pin count and "wireability"
- -large i/o count
- -allows dense wiring on board

Size
- -small

Noise
- -high quality transmission lines
- -low coupling between wires
- -power distribution has low inductance to minimize SSO noise
- -power distribution has low resistance

Thermal and Mechanical
- -high heat removal rate
- -good match between thermal expansion coefficients of the die and chip carrier, and between chip carrier and board.

Test, reliability and cos
- -easy to test and fix
- -easy to manufacture
- -very reliable
- -very low cost

A quick tour of packaging zoo

DIP (dual inline package)
- -one of the orignal packages widely available
- -pin count from 8 to 64, all on periphery
- -through hole mounting limits board packing density
- -position of power and ground usually poor
- -other i/o can have significant L and C (20nH, 20pf)

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PGA (pin grid array)
- -entire bottom surface covered with pins
- -parasitic L and C (10nH, 10pf)
- -pin count 80-500
- -cavity up or cavity down versions
- -cavity down, better heat dissipation, fewer pins
- -ceramic substrate usually used which gives bigger C
- -thermal expansion of package does not match PCB well
- -epoxy fiberglass PCB also used as substrate
  - -cheaper, and had thermal match to PCB
  - -worse match between die and PCB
  - -lower parasitic L an C (10nH, 2pf)
  - -cannot dissipate as much power

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BGA (ball grid array)
- -like PGA but uses solder balls and surface mounting
- -easier access from board to pins
- -parasitic L and C (5nH, 1pf)

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Thermal considerations in Packaging

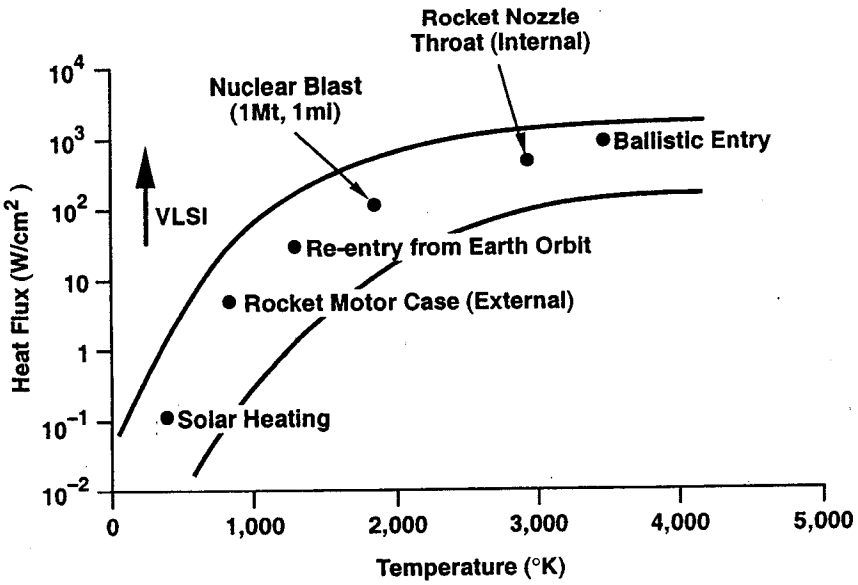
Operation of circuits causes heat dissipation
- -static (quiescent) power dissipation
  - ideally zero in CMOS
  - leakage current breaking this model in DSM
- -dynamic power dissipation (AC)
  - increases with switching frequency

Major contributors are i/o drivers, clock drivers, core
- -I/O: 50Mhz switching rate, 3.3V supply, 100 output buffers driving 70pf load will dissipate 1W.
- clock tree contributes about 40% of total dissipation

Heat must be removed efficiently as virtually all failure mechanisms are enhanced by increased temperatures.

Typical tempeature ranges:
- -commercial: range 0-70 degC, military: -55 to +125 degC
- -this is a junction temperature
- -junction temperature should be kept under 115 degC
  - 85 degC: IBM
  - 90 degC: Intel

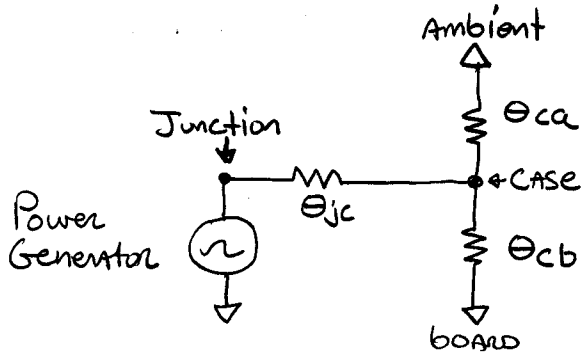
High end device: 17mm x 17mm => 3.0 cm^2
@ 30W dissipation, power flux = 10W/cm^2



Source: ICE, "Roadmaps of Packaging Technology"

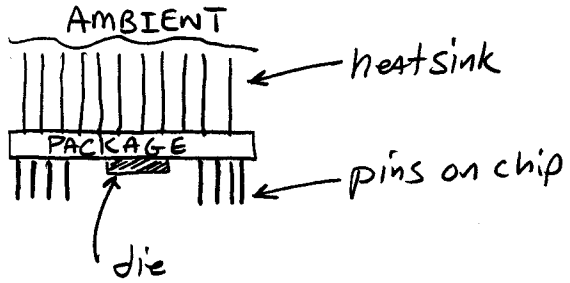
Heat Fluxes of Various Activities

IC Thermal Paths



Two paths for cooling
- through case
- through pins

θ_{JC} = JUNCTION TO CASE THERMAL RESISTANCE
θ_{CA} = CASE TO AMBIENT THERMAL RESISTANCE
θ_{CB} = CASE TO BOARD THERMAL RESISTANCE



Need to keep junction temperature < ≈100 °C

How hot is the die?

$$T_J = T_A + (\theta_{JA} * P_T)$$

T_J = junction temp.

T_A = Ambient temp.

θ_{JA} = thermal resistance junction to ambient

P_T = Power Dissipated

Thermal resistance is exactly Analogous to electrical resistance.

Units of thermal resistance are °C/W

For example: θ_{JA} is 8°C/W
Chip drawing 3A @ 3.3V ($P = VI = 10W$)
Ambient temperature is 25°C

$T_J = 25 + (8°C/W * 10W)$

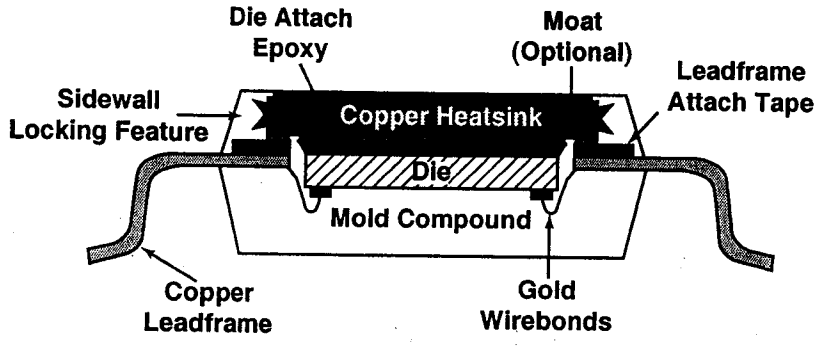
$= 105°C$ Pretty hot!

IC Thermal Paths

To reduce θ_{JA}, we can reduce θ_{JC}, θ_{CA}, θ_{CB}

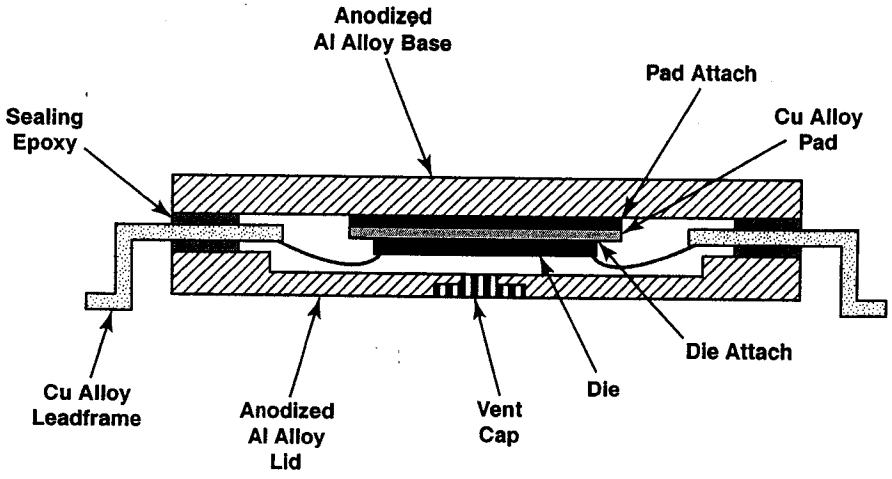
θ_{JC}: need to couple die to case well

- overmolded plastic parts: $\theta_{JC} \approx 20°/W$
  → low power applications only
- cavity down packages
  - back of die faces up to A heat spreader
- plastic fillers to enhance thermal conductivity
  - Aluminium, silicon nitride
  - 30% - 40% improvement
- metal substrate package (MQUAD) $\times 2°/W$
- bond die directly to copper spreader or heat sink
  $< 1°/W$



Source: Amkor Anam/ICE, "Roadmaps of Packaging Technology" 22083

Thermally Enhanced PQFP with Embedded Heat Spreader

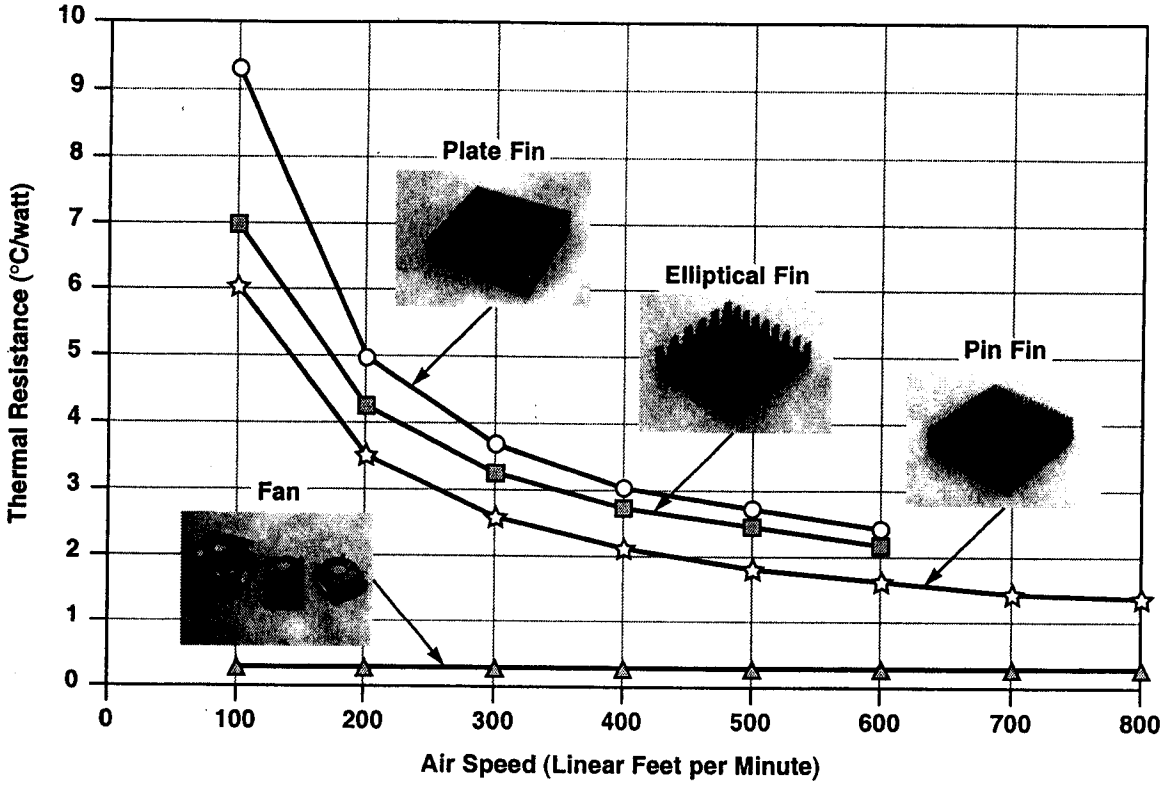


Source: IEEE/Olin/ICE, "Roadmaps of Packaging Technology"

Cavity Down MQUAD® Package

θ_{CA} : need to get heat in case to ambient, depends on:

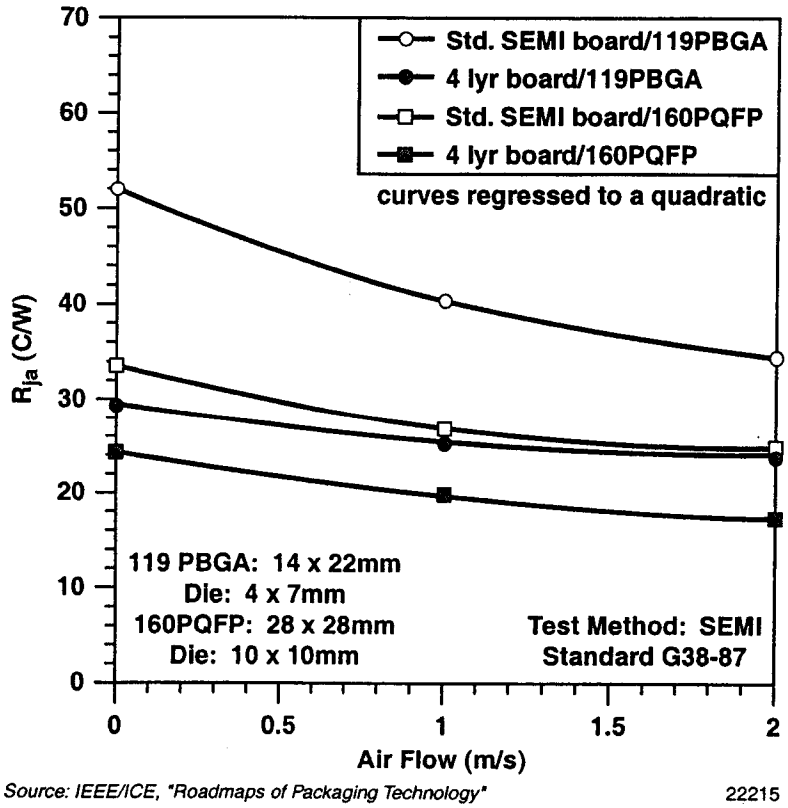
- contact area
- heat sink material
- cooling fluid
  - air
  - water
  - flourinert
- flow rate
  - beyond 600 lfm, little improvement



Source: Intricast/ICE, "Roadmaps of Packaging Technology"

Θ_{CB}: can be more effective that you think

- plastic overmolded parts often get 40% of their heat conduction through the pins.
- 119 pin BGA can sink > 85% of total power dissipation into PCB
- thicker board with multiple ground + power planes can dissipate even more. (thermal vias)
- with proper selection of package and PCB design, Θ_{JA} can be reduced by up to 50%.



R_{ja} Versus Air Flow Characteristics, 119 PBGA Versus 160 PQFP, Standard and Enhanced Boards

AC Power Dissipation in CMOS

The energy, U switched in a capactior C, when it is charged from J to V volts is:

$$U = 1/2CV^2$$

The nature of RC circuits will cause stored engery to be converted to heat every charge/discharge cycle. If the voltage makes two transistions per clock cycle, the average power dissipated is:

$$P = CV^2F_{clock}$$

A major drive for lower voltages is now clear. The squared voltage term makes power dissipation strongly dependent on voltage.
For example in 1um CMOS,

5V core gates dissipate about 6uW/Mhz/gate
3V core gates dissipate about 2.2uW/Mhz/gate

The generic power dissipation equation for CMOS is:

$P = 1/2f_cV_{dd}^2C$; where

f_c = clock frequency
V_{dd} is power supply voltage
C is the capacitive load

This equation assumes:
- -switching once every cycle (core is about 40%)
- -neglects short circuit current
- -DC current in special circuits
- -leakage currents (40% of dissipation in 90nm @ 90 degC)

IBM G5 front side bus: 1Ghz, 1.5V GTL, 50pf load

64 data pins	3.6W
42 address pins	2.4W
	6.0W (56mW/pin)