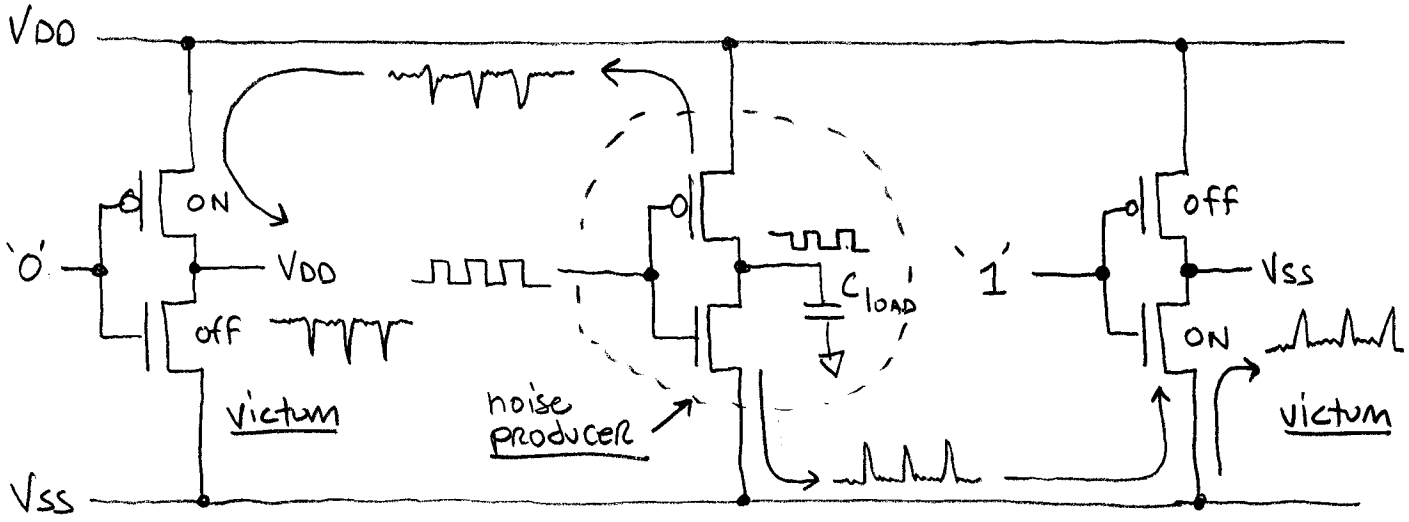
Simultaneous Switching Outputs

Description of Problem

- High density, high speed VLSI devices have many drivers that may switch simultaneously

- The combined current from all the output drivers can produce significant power and ground noise called SSO noise. This noise can cause several different flavors of malfunction.

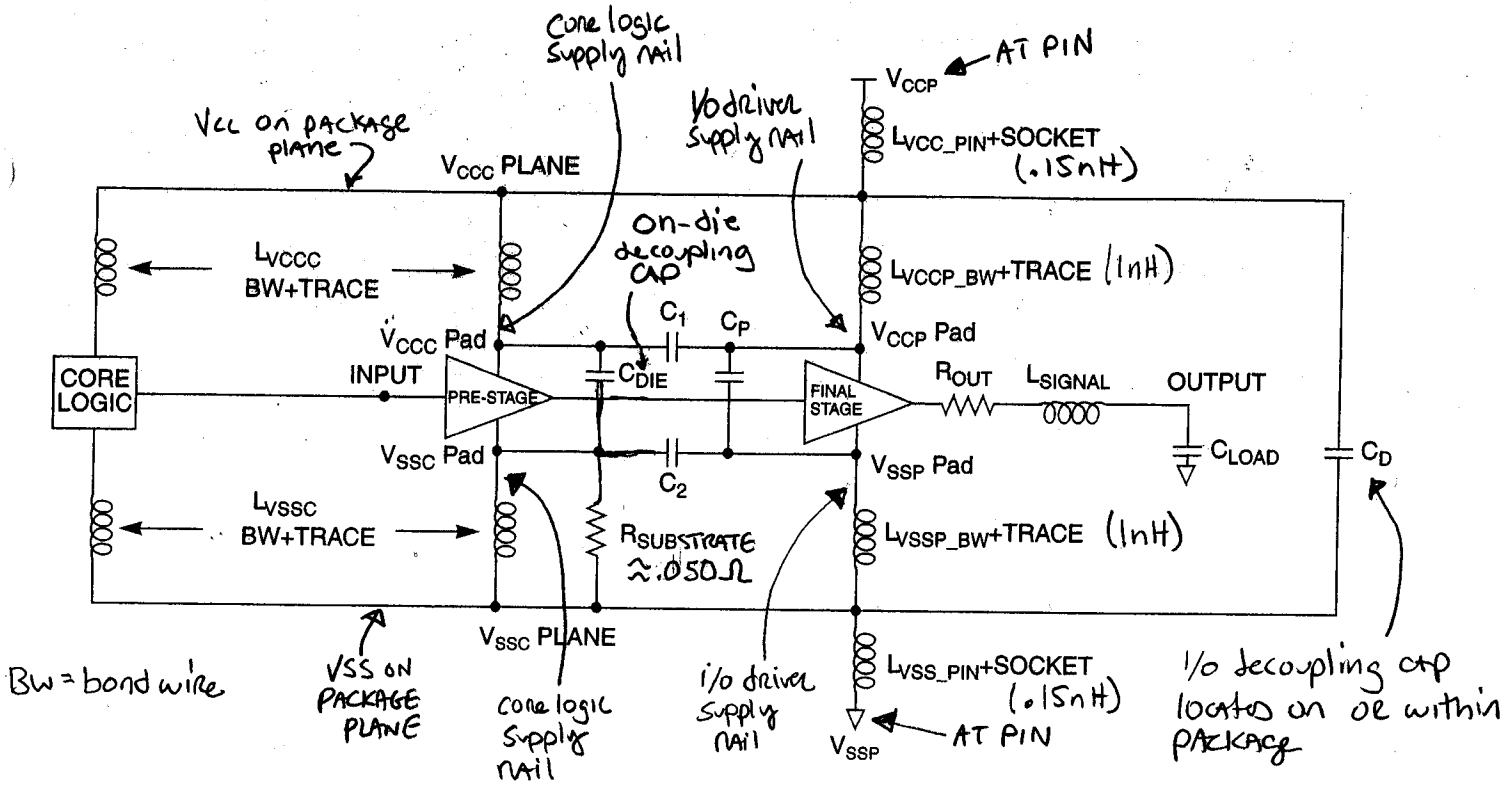
- Single driver scenario



- When P-channel xistor is "on", output is connected to VDD through a small resistor

- When N-channel xistor is "on" output is connected to Vss.

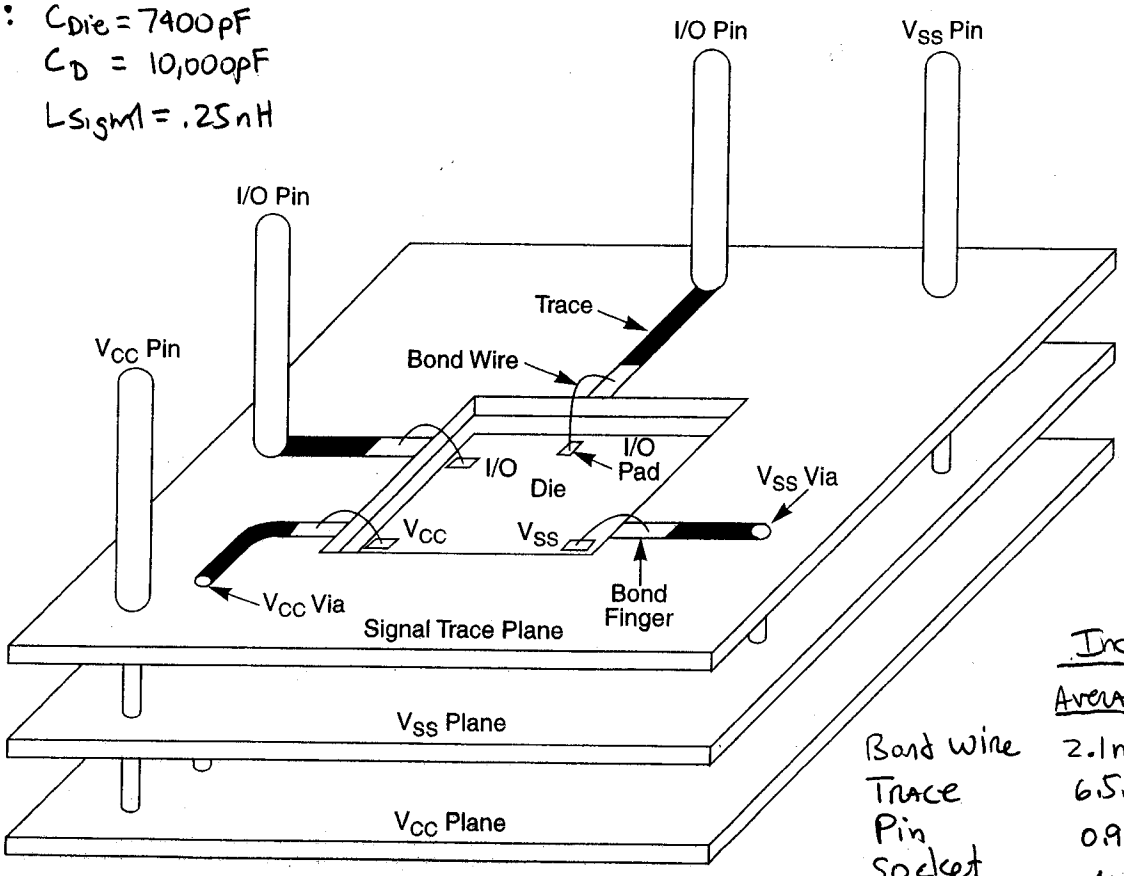
- Therefore, noise on either power rail is directly coupled to an active output.



I/O buffer and PGA circuit

Core & I/O supplys are shunted together at the pins

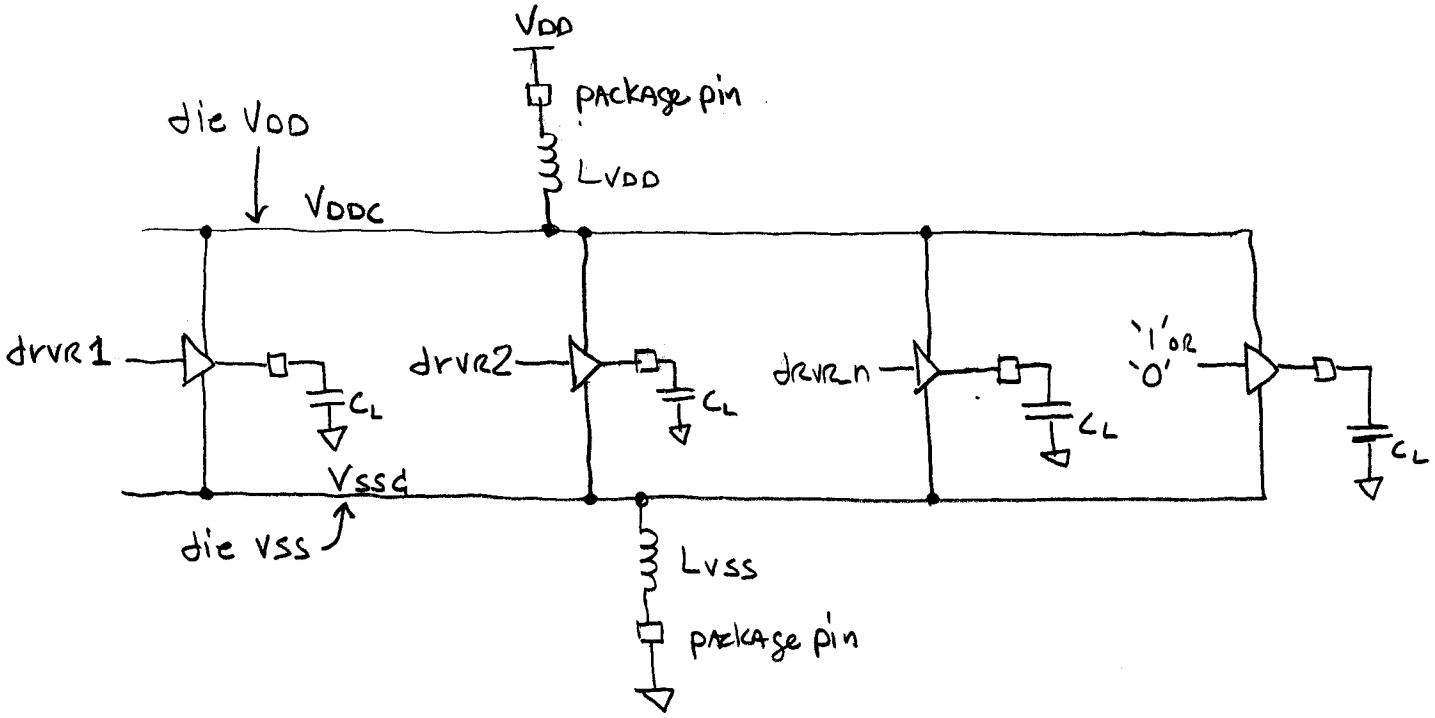
For i486: $C_{Die} = 7400pF$
$C_D = 10{,}000pF$
$L_{Sig1} = .25nH$



Simplified view of the multilayer PGA

	Inductance	
	Average	MAX
Bond wire	2.1nH	2.7nH
Trace	6.5nH	11.4nH
Pin	0.9nH	1.4nH
Socket	4nH	4nH
Leff	13.5nH	19.5nH

- Simultaneous output buffers



- An SSO situation occurs when several drivers switch at once. The worst case is when all drivers switch towards the same level. $0000_H \rightarrow FFFF_H \rightarrow 0000_H$

- The current path for all drivers is shared at the package pins through some inductance.

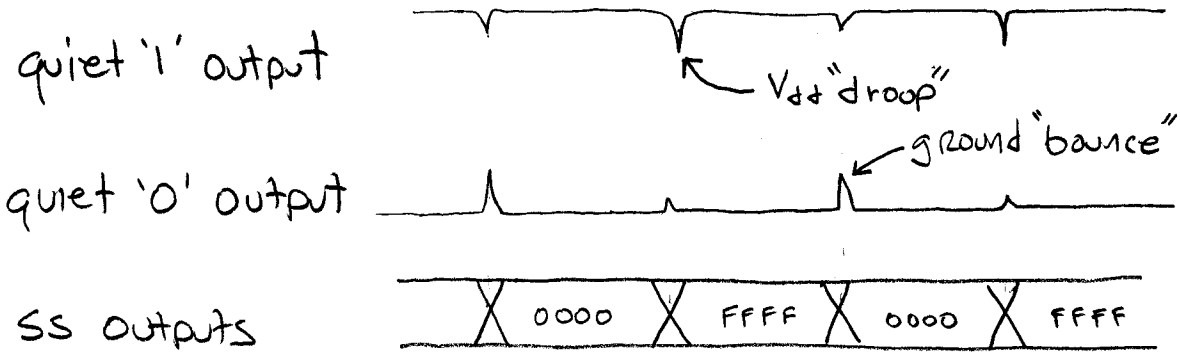
- When the outputs switch, the transient current creates a voltage across Lvss or LVDD. This voltage is:

$$V_L = L\left(\frac{di}{dt}\right) \cdot n$$

V_L = voltage across inductor
L = inductance in current path
di = instantaneous current drawn
dt = rise or fall time of output
n = number of output drivers switching to same level

If L = 15nH
load is 50Ω, capacitative
di = 100mA (5V system)
dt = 1nS
V_L = 1.5V!

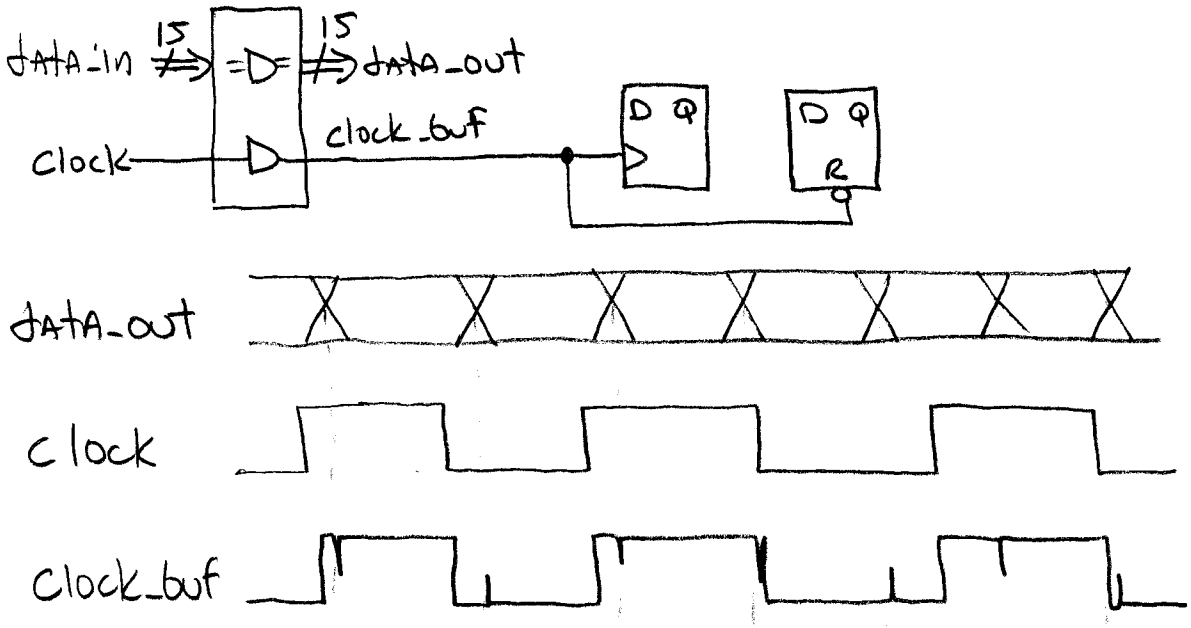
- Resultant waveform is superimposed on quiet outputs by V_{LVSS} or V_{LVDD}.



- V_{DD} droop is usually less of an issue because of greater V_H noise immunity levels

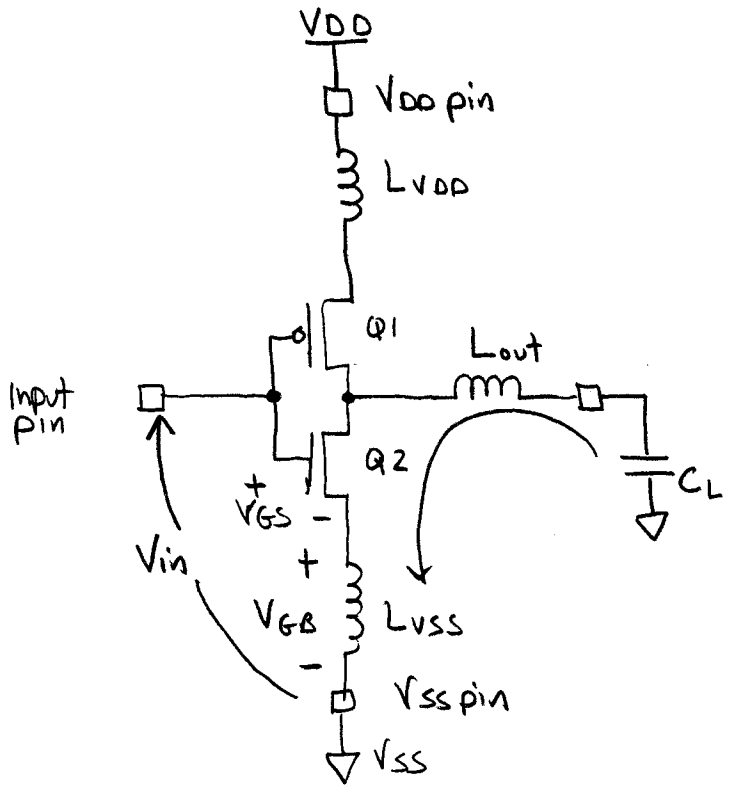
These internal perterbutations can cause malfunctions:

- gliching outputs
- increased propagation delays
- false triggering dve to dynamic threshold shift



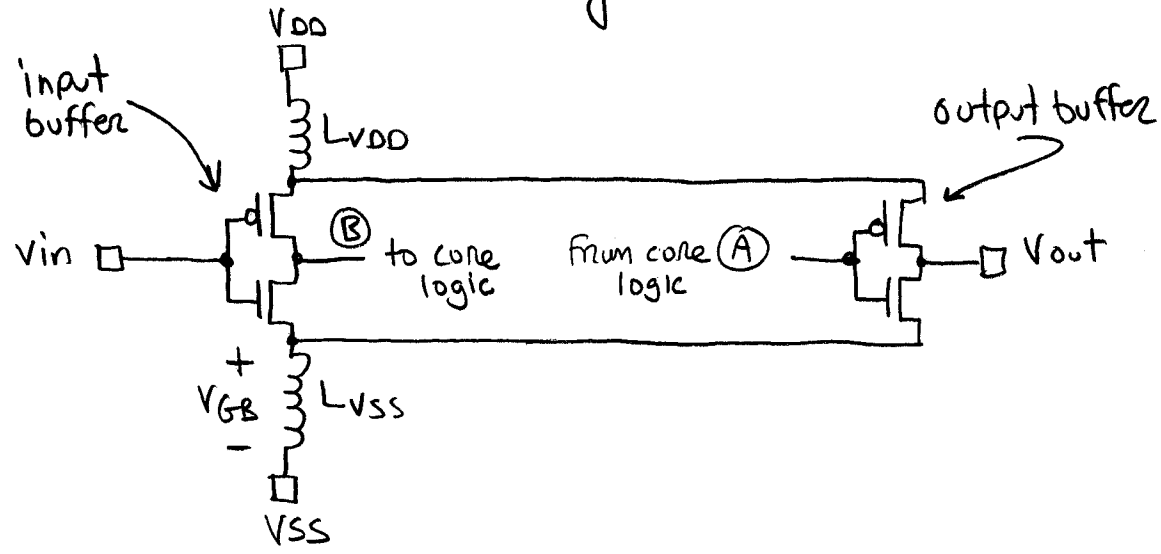
- Glitching outputs to asynchronous inputs

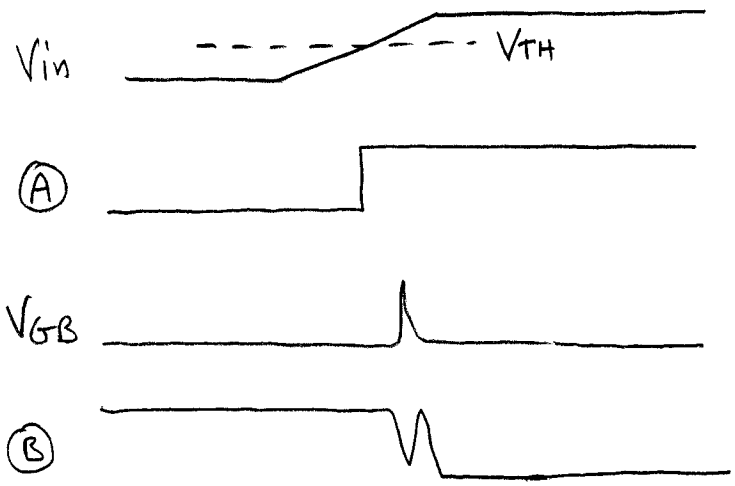
-Increased propagation delay can occur if SSO scenario occurs because output buffer current starving



- In the case where Q2 is turning on, the ground bounce voltage "V_{GB}" is substracted from V_{in} thus lowering V_{GS}. Thus $r_{DS(ON)}$ increases which reduces the rate at which the output voltage can change. This effectively increases t_{pd}.

- Dynamic threshold shifting causes input signals to be interpreted incorrectly.





- The ground bounce voltage effectively shifts the input threshold of the input buffer momentarily.

Solutions to the SSO problem
- Reduce L, reduce di/dt

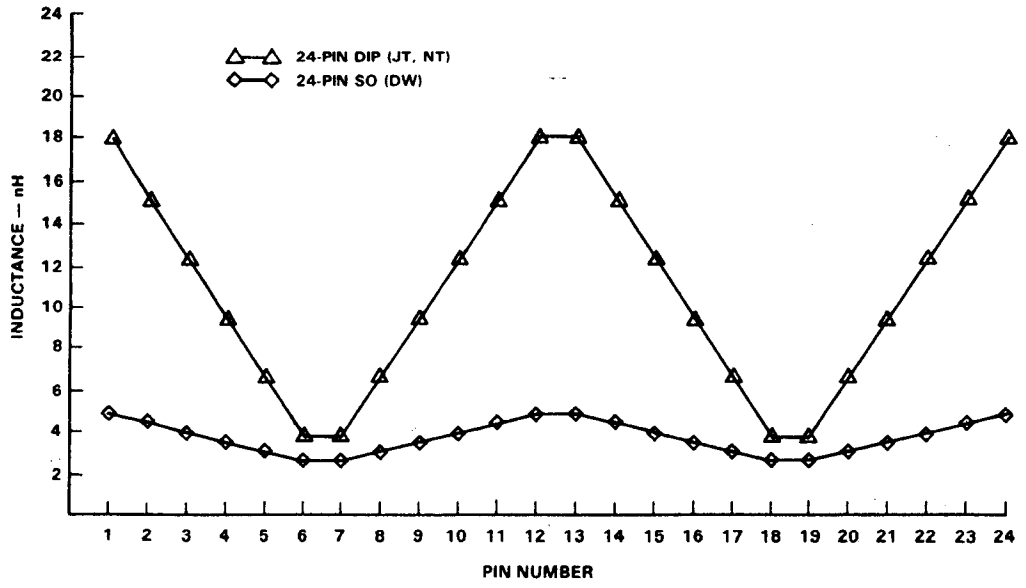
- Reducing L helps but not as much as expected.

- Reducing L also increases the current available to the output buffer when switching. This offsets the improvement somewhat.

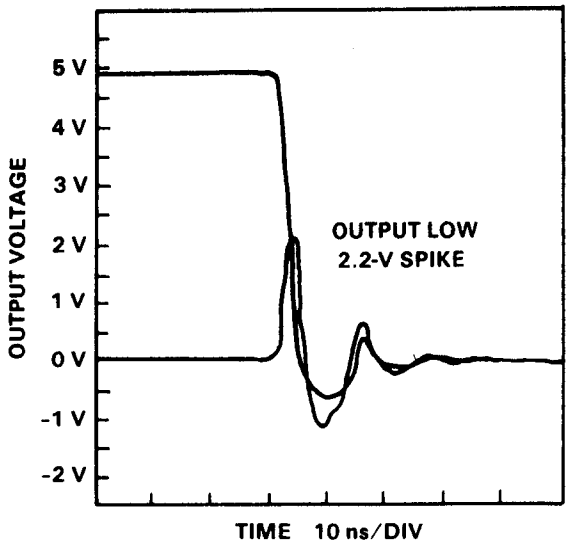
- Center pin V_{DD}, V_{SS} (1 pin each) reduces ground bounce ≈ 10-15%.

- Reducing L_{VSS}, L_{VDD} by 1 order of magnitude reduces ground bounce by ≈ 30%

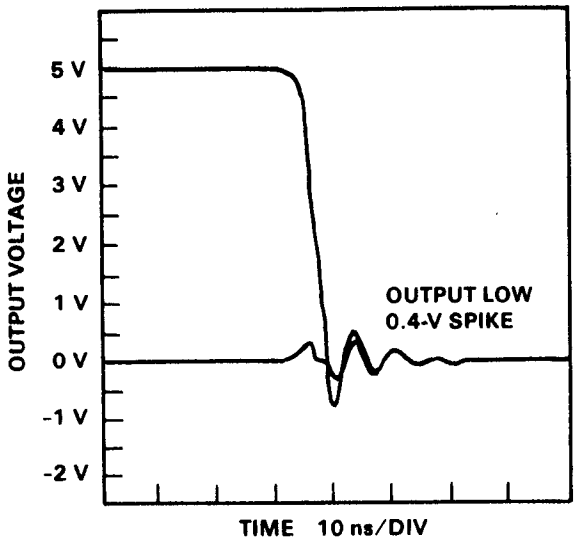
- This approach is most successful when used in conjunction with di/dt reduction.



Pin Inductance for a 24-Pin Package, End-Pin Configuration

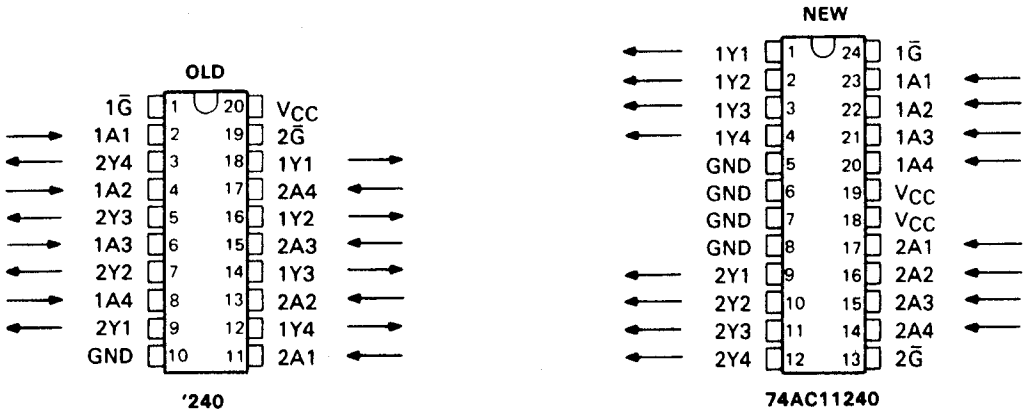


Vendor A Advanced CMOS '244 20-Pin Plastic DIP, 1 V_{CC}/1 GND, End-Pin Package



NOTE: Ground looping was not taken into account.

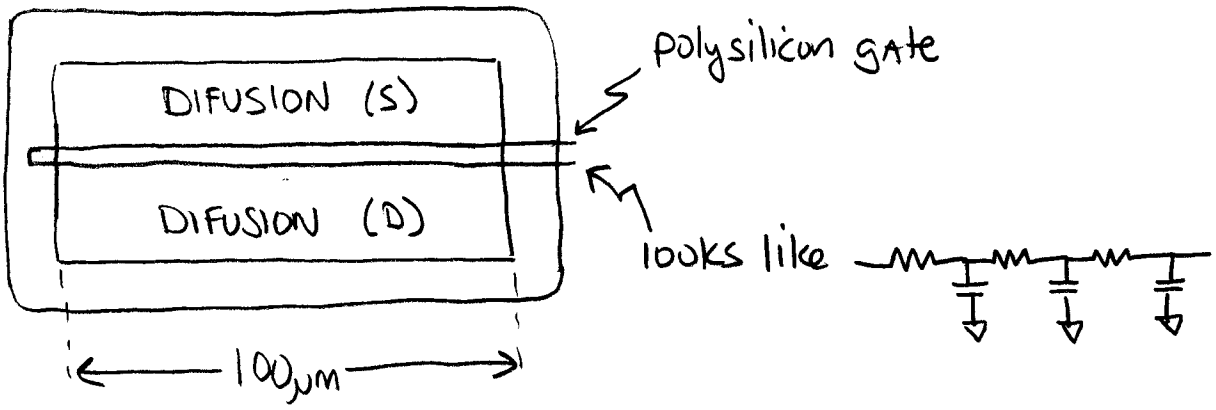
Texas Instruments 'AC11244 24-Pin Plastic DIP, 2 V_{CC}/4 GND, Center-Pin Package



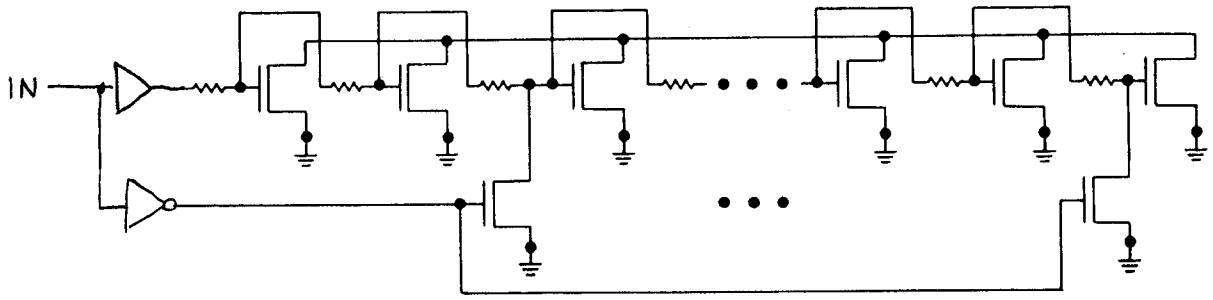
Flow-Through Pinout Architecture for an 'AC11240 Device

Output Edge Rate Control

- Addresses di/dt issue
- Gradually turn output transistors on and off
- A staged turn-on buffer

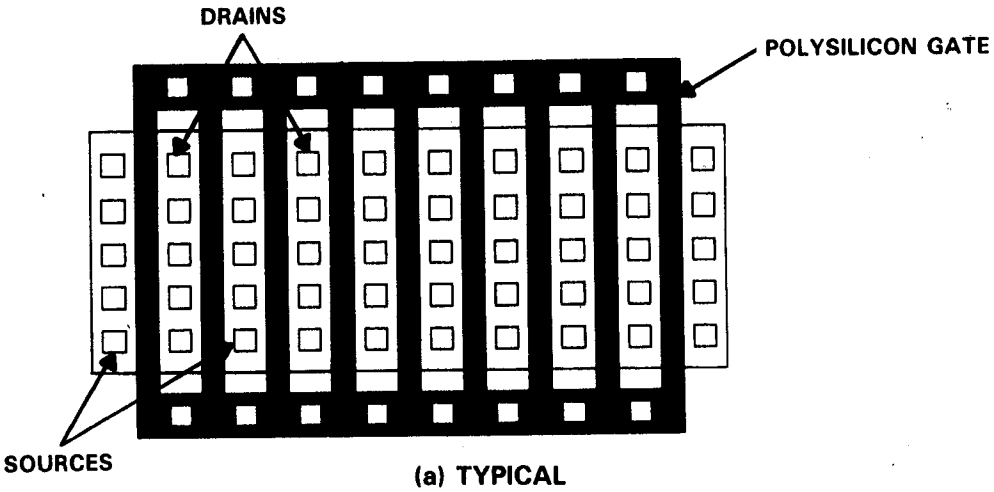


- uses distributed RC delay of polysilicon
- poly 20Ω/sq, $C'_{gox} \approx 3fF/sq$ (1.5μm CMOS)
- $RC \approx 0.06ps/sq^2$, For $W/L = 100 \Rightarrow RC = 600pS$
- TI distributes transistor solution (w/fast turn-off)

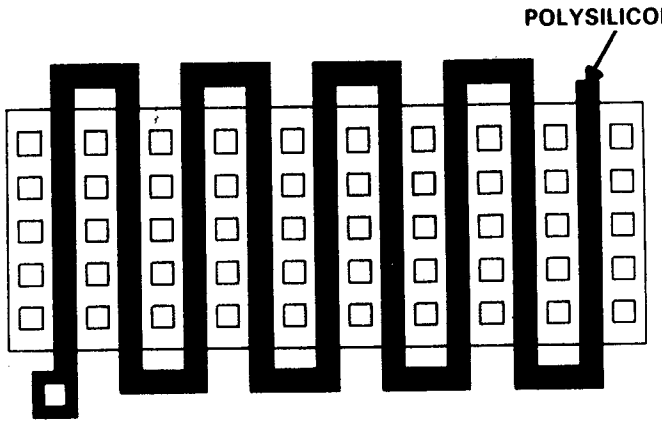


(b) DISTRIBUTED TRANSISTOR WITH ADDED PULL-DOWNS

- TI Solution cont'd

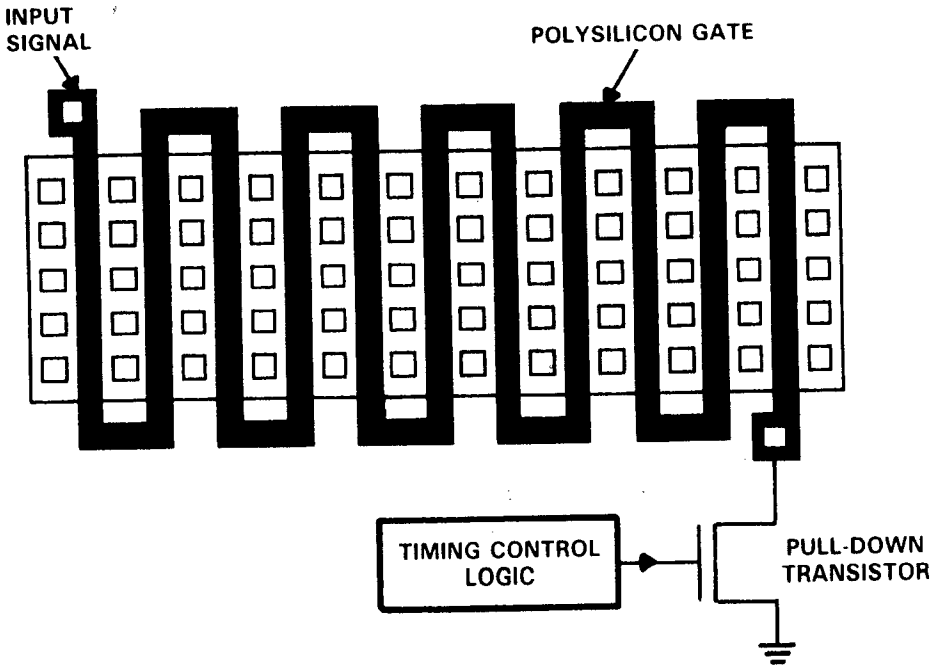


(a) TYPICAL



(b) SERPENTINE ARRANGEMENT

CMOS Transistor Gate Layout



"Distributed" N-Channel with Gate Voltage Control

What can you do to limit SSO issues?

- switch fewer outputs simultaneously
  - stagger outputs
  - use serial interface?
- AVOID lumped CAPACITATIVE LOAD, push LOAD AWAY from IC with T-line
- keep sensitive output pins near ground pin
- lower V_{DD}
- encode data (STARVATION coding)
- use lowest strength buffer possible
- use series source terminations