SECTION 6: INTEGRATED CIRCUIT BUILDING BLOCKS
On-chip real estate is at a premium
- Chip area is costly

High-value resistors consume too much area and are avoided
- Use transistor current sources for loads and biasing

High-value capacitors consume too much area
- Amplifier stages typically directly coupled

Must account for transistor output resistance
- Device dimensions are smaller

Do not have precise control over device parameters
- But, precise matching of devices is attainable

Designers have control over transistor dimensions
- Gate/channel aspect ratio: W, L for CMOS devices
- Emitter area: W, L for BJTs
Building Blocks of Integrated Circuits

- Analog integrated circuits make use of several very common building blocks:

- **Amplifiers**
  - The amplifiers we have already learned about, with some modifications
  - *Cascode amplifiers* employ current buffers between transconductance devices and loads

- **Current sources/current mirrors**
  - Active loads for amplifiers
  - Biasing for amplifiers and other circuits
Current Mirrors
Active Loads

- Transistor current sources are typically used as amplifier loads instead of resistors
  - Higher resistance, higher gain
  - Smaller area

![Diagrams of transistor current sources and amplifiers](image-url)
Current Mirrors

- Current sources are used everywhere on ICs
  - Amplifier loads
  - Transistor biasing

- Single circuit used to generate a reference current
  - Often a single bias generator circuit on a chip

- Reference current is replicated, and scaled, as needed at various circuits across the chip
  - Current steering

- Replication of current accomplished by *current mirrors*
Current mirrors have two components:

- **Transresistance** stage
  - Current-to-voltage conversion
  - Low input resistance
  - Generates a voltage \((V_{BE} \text{ or } V_{GS})\) proportional to the input current \((I_C \text{ or } I_D)\)

- **Transconductance** stage
  - Voltage-to-current conversion
  - High output resistance (a current source)
  - Generates a current \((I_C \text{ or } I_D)\) proportional to the input voltage \((V_{BE} \text{ or } V_{GS})\)
Current Mirror – Transresistance Stage

- Current-to-voltage conversion
- **Diode-tied transistor**
  - Base/collector or gate/drain connected together
  - Looks like a diode
- Reference current applied to collector or drain
- Base-emitter or gate-source voltage generated proportional to collector or drain current

\[ V_{BE} = V_{th} \ln \left( \frac{I_C}{I_S} \right) \]

\[ V_{GS} = \sqrt{\frac{2I_D}{k_n \left( \frac{W}{L} \right)}} + V_t \]
Simple MOS Transresistance Stage

- Drain current
  \[ I_{ref} = \frac{1}{2} k'_n \left( \frac{W}{L} \right) (V_{DD} - I_D R - V_t)^2 \]

- A quadratic equation for \( I_{ref} \)
  \[ R^2 I_{ref}^2 - \left[ 2(V_{DD} - V_t)R + \frac{2}{k'_n \left( \frac{W}{L} \right)} \right] I_{ref} + (V_{DD} - V_t)^2 = 0 \]

  - Solve to determine \( I_{ref} \)

- Or, to determine \( R \) for desired \( I_{ref} \):
  - Calculate overdrive voltage, \( V_{OV} \)
  - Determine gate voltage
  - Apply Ohm’s law:
    \[ R = \frac{V_{DD} - V_G}{I_{ref}} \]
Simple BJT Transresistance Stage

- Resistor in series with a diode-tied transistor
- Current through the resistor
  \[ I_{\text{ref}} = \frac{V_{CC} - V_{BE}}{R} \]
- Using the large-signal BJT model, where \( V_{BE} = 700 \, \text{mV} \):
  \[ I_{\text{ref}} = \frac{V_{CC} - V_{BE}}{R} \]
  \[ I_{\text{ref}} = \frac{V_{CC} - 700 \, \text{mV}}{R} \]
- \( V_{BE} \) is inversely proportional to temperature
  - \( I_{\text{ref}} \) increases with increasing temperature
  - A proportional-to-absolute-temperature (PTAT) current
Current Mirror – Transconductance Stage

- Voltage-to-current conversion
- Transresistance device’s output voltage applied to the base or gate of the transconductance device
- Transistor must remain in the forward active (BJT) or saturation region (MOS)
- Output current proportional to the applied voltage
- High output resistance

\[ I_o = I_s e^{V_{BE}} \]

\[ I_o = \frac{1}{2} k'_n \left( \frac{W}{L} \right) (V_{GS} - V_t)^2 \]
Simple MOS Current Mirror

- Gate-source voltages:
  \[ V_{GS} = \sqrt{\frac{2I_{ref}}{k'_n \left( \frac{W}{L} \right)_1}} + V_t \]

- Output current:
  \[ I_o = \frac{1}{2} k'_n \left( \frac{W}{L} \right)_2 (V_{GS} - V_t)^2 \]

\[ I_o = \frac{1}{2} k'_n \left( \frac{W}{L} \right)_2 \frac{2I_{ref}}{k'_n \left( \frac{W}{L} \right)_1} \]

\[ I_o = I_{ref} \left( \frac{W}{L} \right)_2 \left( \frac{W}{L} \right)_1 \]

- Output current scaled by the device aspect ratios
  - The *current transfer ratio* or current gain of the mirror
Simple BJT Current Mirror

- First, assume $\beta \approx \infty$
- Base-emitter voltages:
  \[ V_{BE} = V_{th} \ln \left( \frac{I_{ref}}{I_{S_1}} \right) \]
- Output current:
  \[ I_o = I_{S_2} e^{V_{BE} / V_{th}} = I_{S_2} e^{\ln(I_{ref}) / I_{S_1}} \]
  \[ I_o = I_{ref} \frac{I_{S_2}}{I_{S_1}} = I_{ref} \frac{A_{E_2}}{A_{E_1}} \]
- Output current is the reference current scaled by the emitter area ratios
  - The current transfer ratio:
  \[ \frac{I_o}{I_{ref}} = \frac{A_{E_2}}{A_{E_1}} = m \]
Now, accounting for finite $\beta$

Collector currents still scale with emitter area

$$I_o = I_{C2} = I_{C1} \frac{A_{E2}}{A_{E1}} = m \cdot I_{C1}$$

The current transfer ratio:

$$I_{ref} = I_{C1} + \frac{I_{C1}}{\beta} + \frac{I_o}{\beta} = \frac{I_o}{m} + \frac{I_o}{m \beta} + \frac{I_o}{\beta}$$

$$I_{ref} = I_o \left( \frac{1}{m} + \frac{1}{m \beta} + \frac{1}{\beta} \right)$$

$$I_{ref} = I_o \left( \frac{\beta + 1 + m}{m \beta} \right)$$

$$\frac{I_o}{I_{ref}} = \frac{m}{1 + \frac{m + 1}{\beta}}$$
BJT Current Mirror With $\beta$ Compensation

- Addition of a transistor can reduce the effect of base current on the current transfer ratio
- KCL at the collector of $Q_1$:

\[ I_{ref} = I_{C1} + I_{B3} = \frac{I_0}{m} + \frac{I_{C3}}{\beta} \]

\[ I_{ref} = \frac{I_0}{m} + \frac{\beta}{(\beta + 1) \beta} I_{E3} \]

where

\[ I_{E3} = \frac{I_{C1}}{\beta} + \frac{I_{C2}}{\beta} = \frac{I_0}{m\beta} + \frac{I_0}{\beta} \]

Substituting into the expression for $I_{ref}$:

\[ I_{ref} = \frac{I_0}{m} + \frac{I_0}{\beta(\beta + 1)} \left( \frac{1}{m} + 1 \right) \]
BJT Current Mirror With $\beta$ Compensation

\[ I_{\text{ref}} = \frac{I_o}{m} + \frac{I_o}{\beta(\beta + 1)} \left( \frac{1}{m} + 1 \right) \]

\[ I_{\text{ref}} = I_o \left[ \frac{1}{m} + \frac{m + 1}{m\beta(\beta + 1)} \right] \]

- The current transfer ratio:
  \[ \frac{I_o}{I_{\text{ref}}} = \frac{1}{\frac{1}{m} + \frac{m + 1}{m\beta(\beta + 1)}} \]

\[ \frac{I_o}{I_{\text{ref}}} = \frac{m}{1 + \frac{m + 1}{\beta(\beta + 1)}} \]

- The error term has been improved by a factor of $(\beta + 1)$
For BJTs emitter area scaling is typically accomplished by connecting multiple devices in parallel.

For example ($\beta = \infty$):
An important figure of merit for any current source is its output resistance.
- For an ideal current source, $R_o = \infty$.
- For simple BJT and MOS current mirrors the output resistance is $r_o$ of the transconductance transistor.

\[ R_o = r_o = \frac{V_A}{I_C} \]

\[ R_o = r_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D} \]
Current Mirror – Example

- Determine the output current, \( I_o \)
- Solve the quadratic for \( I_{\text{ref}} \) :
  \[
  R^2 I_{\text{ref}}^2 - \left[ 2(V_{DD} - V_t)R + \frac{2}{k_n' \left( \frac{W}{L} \right)} \right] I_{\text{ref}} + (V_{DD} - V_t)^2 = 0
  \]
  \[
  (47 \, k\Omega)^2 I_{\text{ref}}^2 - \left[ 2(2.6 \, V)47 \, k\Omega + \frac{2}{1.9 \, mA/V^2} \right] I_{\text{ref}} + (2.6 \, V)^2 = 0
  \]
  \[
  2.248e9 \cdot I_{\text{ref}}^2 - 247,593 \cdot I_{\text{ref}} + 6.76 = 0
  \]
  \[
  I_{\text{ref}} = 50.4 \, \mu A
  \]
- Output current scales with transistor aspect ratio
  \[
  I_o = I_{\text{ref}} \left( \frac{W}{L} \right)_1^2 = 50.4 \, \mu A \cdot \frac{15}{10}
  \]
  \[
  I_o = 75.6 \, \mu A
  \]

\( V_{DD} = 3.3 \, V \)
\( R = 47 \, k\Omega \)

\( \mu_n C_{ox} = 190 \, \frac{\mu A}{V^2} \)
\( V_t = 700 \, mV \)
\( \left( \frac{W}{L} \right)_1 = 10 \)
\( \left( \frac{W}{L} \right)_2 = 15 \)
Current Steering – Example

- Determine all collector currents and node voltages
  - Assume $\beta = \infty$ and $V_{BE} = 700 \, mV$
Current Steering – Example

\[ I_{C1} = I_{C2} = \frac{(+5 \, V - V_{BE}) - (-5 \, V + V_{BE})}{R_1} = \frac{8.6 \, V}{10 \, k\Omega} = 860 \, \mu \text{A} \]

\[ I_{C3} = I_{C2} = 860 \, \mu \text{A} \]

\[ V_{C3} = I_{C3}R_2 = 860 \, \mu \text{A} \cdot 2 \, k\Omega = 1.72 \, V \]

\[ I_{C4} = I_{C3} = 860 \, \mu \text{A} = I_{C5} = I_{C6} \]

\[ V_{C6} = +5 \, V - I_{C6}R_3 = +5 \, V - 860 \, \mu \text{A} \cdot 3.6 \, k\Omega = 1.904 \, V \]

\[ I_{C7} = I_{C8} = I_{C9} = I_{C1} = 860 \, \mu \text{A} \]

\[ V_{C7,8} = -(I_{C7} + I_{C8}) \cdot 2 \, k\Omega = -1.72 \, mA \cdot 2 \, k\Omega = -3.44 \, V \]

\[ I_{C10} = I_{C11} = I_{C9} = 860 \, \mu \text{A} \]

\[ V_{C11} = I_{C11} \cdot 10 \, k\Omega = 860 \, \mu \text{A} \cdot 10 \, k\Omega = 8.6 \, V \]
The Basic Gain Cell
Basic Gain Cell

- The basic gain cell used in integrated circuit (IC) amplifiers
  - Common-emitter or common-source amplifier
  - Load resistance replaced with a transistor current source – an *active load*

- Benefits of an active load
  - Provides both a high-resistance load and bias current
  - Consumes less chip area than a resistor
  - Enables higher gain
To understand why active loads can provide high gain, consider a resistively-loaded CS amplifier:

Amplifier gain:

$$ |A_v| = g_m R_D $$

where

$$ g_m = k'_n \left( \frac{W}{L} \right) V_{OV} $$

And, since

$$ I_D = \frac{1}{2} k'_n \left( \frac{W}{L} \right) V_{OV}^2 $$

we can express $g_m$ as

$$ g_m = \frac{I_D}{\frac{1}{2} V_{OV}} $$
The amplifier gain becomes:

\[ |A_v| = g_m R_D = \frac{I_D R_D}{\frac{1}{2} V_{OV}} \]

The numerator represents the voltage drop across \( R_D \):

\[ |A_v| = \frac{V_{DD} - V_{DS}}{\frac{1}{2} V_{OV}} \]

For active region operation, \( V_{DS} \geq V_{OV} \), so the maximum gain is

\[ |A_v|_{max} = \frac{V_{DD} - V_{OV}}{\frac{1}{2} V_{OV}} \]
Amplifier gain

- For an IC amplifier with $V_{DD} = 3.3$ V and $V_{OV} = 200$ mV max gain is only

$$|A_v|_{max} = \frac{1.1 \text{ V}}{100 \text{ mV}} = 11$$

- Note that at this bias point (i.e., the edge of triode, $V_{DS} = V_{OV}$), the amplifier’s dynamic range is zero
  - An absolute limit, not a usable gain

- Active loads allow for higher gain, because:
  - voltage drop across the load is decoupled from current and from high small-signal resistance
  - They are not resistors, so are not constrained by Ohm’s law
Active Loads and Biasing

- Note that, in order to remain in the active region, $I_D$ or $I_C$ set by $V_{GS}$ or $V_{BE}$ must exactly match that of the current-source load.

- You are only getting part of the story here:
  - In practice, additional circuitry, including negative feedback stabilizes the bias point.

- For now, just assume that the DC component of the input is such that its bias current matches the current source.
Basic Gain Cell - Gain

- Small-signal models for the amplifiers:

- Treat the current sources as ideal
  - Infinite resistance – open circuit
  - In practice it would be a transistor output resistance

- Transistor $r_o$ is the only load

- For both amplifiers, the gain is
  \[ A_v = -g_m r_o \]

- This is the maximum possible CS or CE gain
  - The intrinsic gain, $A_0$
Intrinsic Gain – MOSFET

For the MOSFET, 

\[ g_m = \frac{I_D}{V_{OV}/2} \]

\[ r_o = \frac{V_A}{I_D} \]

So, the intrinsic gain is 

\[ A_0 = -\frac{V_A}{V_{OV}/2} \]

- Proportional to the Early voltage
- Inversely proportional to channel length, \( L \)
- Inversely proportional to the overdrive voltage, \( V_{OV} \)
- Inversely proportional to drain current, \( I_D \)
Intrinsic Gain – BJT

\[
A_0 = -g_m r_o
\]

- For the BJT,

\[
g_m = \frac{I_C}{V_t}
\]

\[
r_o = \frac{V_A}{I_C}
\]

- So, the intrinsic gain is

\[
A_0 = -\frac{V_A}{V_t}
\]

- Proportional to the Early voltage
- Inversely proportional to collector current, \( I_C \)

- BJTs vs. MOSFETs
  - \( V_t \) is much smaller than typical overdrive voltages (e.g. \( 150 - 300 \ mV \))
  - \( V_A \) is typically larger for BJTs
  - In comparable modern processes, BJT intrinsic gain is an order of magnitude higher than that of MOSFETs
Finite Current-Source Resistance

- In practice, active loads are not ideal current sources
  - Transistor current sources
  - Resistance is the $r_o$ of that transistor
  - Appears in parallel with the amplifier transistor’s $r_o$
  - Gain will be significantly lower than the intrinsic gain

\[ A_v = -g_m r_{o1} \parallel r_{o2} \]

- Next, we’ll see how we can increase gain by increasing the output resistance, $r_{o1} \parallel r_{o2}$
CG/CB Amplifiers as Current Buffers
Increasing the Gain

- If we can increase \( r_{o1} || r_{o2} \), we can increase gain.
- For now, we’ll focus on increasing \( r_{o1} \).
  - I.e., the resistance seen looking back toward the amplifier transistor.

![Transistor Diagram]
Current Buffers

- The amplifier transistor’s output current is applied to the active load transistor, where it is converted to a voltage.

- Want a device that will:
  - Replicate that current
  - Apply it to the active load
  - Do so with a higher $r_o$

- A **current buffer**
  - Low input resistance
    - Input current unaffected
  - High output resistance
    - Approximating an ideal current source
    - Gain will be increased
Current Buffers

- We have already seen transistor circuits that fit this description of a current buffer
  - *Common-base* amplifier
  - *Common-gate* amplifier

- We now revisit these circuits, looking more closely at the characteristics that make them suitable current buffers:
  - Current gain
  - Input resistance
  - Output resistance
Consider the following CB amplifier
- Current source input with finite source resistance, $R_S$
- Load resistance, $R_L$

The small-signal equivalent circuit:
First, we will determine the short-circuit current gain for the CB amplifier

\[ A_{is} = \frac{i_o}{i_s} \]

For the short circuit-current gain, the output is shorted to ground

The small-signal circuit simplifies to
Common-Base – Current Gain

- Note that the voltage across the VCCS is the source’s controlling voltage, $v_{be}$
- The VCCS, therefore, can be replaced by a resistance:

Output current is given by current division:

$$i_o = i_s \frac{g_m + \frac{1}{r_o}}{g_m + \frac{1}{r_o} + \frac{1}{R_S||r_\pi}}$$
Common-Base – Current Gain

- The short-circuit current gain is

\[ A_{is} = \frac{i_o}{i_s} = \frac{g_m + \frac{1}{r_o}}{g_m + \frac{1}{r_o} + \frac{1}{R_S || r_\pi}} \]

- If \( r_o \gg \frac{1}{g_m} \) and \( R_S || r_\pi \gg \frac{1}{g_m} \), then the current gain is approximately unity

\[ A_{is} \approx 1 \]

- As would be desired for a current buffer
To determine the input resistance, apply a test voltage source, $v_t$, and determine the resulting current, $i_t$.

KVL around the loop:

$$v_t - i_2 r_o - i_c R_L = 0$$  \hspace{1cm} (1)

KCL at the input node:

$$i_t + g_m v_{be} - i_1 - i_2 = 0$$

$$i_t + g_m v_{be} - \frac{v_t}{r_\pi} - i_2 = 0$$

Note that $v_{be} = -v_t$, so

$$i_t - g_m v_t - \frac{v_t}{r_\pi} - i_2 = 0$$

$$i_2 = i_t - g_m v_t - \frac{v_t}{r_\pi}$$  \hspace{1cm} (2)
KCL at the collector gives the collector current

\[ i_c = i_2 - g_m v_{be} = i_2 + g_m v_t \]

\[ i_c = i_t - g_m v_t - \frac{v_t}{r_\pi} + g_m v_t \]

\[ i_c = i_t - \frac{v_t}{r_\pi} \]  \hspace{1cm} (3)

Substituting (2) and (3) into (1):

\[ v_t - i_t r_o + g_m r_o v_t + \frac{v_t}{r_\pi} r_o - i_t R_L + \frac{v_t R_L}{r_\pi} = 0 \]

\[ v_t \left(1 + g_m r_o + \frac{r_o}{r_\pi} + \frac{R_L}{r_\pi}\right) = i_t (r_o + R_L) \]  \hspace{1cm} (4)
The input resistance is

\[ R_i = \frac{v_t}{i_t} = \frac{r_o + R_L}{1 + g_m r_o + \frac{r_o + R_L}{r_\pi + r_\pi}} \]  

We can simplify (5) by noting the following:

\[ g_m r_o \gg 1 \]

\[ \frac{r_o}{r_\pi} \approx \frac{g_m r_o}{\beta} \ll g_m r_o \]

\[ \frac{R_L}{r_\pi} \approx \frac{g_m R_L}{\beta} \ll g_m r_o \]

The input resistance simplifies to

\[ R_i \approx \frac{r_o + R_L}{g_m r_o} = \frac{1}{g_m} + \frac{R_L}{g_m r_o} = r_e + \frac{R_L}{g_m r_o} \]
Common-Base – Input Resistance

- **Common-base input resistance:**
  
  \[ R_i \approx \frac{1}{g_m} + \frac{R_L}{g_m r_o} = r_e + \frac{R_L}{g_m r_o} \]  

- **Two components to** \( R_i \):
  - Emitter resistance, \( r_e \)
    - Typically small
  - Load resistance, \( R_L \), *reduced by the transistor’s intrinsic gain*
    - Effect of \( R_L \) reduced

- \( R_i \) is typically small, as desired from a current buffer
Common-Base – Output Resistance

- To determine output resistance, $R_o$, apply a test voltage to the output.
- Applying KVL
  \[ v_t - i_1 r_o - i_2 (R_E || r_\pi) = 0 \]  \hspace{1cm} (7)
- Applying KCL gives
  \[ i_1 = i_t - g_m v_{be} \]  \hspace{1cm} (8)
  \[ i_2 = i_1 + g_m v_{be} = i_t \]  \hspace{1cm} (9)
- The base-emitter voltage is
  \[ v_{be} = -i_2 (R_E || r_\pi) = -i_t (R_E || r_\pi) \]  \hspace{1cm} (10)
- Substituting (8), (9), and (10) into (7) gives
  \[ v_t - i_t r_o - g_m i_t (R_E || r_\pi) r_o - i_t (R_E || r_\pi) = 0 \]  \hspace{1cm} (11)
Rearranging (11) gives the output resistance

\[ R_o = \frac{v_t}{i_t} = r_o + (R_E||r_\pi) + g_m r_o (R_E||r_\pi) \]

\[ R_o = r_o + (1 + g_m r_o)(R_E||r_\pi) \]  \hspace{1cm} (12)

We can simplify, assuming \( g_m r_o \gg 1 \)

\[ R_o \approx r_o + g_m r_o (R_E||r_\pi) \]  \hspace{1cm} (13)

And, if \( g_m (R_E||r_\pi) \gg 1 \), then

\[ R_o \approx g_m r_o (R_E||r_\pi) \]

Here, the resistance at the input is increased by the transistor’s intrinsic gain

\( R_o \) will typically be a large resistance, as would be desired
Consider the following CG amplifier
- Current source input with finite source resistance, $R_S$
- Load resistance, $R_L$

The small-signal equivalent circuit:
To determine short-circuit current gain, $A_{is}$, we can simplify the small-signal circuit just as we did for the CB circuit:

Output current is given by current division:

$$i_o = i_s \frac{g_m + \frac{1}{r_o}}{g_m + \frac{1}{r_o} + \frac{1}{R_s}}$$
Common-Gate – Current Gain

- The short-circuit current gain is
  \[ A_{is} = \frac{i_o}{i_s} = \frac{g_m + \frac{1}{r_o}}{g_m + \frac{1}{r_o} + \frac{1}{R_S}} \]

- If \( r_o \gg \frac{1}{g_m} \) and \( R_S \gg \frac{1}{g_m} \), then the current gain is approximately unity
  \[ A_{is} \approx 1 \]

- As desired, and similar to the CB amplifier
To determine the input resistance, apply a test voltage source, \( v_t \), and determine the resulting current, \( i_t \).

KVL around the loop:

\[
v_t - i_1 r_o - i_d R_L = 0
\]  

(14)

KCL at the input node:

\[
i_1 = i_t + g_m v_{gs} = 0
\]

Note that \( v_t = -v_{gs} \), so

\[
i_1 = i_t - g_m v_t
\]  

(15)

Substituting (15) into (14) and noting that drain and source currents are equal

\[
v_t - i_t r_o + g_m r_o v_t - i_t R_L = 0
\]

\[
v_t (1 + g_m r_o) = i_t (r_o + R_L)
\]  

(16)
Common-Gate – Input Resistance

- Solving (16) gives the input resistance:
  \[ R_i = \frac{v_t}{i_t} = \frac{r_o + R_L}{1 + g_m r_o} \]  
  (17)

- For \( g_m r_o \gg 1 \), \( R_i \) simplifies to
  \[ R_i \approx \frac{1}{g_m} + \frac{R_L}{g_m r_o} \]  
  (18)

- Two components to \( R_i \)
  - The input resistance when neglecting \( r_o \)
  - The load resistance *reduced by the intrinsic gain*
Common-Gate – Output Resistance

- To determine output resistance, $R_o$, apply a test voltage to the output.

- Applying KVL
  \[ v_t - i_1 r_o - i_s R_S = 0 \]  \hspace{1cm} (19)

- Applying KCL gives
  \[ i_1 = i_t - g_m v_{gs} \]  \hspace{1cm} (20)

- The gate-source voltage is
  \[ v_{gs} = -i_s R_S = -i_t R_S \]  \hspace{1cm} (21)

- Substituting (20) and (21) into (19) gives
  \[ v_t - i_t r_o - g_m i_t R_S r_o - i_t R_S = 0 \]  \hspace{1cm} (22)
Common-Gate – Output Resistance

- Rearranging (22) gives the output resistance

\[ R_o = \frac{v_t}{i_t} = r_o + R_S + g_m r_o R_S \]

\[ R_o = r_o + (1 + g_m r_o) R_S \quad (23) \]

- We can simplify, assuming \( g_m r_o \gg 1 \)

\[ R_o \approx r_o + g_m r_o R_S \quad (24) \]

- If we assume \( g_m r_o \gg 1 \), we can simplify further

\[ R_o \approx g_m r_o R_S \]

- Here, the resistance at the input is **increased by the transistor’s intrinsic gain**

- \( R_o \) will typically be a relatively large resistance
Common-Base/Common-Gate - Summary

$$A_{is} = \frac{g_m + 1}{g_m + \frac{1}{r_o} + \frac{1}{R_S}||r_\pi}} \approx 1$$

$$R_i = \frac{r_o + R_L}{1 + g_m r_o + \frac{r_o}{r_\pi} + \frac{R_L}{r_\pi}}$$

$$R_i \approx \frac{1}{g_m} + \frac{R_L}{g_m r_o} = r_e + \frac{R_L}{g_m r_o}$$

$$R_o = r_o + (1 + g_m r_o) (R_E||r_\pi)$$

$$R_o \approx r_o + g_m r_o (R_E||r_\pi)$$

$$R_o \approx g_m r_o (R_E||r_\pi)$$
Cascode Amplifiers
Recall the gain of a basic gain cell with an active load

\[ A_v = -g_{m1}R_o = -g_{m1}(r_{o1}\parallel r_{o2}) \]

We can increase this gain by increasing \( r_{o1} \) or \( r_{o2} \).

First, we’ll focus on \( r_{o1} \) by adding a cascode device.

Now, \( R_o \) becomes

\[ R_o = R_{on}\parallel R_{op} = R_{on}\parallel r_{o3} \]

where

\[ R_{on} = g_{m2}r_{o2}(r_{o1}) \]

The gain is then

\[ A_v = -g_{m1}(R_{on}\parallel r_{o3}) \]
\[ A_v = -g_{m1}[(g_{m2}r_{o2}r_{o1})\parallel r_{o3}] \]

\( r_{o1} \) has been increased by a factor of \( g_{m2}r_{o2} \)

Gain is increased significantly.
For the BJT cascode, $R_{on}$ is

$$R_{on} = g_m r_2 (r_1 || r_2)$$

And the gain is

$$A_v = -g_m (R_{on} || r_3)$$

$$A_v = -g_m [(g_m r_2 (r_1 || r_2)) || r_3]$$

A bit more complicated result than for the MOS circuit

- Gain still significantly increased

Note that in both cases, we have only improved one component of $R_o$

- We can further increase gain by increasing $r_3$ as well
We can further increase $R_o$ and gain by adding a cascode device to the active load transistor
   - Increases $r_{o3}$ and $R_{op}$

Now, $R_{op}$ is

$$R_{op} = g_{m3} r_{o3} (r_{o4})$$

The gain is

$$A_v = -g_{m1} (R_{on} || R_{op})$$

$$A_v = -g_{m1} [(g_{m2} r_{o2} r_{o1}) || (g_{m3} r_{o3} r_{o4})]$$

Now $r_{o4}$ has been increased by a factor of $g_{m3} r_{o3}$
   - Another significant gain increase
For the BJT cascode amplifier, the cascode device on the active load increases $R_{op}$ similarly

$$R_{op} = g_m r_3 (r_{o4} \parallel r_{\pi3})$$

The gain is

$$A_v = -g_m (R_{on} \parallel R_{op})$$

$$A_v = -g_m \{[g_m r_2 (r_{o1} \parallel r_{\pi2})] [g_m r_3 (r_{o4} \parallel r_{\pi3})]\}$$

Again, the result is a bit more complicated than for the MOS circuit

- Resulting increase of gain is similar
Find the gain of the basic gain cell in a 0.18 \mu m CMOS process with the given parameters

Gain is given by

\[ A_v = -g_{m1}R_o = -g_{m1}r_{o1}||r_{o2} \]

The transistor transconductances:

\[ g_{m1} = \sqrt{2k'_{n} \left( \frac{W}{L} \right)_{n} I_D} \]

\[ g_{m1} = \sqrt{2 \cdot 387 \frac{\mu A}{V^2} \cdot 10 \cdot 100 \mu A} \]

\[ g_{m1} = 880 \mu S \]
Cascode Amplifier – Example 1

- The transistor output resistances:

\[ r_{o1} = \frac{V_{An}}{I_D} = \frac{5 \text{ V}}{100 \, \mu\text{A}} = 50 \, \text{k}\Omega \]
\[ r_{o2} = \frac{V_{Ap}}{I_D} = \frac{6 \text{ V}}{100 \, \mu\text{A}} = 60 \, \text{k}\Omega \]

- The gain:

\[ A_v = -g_{m1}r_{o1}||r_{o2} \]
\[ A_v = -880 \, \mu\text{S} \cdot 50 \, \text{k}\Omega || 60 \, \text{k}\Omega \]
\[ A_v = -880 \, \mu\text{S} \cdot 27.3 \, \text{k}\Omega \]

\[ A_v = -24 \]
Next, add a cascode device and determine the resulting gain

Now, the gain is given by

\[ A_v = -g_{m1}R_o = -g_{m1}R_{on}||r_{o3} \]

Transconductance of the NMOS devices is unchanged:

\[ g_{m1} = g_{m2} = 880 \mu S \]

As are all output resistances

\[ r_{o1} = r_{o2} = 50 \text{k}\Omega \]

\[ r_{o3} = 60 \text{k}\Omega \]
Cascode Amplifier – Example 2

- The resistance looking into the drain of $Q_2$ is
  \[ R_{on} = g_{m2}r_{o2} \cdot r_{o1} \]
  \[ R_{on} = 880 \mu S \cdot 50 \, k\Omega \cdot 50 \, k\Omega \]
  \[ R_{on} = 44 \cdot 50 \, k\Omega = 2.2 \, M\Omega \]

- The gain:
  \[ A_v = -g_{m1}R_{on}||r_{o3} \]
  \[ A_v = -880 \mu S \cdot 2.2 \, M\Omega||60 \, k\Omega \]
  \[ A_v = -880 \mu S \cdot 58.4 \, k\Omega \]
  \[ A_v = -51.4 \]

- The cascode transistor increased the gain from 24 to 51.4
  - A relatively small increase compared to the 44x increase in $R_{on}$
  - $R_o$ dominated by $r_{o3}$
Finally, add a cascode device to the current-source load and determine the gain:

\[ A_v = -g_{m1}R_o = -g_{m1}R_{on} \parallel R_{op} \]

Now, the gain is given by

\[ A_v = -g_{m1}R_o = -g_{m1}R_{on} \parallel R_{op} \]

Transconductance of the PMOS devices:

\[ g_{m3} = g_{m4} = \sqrt{2k'_p \left( \frac{W}{L} \right)_p I_D} \]

\[ g_{m3} = \sqrt{2 \cdot 86 \frac{\mu A}{V^2} \cdot 50 \cdot 100 \mu A} \]

\[ g_{m3} = 927 \mu S \]

All other quantities are the same

\[ I_D = 100 \mu A \]

\[ \mu_n C_{ox} = 387 \frac{\mu A}{V^2} \]

\[ \mu_p C_{ox} = 86 \frac{\mu A}{V^2} \]

\[ \left( \frac{W}{L} \right)_n = \frac{10 \mu m}{1 \mu m} \]

\[ \left( \frac{W}{L} \right)_p = \frac{50 \mu m}{1 \mu m} \]

\[ V_{An} = 5 V \]

\[ V_{Ap} = 6 V \]
The resistance looking into the drain of $Q_3$ is

$$R_{op} = g_{m3}r_{o3} \cdot r_{o4}$$

$$R_{op} = 927 \, \mu S \cdot 60 \, k\Omega \cdot 60 \, k\Omega$$

$$R_{op} = 55.6 \cdot 60 \, k\Omega = 3.34 \, M\Omega$$

The gain:

$$A_v = -g_{m1}R_{on} || R_{op}$$

$$A_v = -880 \, \mu S \cdot 2.2 \, M\Omega || 3.34 \, M\Omega$$

$$A_v = -880 \, \mu S \cdot 1.33 \, M\Omega$$

$$A_v = -1167$$

Cascode current-source load results in a significant gain increase

- Both components of $R_o$ were increased by a factor of $g_m r_o$
Improved Current Mirrors
Current Mirror Performance

- There are three main current-mirror figures of merit:
  - **Current transfer ratio**
    - How closely does the output current match the input/reference current?
    - A function of the Early effect and of $\beta$ (BJTs)
  - **Output resistance**
    - Enables higher amplifier gain if used as an active load
    - Also affects current transfer ratio
      - How much is output current affected by output voltage?
  - **Overhead voltage**
    - What is the minimum voltage required at the output such that the transistors remain in the active region?
- We will now look at a few circuits that aim to improve on one or more of these characteristics
As we have seen, a cascode device can improve output resistance.

A MOSFET cascode current mirror:
- Assume matched devices (i.e., \( m = 1 \))
- Output resistance:
  \[
  R_o = g_m r_{o3} \cdot r_{o2}
  \]
- Voltage at the gate of \( Q_3/Q_4 \):
  \[
  V_{G3} = 2(V_t + V_{OV})
  \]
- To remain in the active region:
  \[
  V_{D3} > V_t + 2V_{OV}
  \]
- If, for example, \( V_t = 500 \text{ mV} \) and \( V_{OV} = 200 \text{ mV} \)
  \[
  V_{D3} > 900 \text{ mV}
  \]
- A significant portion of the total supply voltage
Cascode Current Mirror – BJT

- The BJT cascode current mirror:
- Output resistance:
  \[ R_o = g_{m3} r_{o3} (r_{o2} \| r_{\pi3}) \]
- Voltage at the base of \( Q_3/Q_4 \):
  \[ V_{B3} = 2V_{BE} \]
- To remain in the active region:
  \[ V_{C3} > V_{B3} = 2V_{BE} \]
  \[ V_{C3} > \sim 1.4 \, V \]
  - Again, a significant portion of the total supply voltage
- Cascode does not affect the current transfer ratio:
  \[ \frac{I_o}{I_{ref}} = \frac{1}{1 + \frac{2}{\beta}} \]
The Wilson current mirror uses **negative feedback** to increase $R_o$

- Output current, $I_o$, is applied to the current mirror formed by $Q_2$ and $Q_1$
- Mirrored $I_o$ is fed back to the gate of $Q_3$
- $I_{G3} = 0$, so $I_o$ must be equal to $I_{ref}$
- If $I_o > I_{ref}$, $V_{G3}$ will drop, decreasing $I_o$
- If $I_o < I_{ref}$, $V_{G3}$ will rise, increasing $I_o$

Output resistance:

$$R_o = g_{m3}r_{o3} \cdot r_{o1} + r_{o3} + \frac{1}{g_{m2}}$$

$$R_o \approx g_{m3}r_{o3} \cdot r_{o1}$$

Same $R_o$ as for the cascode current mirror
Wilson mirror can be improved by adding a fourth transistor
- $Q_4$ helps to balance the drain-source voltages for $Q_1$ and $Q_2$
- Reduces current-transfer-ratio errors
Wilson Current Mirror – BJT

- Benefits of the Wilson mirror are greater for BJTs than for MOSFETs
  - $\beta$-related current error reduced
- Current transfer ratio:
  \[
  \frac{I_o}{I_{ref}} = \frac{1}{1 + \frac{2}{\beta(\beta + 2)}}
  \]
  \[
  \frac{I_o}{I_{ref}} \approx \frac{1}{1 + \frac{2}{\beta^2}}
  \]
  - Error significantly reduced compared to the simple mirror and cascode mirror
- Output resistance:
  \[
  R_o = \left(\frac{\beta_3}{2} + 1\right)r_{o3} + \frac{1}{2g_{m2}}
  \]
  \[
  R_o \approx \frac{\beta_3}{2}r_{o3}
  \]
Improved Wilson Mirror – BJT

- Similar to the MOSFET circuit, current-transfer-ratio error can be reduced by adding a fourth transistor to balance the $Q_1$ and $Q_2$ collector voltages
Widlar Current Source – BJT

- Widlar current source adds an emitter resistor on the output transistor
- More of a source than a mirror
  - Current not replicated from one branch to the other
- Can generate small currents without the need for very large resistors
- Output resistance:

\[ R_o \approx [1 + g_{m2}(R_E2||r_{\pi2})]r_{o2} \]
We can illustrate the function and benefit of a Widlar current source through an example

- Compare the Widlar current source to a basic current mirror

Design each source below for $I_o = 10 \, \mu A$

- Emitter areas are equal
- $I_s = 2 \times 10^{15} \, A = 2 \, fA$
First, design the basic current mirror

The reference and output currents are equal

\[ I_{ref1} = I_o = 10 \, \mu A \]

Use \( I_{ref1} \) to determine \( V_{BE} \)

\[ V_{BE} = V_T \ln \left( \frac{I_{ref1}}{I_s} \right) = 26 \, mV \ln \left( \frac{10 \, \mu A}{2 \, fA} \right) \]

\[ V_{BE} = 581 \, mV \]

Determine the value of \( R_1 \)

\[ R_1 = \frac{V_{CC} - V_{BE1}}{I_{ref1}} = \frac{3.3 \, V - 581 \, mV}{10 \, \mu A} \]

\[ R_1 = 272 \, k\Omega \]
Widlar Current Source – Example

Next, design the Widlar source

Here, we can choose the reference current

\[ I_{ref2} = 1 \text{ mA} \]

Use \( I_{ref2} \) to determine \( V_{BE1} \)

\[ V_{BE1} = V_T \ln \left( \frac{I_{ref2}}{I_s} \right) = 26 \text{ mV} \ln \left( \frac{1 \text{ mA}}{2 \text{ fA}} \right) \]

\[ V_{BE1} = 700 \text{ mV} \]

Determine the value of \( R_2 \)

\[ R_2 = \frac{V_{CC} - V_{BE1}}{I_{ref1}} = \frac{3.3 \text{ V} - 700 \text{ mV}}{1 \text{ mA}} \]

\[ R_2 = 2.6 \text{ k}\Omega \]
Next, determine \( R_3 \)

- KVL around the B-E loop gives
  \[
  V_{BE1} - V_{BE2} - I_{O2} R_3 = 0
  \]
  \[ R_3 = \frac{V_{BE1} - V_{BE2}}{I_{O2}} \]

- We already determined \( V_{BE2} \)
  \[
  V_{BE2} = 26 \text{ mV} \ln \left( \frac{10 \mu A}{2 fA} \right) = 581 \text{ mV}
  \]

- So, \( R_3 \) is
  \[
  R_3 = \frac{700 \text{ mV} - 581 \text{ mV}}{10 \mu A} = 11.9 \text{ k\Omega}
  \]

\[
R_2 = 2.6 \text{ k\Omega} \text{ and } R_3 = 11.9 \text{ k\Omega}
\]

- Both much smaller than required for the basic mirror (272 k\Omega)